(2)

Review of The MOSFET

(**M**etal-**O**xide-**S**emiconductor **F**ield **E**ffect **T**ransistor)

Reference: Neamen, Chapter 3 and Chapter 4

1

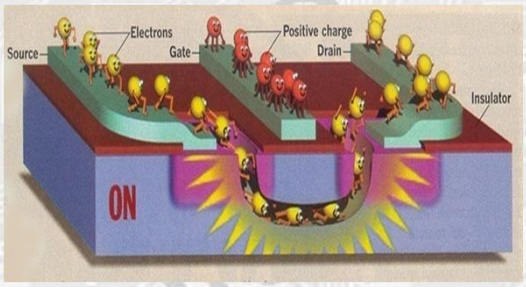
Learning Outcome

Able to:

- Understand the **general operation** of n-channel and p-channel enhancement-mode MOSFETs.
- Apply the **ideal current-voltage relations** in the dc analysis and design of various MOSFET circuits.
- Describe the **small-signal equivalent circuit of the MOSFET** and able to determine the values of the small-signal parameters.

2

2.1) Field Effect Transistor (FET)



The voltage between two terminals (G-S) controls the current through the third terminal (D)

3

2.2) MOSFET Characteristics and Properties

2.2.1) Circuit Symbols and Conventions

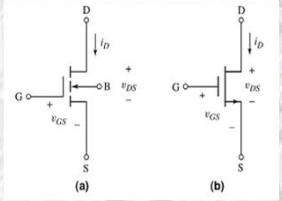


Figure 3.12: The **n-channel** enhancement-mode MOSFET (**NMOS**): (a) conventional circuit symbol, and (b) **simplified** circuit symbol used.

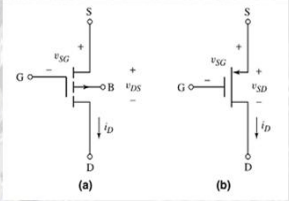


Figure 3.13: The **p-channel** enhancement-mode MOSFET (**PMOS**): (a) conventional circuit symbol, and (b) **simplified** circuit symbol used.

4

2.2) MOSFET Characteristics and Properties (Cont)

2.2.2) Basic Principle of Operation

"The voltage between two terminals (G-S) controls the current through the third terminal (D)."

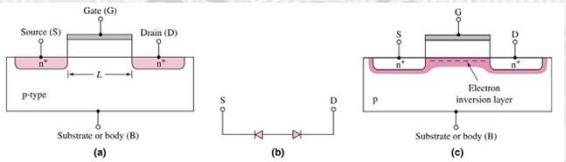


Figure 3.6: (a) Cross section of the n-channel MOSFET prior to formation of an electron inversion layer, (b) equivalent back-to-back diodes between source and drain when transistor is in cut off, and (c) cross-section after the formation of an electron inversion layer.

5

2.2) MOSFET Characteristics and Properties (Cont)

2.2.2) Basic Principle of Operation (Cont)

a) Operation of NMOS:

- **+ve voltage applied to GATE (G)** creates an electric field in the underlying p-type substrate. This forces holes down into the substrate and attracts electrons towards the surface.
- For **zero or small** V_{GS}, the **SOURCE (S)** and **DRAIN (D)** terminals are separated by the p-region (like two back-to-back diodes). Hence, **no current can flow** between S and D.
- For **larger** V_{GS}, the region near the surface becomes inverted (i.e. changes from p-type to n-type) and an **n-channel inversion layer is created** between the S and D terminals. This provides **current flow from D to S**.
- Appreciable channel conduction occurs only when V_{GS} **exceeds Threshold voltage,** V_{TN}.

2.2) MOSFET Characteristics and Properties (Cont)

2.2.2) Basic Principle of Operation (Cont)

b) Operation of PMOS:

The operation of **p-channel device** is the same except:
- Å The **hole is the carrier** rather than the electron.
- Å **Negative gate bias** is required to induce an inversion layer of holes (because substrate is of **n-type**).
- Å **Current flows from S to D**.
- Å **Threshold** voltage for p-channel device is denoted as V_{TP}.

In both types of MOSFET (i.e. **NMOS and PMOS**), the **GATE is electrically isolated** from the channel by the oxide layer,

hence I_G = 0 (No gate current!)

7

2.2) MOSFET Characteristics and Properties (Cont)

2.2.3) Modes of Operation

There are **3 modes** of operation:

Region	NMOS	PMOS
Cut off	$0 < v_{GS} < V_{TN}$ $i_D = 0$	$0 < v_{SG} < V_{TP}$ $i_D = 0$
Non-saturation	$v_{GS} > V_{TN}$ $v_{DS} < v_{GS} - V_{TN}$ $i_D \neq 0$	$v_{SG} > V_{TP}$ $v_{SD} < v_{SG} + V_{TP}$ $i_D \neq 0$
Saturation	$v_{GS} > V_{TN}$ $v_{DS} \geq v_{GS} - V_{TN}$ $i_D \neq 0$	$v_{SG} > V_{TP}$ $v_{SD} \geq v_{SG} + V_{TP}$ $i_D \neq 0$

Saturation region is usually used for amplifier circuits.

8

2.2) MOSFET Characteristics and Properties (Cont)

2.2.4) Current-voltage Relationships

Region	NMOS	PMOS
Non-saturation	$v_{DS} < v_{DS}(\text{sat})$ $i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$v_{SD} < v_{SD}(\text{sat})$ $i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation	$v_{DS} \geq v_{DS}(\text{sat})$ $i_D = K_n[v_{GS} - V_{TN}]^2$	$v_{SD} \geq v_{SD}(\text{sat})$ $i_D = K_p[v_{SG} + V_{TP}]^2$
Transition Point	$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$	$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$
Enhancement Mode	$V_{TN} > 0$ V	$V_{TP} < 0$ V
Depletion Mode	$V_{TN} < 0$ V	$V_{TP} > 0$ V

9

2.2) MOSFET Characteristics and Properties (Cont)

2.2.5) Conduction Parameters, K_n and K_p

Å NMOSFET: $K_n = \frac{W\mu_n C_{ox}}{2L} = \frac{k_n'}{2}\cdot\frac{W}{L}$

Å PMOSFET: $K_p = \frac{W\mu_p C_{ox}}{2L} = \frac{k_p'}{2}\cdot\frac{W}{L}$

where: $C_{ox} = \varepsilon_{ox}/t_{ox}$

is the oxide capacitance per unit area

10

2.2) MOSFET Characteristics and Properties (Cont)

2.2.5) Conduction Parameters , K_n and K_p (Cont)

μ_n	mobility of electrons
μ_p	mobility of holes
ε_{ox}	oxide permittivity
t_{ox}	oxide **t**hickness
W	channel **W**idth
L	channel **L**ength
$k'_n = \mu_n C_{ox}$	process conduction parameter (provided by manufacturer for a particular process)

➔ The channel geometry, i.e. **width-to-length ratio (*W/L*)**, is a variable in the design of MOSFETs that **can be utilized to produce specific current-voltage characteristics** in MOSFET circuits.

11

2.2) MOSFET Characteristics and Properties (Cont)

2.2.5) Conduction Parameters , K_n and K_p (Cont)

Schematic of **n-Channel** Enhancement Mode MOSFET

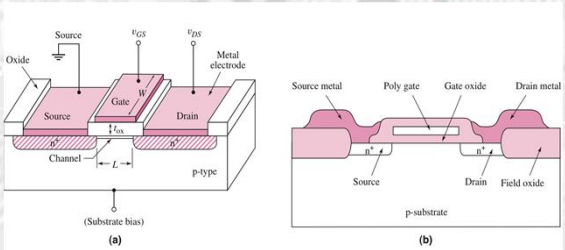
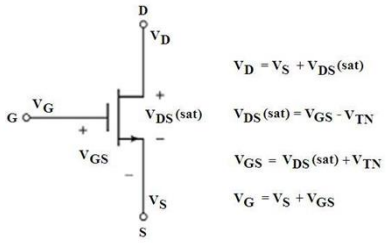


Figure 3.5

12

2.2) MOSFET Characteristics and Properties (Cont)

2.2.6) Voltage Relationships



Useful relationships → DO NOT FORGET!

13

2.2) MOSFET Characteristics and Properties (Cont)

2.2.7) MOSFET Operating Curve

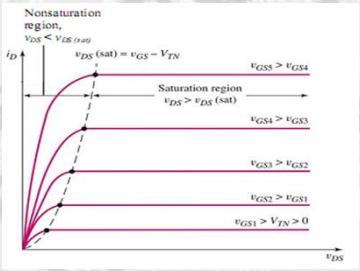


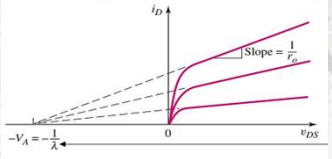
Figure 3.15: Family of i_D **versus** v_{DS} curves for NMOS

14

2.2) MOSFET Characteristics and Properties (Cont)

2.2.8) Finite Output Resistance

In an actual MOSFET, the output curve has a finite slope beyond the saturation point due to **channel length modulation** (as $v_{DS} > v_{DS}$(sat)), the point of inversion zero charge moves away from D terminal causing a reduction of channel length).



λ is a positive quantity called channel length modulation parameter

Figure 3.20: Effect of **channel length modulation**, resulting in a finite output resistance

15

2.2) MOSFET Characteristics and Properties (Cont)

2.2.8) Finite Output Resistance (Cont)

The effect of Finite Output Resistance (r_o) is included in the **drain current** equation:

$$i_D = K_n[v_{GS} - V_{TN}]^2 \rightarrow i_D = K_n\left[(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})\right]$$

Output resistance:

$$r_o = \left[\frac{\partial v_{DS}}{\partial i_D}\right]\Big|_{v_{GS}=const} \cong \frac{1}{\lambda I_{DQ}}$$

where I_{DQ} **= quiescent drain current**.

16

2.3) DC Analysis Of MOSFET Circuits

➔ DC biasing of MOSFET amplifiers is required to obtain **saturation mode** of operation

Step 1	Assume transistor is biased in the saturation region, i.e. $V_{GS} > V_{TN}$, $I_D > 0$ and $V_{DS} \geq V_{DS}$(sat).
Step 2	Analyze the circuit using the saturation current-voltage relations. ❑ Calculate V_G and V_{GS} from the biasing circuit. ❑ Calculate I_D. ❑ Perform KVL on D-S (or S-D) loop to find V_{DS} (or V_{SD}).

17

2.3) DC Analysis Of MOSFET Circuits (Cont)

➔ DC biasing of MOSFET amplifiers is required to obtain **saturation mode** of operation

Step 3	Evaluate the resulting bias condition of the transistor. If the assumed parameter values in step 1 are valid, then the initial assumption is correct. However, ❑ if $V_{GS} < V_{TN}$, then the transistor is probably cut off, and ❑ if $V_{DS} < V_{DS}$(sat), the transistor is likely to be biased in non-saturation.
Step 4	If the initial assumption is proven incorrect, then a new assumption must be made and the circuit reanalyzed. **Step 3** must then be repeated.

18

2.3) DC Analysis Of MOSFET Circuits (Cont)

Example of a Common-Source Circuit

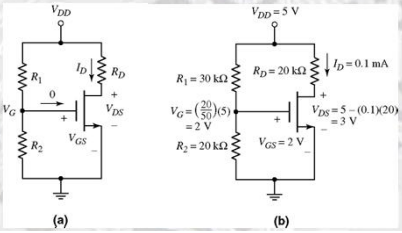


Fig 3.25: (a) An NMOS common-source circuit and (b) the NMOS circuit for Example 3.3

Example 3.3: Calculate the I_D and V_{DS}
(Note: V_{TN} = 1V and K_n = 0.1mA/V²)

19

2.4) AC Analysis Of MOSFET Circuits

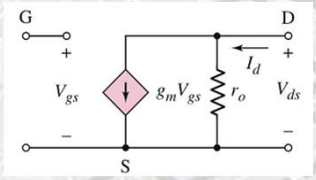
- In the MOSFET amplifier analysis, superposition theory applies, i.e. perform dc and ac analysis separately.

Step 1	Analyze with only dc sources present to give the dc or quiescent solution. The transistor must be **biased in the saturation region** in order to produce a linear amplifier.
Step 2	Replace each element in the circuit with its small-signal model, including replacing the transistor by its small-signal equivalent model. **To draw the small-signal model of the amplifier circuit:** ❑ **Start with the three terminals of the transistor.** ❑ **Then sketch equivalent circuit between these terminals.** ❑ **Connect the small-signal model of the remaining circuit elements to the transistor terminals.**
Step 3	**Analyze the small-signal equivalent circuit, setting the dc source components equal to zero, to produce the response of the circuit to time-varying input signals only.**

20

2.4) AC Analysis Of MOSFET Circuits (Cont)

2.4.1) Small-signal Hybrid-π Equivalent Circuit of MOSFET



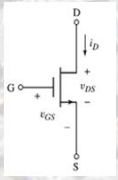


Figure 4.6: Expanded **small-signal** equivalent circuit, including output resistance (r_o), for **NMOS transistor**.

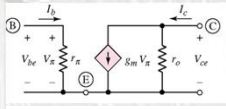


Figure 6.13: NPN BJT

21

2.4) AC Analysis Of MOSFET Circuits (Cont)

2.4.1) Small-signal Hybrid-π Equivalent Circuit of MOSFET (Cont)

- **Transconductance:**

$$g_m = \frac{\partial i_D}{\partial v_{GS}}\Big|_{v_{GS}=V_{GSQ}=const} = 2K_n\left(V_{GSQ} - V_{TN}\right) = 2\sqrt{K_n I_{DQ}}$$

- **Small-signal transistor output resistance:**

$$r_o = \left[\frac{\partial v_{DS}}{\partial i_D}\right]\Big|_{v_{GS}=V_{GSQ}=const} = \frac{1}{\lambda K_n\left(V_{GSQ} - V_{TN}\right)^2} \cong \frac{1}{\lambda I_{DQ}}$$

Note: The small-signal model of a PMOS transistor is the same as in **Figure 4.6** but with all ac voltage polarities and current directions reversed. All the parameter equations **stated above** still apply for the PMOS transistor.

22

2.5) Basic Single Stage MOSFET Amplifiers

2.5.1) Basic Common-Source (CS) Amplifier Circuit

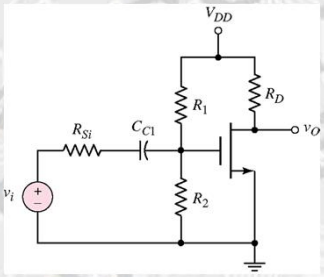


Figure 4.14: Common-source circuit with voltage-divider biasing and coupling capacitor.

23

2.5) Basic Single Stage MOSFET Amplifiers (Cont)

2.5.1) Basic Common-Source (CS) Amplifier Circuit (Cont)

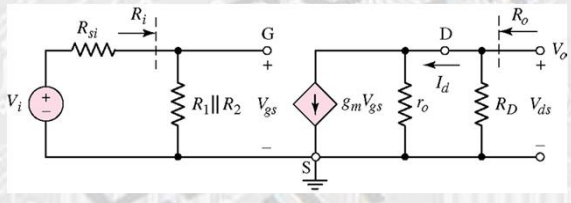


Figure 4.15: Small-signal equivalent circuit, assuming the coupling capacitor is a short circuit.

24

2.5) Basic Single Stage MOSFET Amplifiers (Cont)

2.5.2) Common-Source (CS) Amplifier with Source Resistor

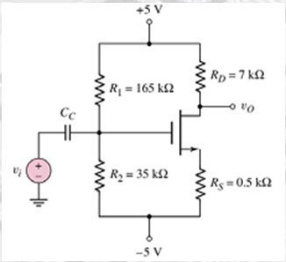


Figure 4.19: Common-source circuit with source resistor and positive and negative supply.

25

2.5) Basic Single Stage MOSFET Amplifiers (Cont)

2.5.2) CS Amplifier with Source Resistor (Cont)

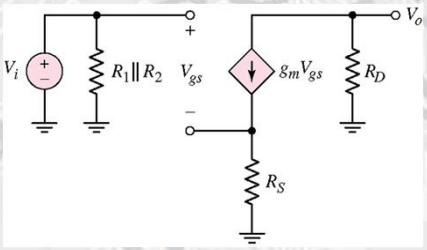


Figure 4.20: Small-signal equivalent circuit of NMOS common-source amplifier with source resistor.

26

2.5) Basic Single Stage MOSFET Amplifiers (Cont)

2.5.3) Common-Drain (CD) Amplifier a.k.a Source Follower

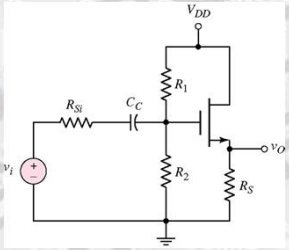


Figure 4.26: NMOS source-follower or common-drain amplifier.

27

2.5) Basic Single Stage MOSFET Amplifiers (Cont)

2.5.3) Common-Drain (CD) Amplifier a.k.a Source Follower (Cont)

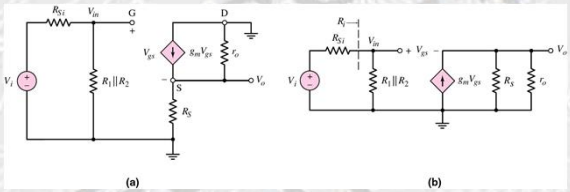


Figure 4.27:
(a) Small-signal equivalent circuit of NMOS source-follower and
(b) Small-signal equivalent circuit of NMOS source-follower with all signal grounds at a common point

28

2.5) Basic Single Stage MOSFET Amplifiers (Cont)

2.5.4) Common-Gate (CG) Amplifier

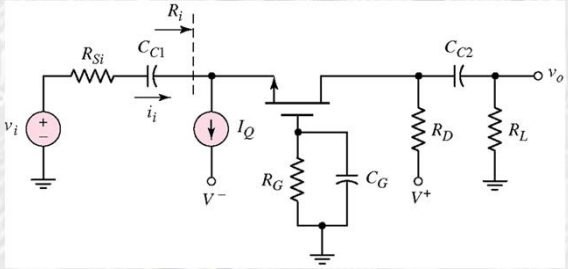


Figure 4.32: Common-gate circuit.

29

2.5) Basic Single Stage MOSFET Amplifiers (Cont)

2.5.4) Common-Gate (CG) Amplifier (Cont)

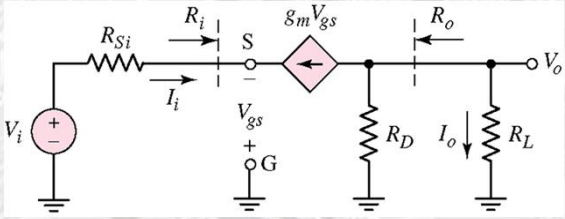


Figure 4.33: Small-signal equivalent circuit of common-gate amplifier.

30