(4) MOSFET Current Sources

Reference: Neamen, Chapter 10

Learning Outcome

Able to:

- Analyze and design a basic two-transistor MOSFET current-source circuit with additional MOSFET devices in the reference portion of the circuit to obtain a given bias current.
- Analyze and design more sophisticated MOSFET current-source circuits, such as the cascode circuit, Wilson circuit, and wide-swing cascode circuit.
- Analyze the output resistance of the various MOSFET current-source circuits and design a MOSFET current-source circuit to obtain a specified output resistance.

4.0) FET Integrated Circuit Biasing

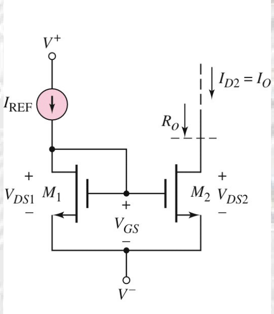
- Field-effect transistor (**FET**) ICs are biased **with current sources in the same way as bipolar circuits**.

Problem-Solving Technique

- Analyze the reference side of the circuit to determine gate-to-source voltages. Using these gate-to-source voltages, determine the bias current in terms of the reference current.
- To find the output resistance, place a test voltage at the output node and analyze the small-signal equivalent circuit. Keep in mind that the reference current is constant, which may make some of the gate voltages constant or at ac ground.

4.1) Basic Two-Transistor MOSFET Current Source

4.1.0) The Circuit



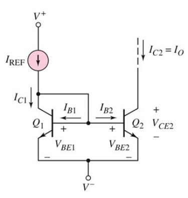
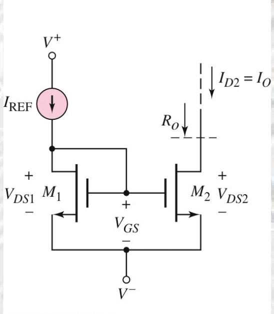


Figure 10.2: Basic two-transistor **BJT** current source.

Fig 10.16: Basic two-transistor **N-MOSFET** current source

4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.1) Current Relationship



- M_1 is **always biased in saturation region** because the drain and gate terminals of enhancement-mode M_1 are connected.

Fig 10.16: Basic two-transistor **N-MOSFET** current source.

4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.1) Current Relationship (Cont)

- **When $\lambda = 0$**: $$I_{REF} = K_{n1}(V_{GS} - V_{TN1})^2 \quad (10.40)$$

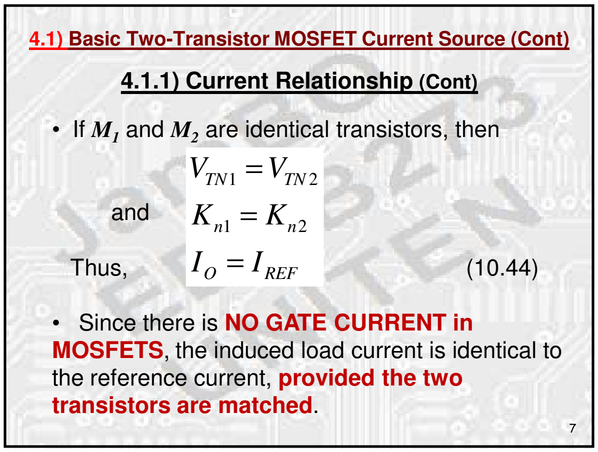
Therefore: $$V_{GS} = V_{TN1} + \sqrt{\frac{I_{REF}}{K_{n1}}} \quad (10.41)$$

- **M_2 is always be biased in saturation region.**

Thus

Load current is: $$I_O = K_{n2}(V_{GS} - V_{TN2})^2 \quad (10.42)$$

(10.43) → $$I_O = K_{n2}\left[\sqrt{\frac{I_{REF}}{K_{n1}}} + V_{TN1} - V_{TN2}\right]^2$$



4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.1) Current Relationship (Cont)

- If M_1 and M_2 are identical transistors, then

$$V_{TN1} = V_{TN2}$$

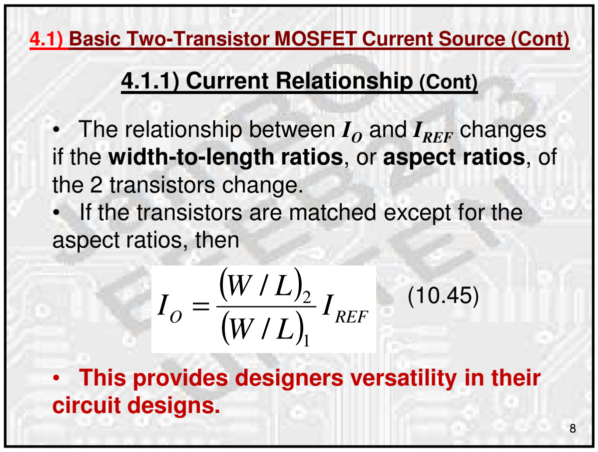
and

$$K_{n1} = K_{n2}$$

Thus,

$$I_O = I_{REF} \qquad (10.44)$$

- Since there is **NO GATE CURRENT in MOSFETS**, the induced load current is identical to the reference current, **provided the two transistors are matched**.



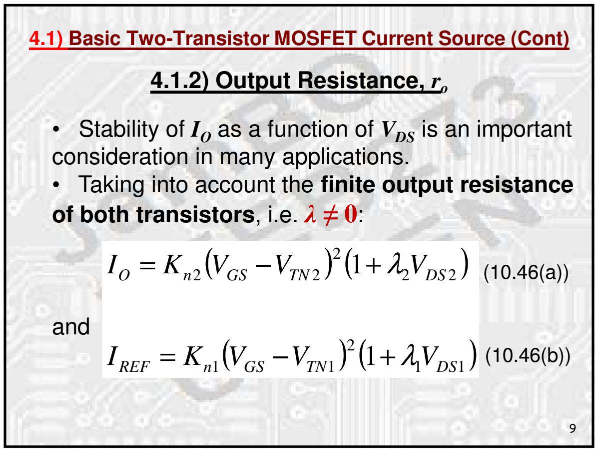
4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.1) Current Relationship (Cont)

- The relationship between I_O and I_{REF} changes if the **width-to-length ratios**, or **aspect ratios**, of the 2 transistors change.
- If the transistors are matched except for the aspect ratios, then

$$I_O = \frac{(W/L)_2}{(W/L)_1} I_{REF} \qquad (10.45)$$

- **This provides designers versatility in their circuit designs.**



4.1) Basic Two-Transistor MOSFET Current Source (Cont)

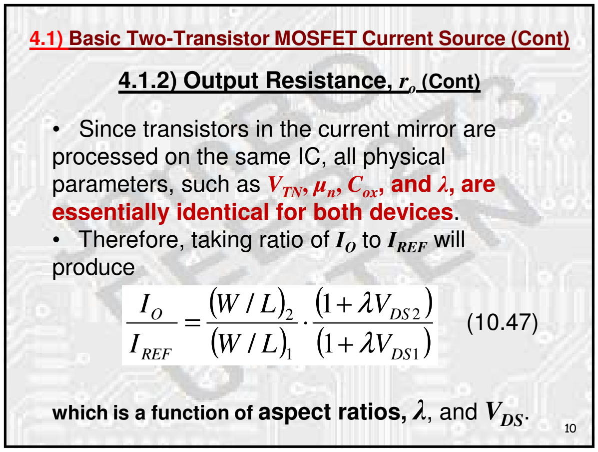
4.1.2) Output Resistance, r_o

- Stability of I_O as a function of V_{DS} is an important consideration in many applications.
- Taking into account the **finite output resistance of both transistors**, i.e. $\lambda \neq 0$:

$$I_O = K_{n2}(V_{GS} - V_{TN2})^2(1 + \lambda_2 V_{DS2}) \qquad (10.46(a))$$

and

$$I_{REF} = K_{n1}(V_{GS} - V_{TN1})^2(1 + \lambda_1 V_{DS1}) \qquad (10.46(b))$$



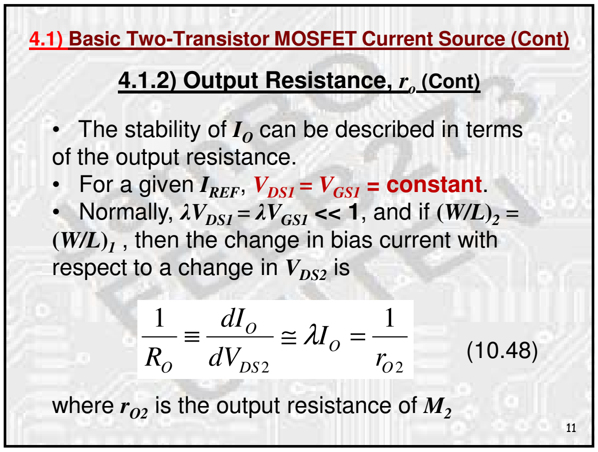
4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.2) Output Resistance, r_o (Cont)

- Since transistors in the current mirror are processed on the same IC, all physical parameters, such as **V_{TN}, μ_n, C_{ox}, and λ, are essentially identical for both devices**.
- Therefore, taking ratio of I_O to I_{REF} will produce

$$\frac{I_O}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})} \qquad (10.47)$$

which is a function of **aspect ratios**, λ, and V_{DS}.



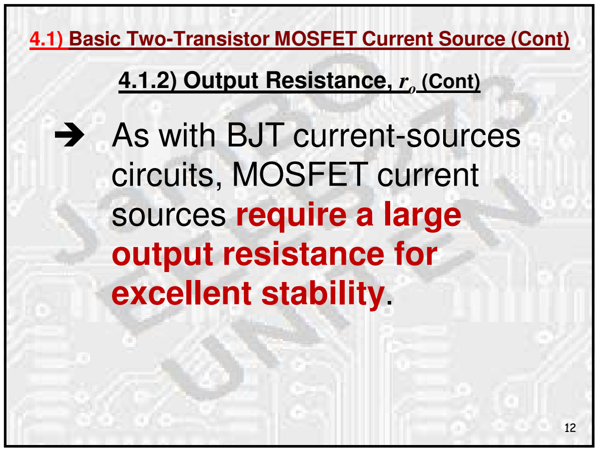
4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.2) Output Resistance, r_o (Cont)

- The stability of I_O can be described in terms of the output resistance.
- For a given I_{REF}, **$V_{DS1} = V_{GS1}$ = constant**.
- Normally, $\lambda V_{DS1} = \lambda V_{GS1} << 1$, and if $(W/L)_2 = (W/L)_1$, then the change in bias current with respect to a change in V_{DS2} is

$$\frac{1}{R_O} \equiv \frac{dI_O}{dV_{DS2}} \cong \lambda I_O = \frac{1}{r_{O2}} \qquad (10.48)$$

where r_{O2} is the output resistance of M_2



4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.2) Output Resistance, r_o (Cont)

➔ As with BJT current-sources circuits, MOSFET current sources **require a large output resistance for excellent stability**.

4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.3) Reference Current, I_{REF}

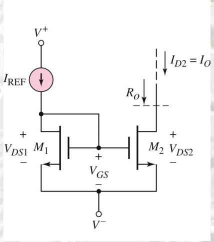


Fig 10.16: Basic two-transistor **N-MOSFET** current source

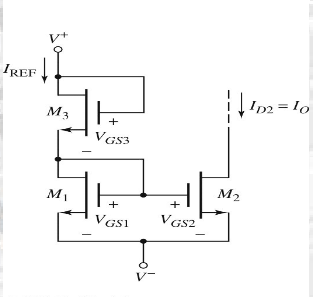
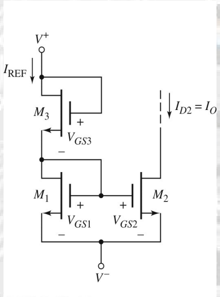


Fig 10.17: MOSFET current source.

4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.3) Reference Current, I_{REF} (Cont)



- In **BJT circuits**, the I_{REF} is generally established by the **bias voltages and a resistor**.
- **Since MOSFETs can be configured to act like a resistor**, the I_{REF} in MOSFET current mirrors is usually **established by using additional transistors, e.g.** M_3.

Fig 10.17: MOSFET current source.

4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.3) Reference Current, I_{REF} (Cont)

- Use current mirror in **Figure 10.17**
- Transistors M_1 and M_3 are in series. Assuming $\lambda = 0$:

$$I_{REF} = K_{n1}(V_{GS1} - V_{TN1})^2 = K_{n3}(V_{GS3} - V_{TN3})^2$$

- Assuming **V_{TN}, μ_n, and C_{ox} are identical** in all transistors, thus:

$$V_{GS1} = \sqrt{\frac{(W/L)_3}{(W/L)_1}} \cdot V_{GS3} + \left(1 - \sqrt{\frac{(W/L)_3}{(W/L)_1}}\right) \cdot V_{TN}$$

4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.3) Reference Current, I_{REF} (Cont)

- From the circuit, can be seen:

$$V_{GS1} + V_{GS3} = V^+ - V^-$$

- Therefore,

$$V_{GS1} = \frac{\sqrt{\frac{(W/L)_3}{(W/L)_1}}}{1 + \sqrt{\frac{(W/L)_3}{(W/L)_1}}} \cdot (V^+ - V^-) + \frac{\left(1 - \sqrt{\frac{(W/L)_3}{(W/L)_1}}\right)}{\left(1 + \sqrt{\frac{(W/L)_3}{(W/L)_1}}\right)} \cdot V_{TN} = V_{GS2}$$

4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.3) Reference Current, I_{REF} (Cont)

- Finally, the load current, for $\lambda = 0$, is given by

$$I_O = \left(\frac{W}{L}\right)_2 \left(\frac{1}{2}\mu_n C_{ox}\right)(V_{GS2} - V_{TN})^2$$

$$I_O = \frac{k_n'}{2} \cdot \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TN})^2 \qquad (10.53)$$

- Since the **designer has control over the width-to-length ratios of the transistors**, there is a **considerable flexibility** in the design of MOSFET current sources.

4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.3) Reference Current, I_{REF} (Cont)

Design Example 10.8

Objective: Design a MOSFET current source to meet a set of specifications.

Specifications: The circuit to be designed has the configuration shown in Figure 10.17.

The bias voltages are V^+ = +2.5 V, V^- = 0 V.

Transistors are available with parameters k'_n = 100 μA/V², V_{TN} = 0.4 V, and $\lambda = 0$.

Design the circuit such that I_{REF} = 100 μA, I_O = 60 μA, and V_{DS2}(sat) = 0.4 V.

4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.3) Reference Current, I_{REF} (Cont)

Design Example 10.8 (Cont)

Solution: With V_{DS2}(sat) = 0.4 = V_{GS2} – 0.4, then V_{GS2} = 0.4 + 0.4 = 0.8 V = V_{GS1}

Therefore,

$$\left(\frac{W}{L}\right)_2 = \frac{I_O}{\frac{k_n'}{2}(V_{GS2}-V_{TN})^2}$$

$$\therefore \left(\frac{W}{L}\right)_2 = \frac{60\mu}{\frac{100\mu}{2}(0.8-0.4)^2} = 7.5$$

4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.3) Reference Current, I_{REF} (Cont)

Design Example 10.8 (Cont)

The reference current is given by

$$I_{REF} = \frac{k_n'}{2}\cdot\left(\frac{W}{L}\right)_1 (V_{GS1}-V_{TN})^2$$

Since $V_{GS1} = V_{GS2}$ ➔

$$\left(\frac{W}{L}\right)_1 = \frac{I_{REF}}{\frac{k_n'}{2}(V_{GS2}-V_{TN})^2}$$

$$\therefore \left(\frac{W}{L}\right)_1 = \frac{100\mu}{\frac{100\mu}{2}(0.8-0.4)^2} = 12.5$$

4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.3) Reference Current, I_{REF} (Cont)

Design Example 10.8 (Cont)

The value of V_{GS3} is

$V_{GS3} = (V^+ - V^-) - V_{GS1}$ = 2.5 – 0.8 = 1.7 V

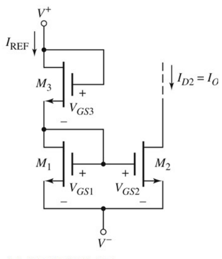
Since $I_{REF} = K_{n3}(V_{GS3} - V_{TN})^2$, therefore

$$\left(\frac{W}{L}\right)_3 = \frac{I_{REF}}{\frac{k_n'}{2}(V_{GS3}-V_{TN})^2}$$

$$\therefore \left(\frac{W}{L}\right)_3 = \frac{100\mu}{\frac{100\mu}{2}(1.7-0.4)^2} = 1.18$$

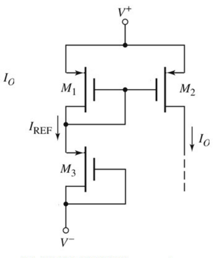
4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.4) Using N-MOSFET and P-MOSFET



(a) 2T N-MOSFET current source

Figure 10.17



(b) 2T P-MOSFET current source

Figure P10.52

4.2) Multi-MOSFET Current-Source Circuits

- Among multi-MOSFET current-source circuits are:

❑ **Cascode Current Mirror**

❑ **Wilson Current Mirror**

❑ **Wide-Swing Current Mirror**

4.2.1) Cascode Current Mirror

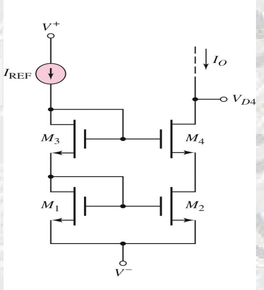


Fig 10.18: MOSFET cascode current mirror.

- As in **Figure 10.18, with increased output resistance R_O**
- I_{REF} is established using another transistor.
- When all transistors are matched:

$$I_O = I_{REF}$$

4.2.1) Cascode Current Mirror (Cont)

- To determine output resistance at the drain of M_4, use the small-signal equivalent circuit.

- I_{REF} constant → **gate voltages** to M_1 and M_3, and hence M_2 and M_4, **are constant**

  →Equivalent to an **ac short circuit**.
- Therefore, the **ac equivalent circuit** for calculating the output resistance is shown in **Figure 10.19(a)**. The **small signal equivalent circuit** is given in **Figure 10.19(b)**.

- **The small-signal resistance looking into the drain of M_2 is r_{O2}.**

4.2.1) Cascode Current Mirror (Cont)

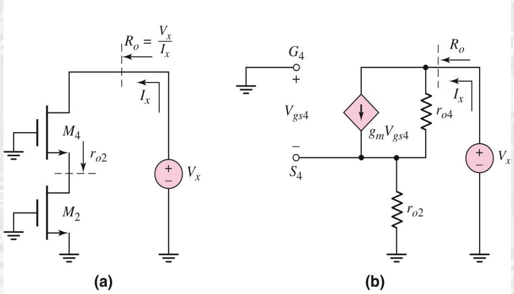
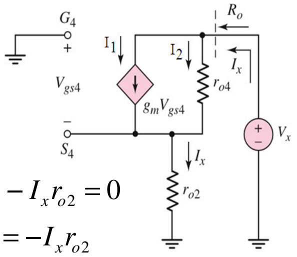


Fig 10.19: Equivalent circuits of the MOSFET cascode current mirror for determining R_O

4.2.1) Cascode Current Mirror (Cont)

$$I_x = I_1 + I_2 \Rightarrow I_x = g_m V_{gs4} + \frac{V_x - (-V_{gs4})}{r_{o4}}$$



$$0 - V_{gs4} - I_x r_{o2} = 0$$

$$\Rightarrow V_{gs4} = -I_x r_{o2}$$

4.2.1) Cascode Current Mirror (Cont)

- From Figure 10.19(b), summing currents at output node yields

$$I_x = g_m V_{gs4} + \frac{V_x - (-V_{gs4})}{r_{o4}}$$

Also

$$V_{gs4} = -I_x r_{o2}$$

Therefore

$$I_x + \frac{r_{o2}}{r_{o4}} I_x + g_m r_{o2} I_x = \frac{V_x}{r_{o4}}$$

Finally

$$R_O = \frac{V_x}{I_x} = r_{o4} + r_{o2}(1 + g_m r_{o4}) \quad (10.57)$$

4.2.1) Cascode Current Mirror (Cont)

- Normally $g_m r_{o4} >> 1 \Rightarrow g_m r_{o4} r_{o2} >> r_{o4}$

Thus $R_O \cong g_m r_{o4} r_{o2}$

- This implies that the **output resistance of this cascode configuration is much larger** than that of the basic two-transistor current source.

→ Since ***dI_O is proportional to $1/R_O$***, the load current in the cascode circuit is more stable against variations in output voltage.

4.2.1) Cascode Current Mirror (Cont)

Example 10.9

Objective: Compare the output resistance of the cascode **MOSFET** current mirror (CMCM) to that of the two-transistor MOSFET current mirror (2TMCM).

Consider the 2TMCM in Figure 10.17 and the CMCM in Figure 10.18.

Assume that $I_{REF} = I_O = 100$ µA in both circuits, $\lambda = 0.01$ V^{-1} for all transistors, and $g_m = 0.5$ mA/V.

4.2.1) Cascode Current Mirror (Cont)

Example 10.9 (Cont)

Solution: The output resistance of 2TMCM is, from Equation (10.48),

$$r_O = 1/(\lambda I_{REF}) = 1/[(0.01)(100\mu)] = \mathbf{1}\ \text{M}\Omega$$

For the CMCM circuit,

$$r_{O2} = r_{O4} = 1/(\lambda I_O) = 1/[(0.01)(100\mu)] = \mathbf{1}\ \text{M}\Omega$$

Therefore, R_O of the CMCM circuit is, from Equation (10.57),

$$R_O = r_{O4} + r_{O2}(1 + g_m r_{O4})$$
$$= 1\text{M} + (1\text{M})[1 + (0.5\text{m})(1\text{M})] = \mathbf{502}\ \text{M}\Omega$$

4.2.2) Wilson Current Mirror

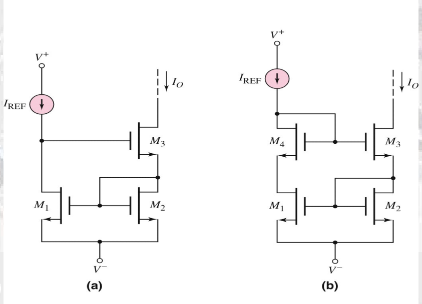


Fig 10.20: (a) MOSFET Wilson current mirror, (b) Modified MOSFET Wilson CM.

4.2.2) Wilson Current Mirror (Cont)

- **Fig 10.20(a)** is MOSFET Wilson current mirror.
- Note: $V_{DS1} = V_{GS2} + V_{GS3}$
  $V_{DS2} = V_{GS2}$
  ➔ $V_{DS1} \neq V_{DS2}$
- Since: $\lambda \neq 0$
  ➔ I_O / I_{REF} is slightly different from the aspect ratios
- This problem is solved in the **modified Wilson current mirror**, shown in **Figure 10.20(b).**

4.2.2) Wilson Current Mirror (Cont)

- In modified MOSFET Wilson current mirror:
  ➔ Add transistor M_4
- For a constant I_{REF}, V_{DS} of M_1, M_2 and M_4 are held constant
  ➔ V_{DS} of M_1 and M_2 are equal ($V_{DS1} = V_{DS2}$)
- Primary advantage of both Wilson current mirrors: **INCREASE in output resistance R_O**,
  ➔ i.e. further stabilizes the load current I_O.
- Output resistance of Wilson current mirror:

$$R_O \cong g_m r_{o3} r_{o2}$$

4.2.3) Wide-Swing Current Mirror

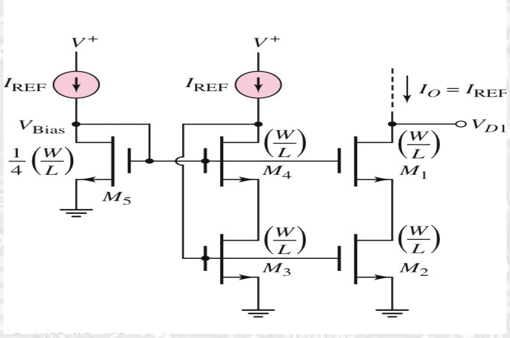
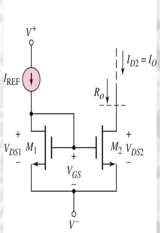


Fig 10.21: A wide-swing MOSFET cascode current mirror.

4.2.3) Wide-Swing Current Mirror (Cont)

4.2.3.1) Minimum output voltage swing, V_O(min)

a) Simple two-transistor CM



- The minimum output voltage for the **simple two-transistor** current mirror is

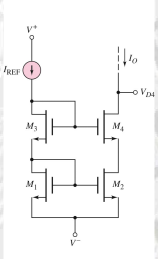
$$V_O(\min) = V^- + V_{DS2}(\text{sat})$$

- If V_{GS} = 0.75V and V_{TN} = 0.50V then $V_O(\min)$ is only 0.25V above V^- i.e. $V_{DS2}(\text{sat}) = V_{GS} - V_{TN}$ = 0.25V.

4.2.3) Wide-Swing Current Mirror (Cont)

4.2.3.1) Minimum output voltage swing, V_O(min)

b) MOSFET cascode CM



- The gate voltage of M_4 is

$$V_{G4} = V^- + V_{GS1} + V_{GS3}$$

- The minimum V_{D4} is then

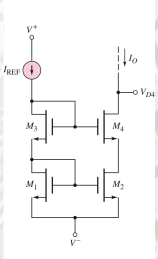
$$V_{D4}(\min) = V_{S4} + V_{DS4}(\text{sat})$$

$$V_{D4}(\min) = V_{G4} - V_{GS4} + V_{DS4}(\text{sat})$$

4.2.3) Wide-Swing Current Mirror (Cont)

4.2.3.1) Minimum output voltage swing, V_O(min)

b) MOSFET cascode CM (Cont)



- Assuming matched transistors,

$$V_{GS1} = V_{GS2} = V_{GS4} \equiv V_{GS}$$

- Then

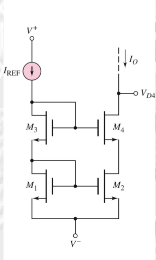
$$V_{D4}(\min) = V^- + (V_{GS} + V_{DS4}(\text{sat}))$$

- If V_{GS} = 0.75V and V_{TN} = 0.50V then V_{D4}(min) = 1.0V above V^-

4.2.3) Wide-Swing Current Mirror (Cont)

4.2.3.1) Minimum output voltage swing, V_O(min)

b) MOSFET cascode CM (Cont)



- Increase in V_O(min) means **reduced** maximum output voltage swing of the load circuit, which is critical in low-power applications.

➔ Although R_O of cascode is higher, output swing is smaller.

***** Wide-swing cascode current-mirror produces *increased Ro* and *increased output voltage swing.***

4.2.3) Wide-Swing Current Mirror (Cont)

4.2.3.2) V_O(min) of Wide-swing cascode CM

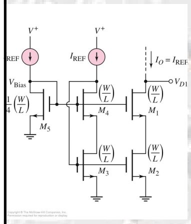


Figure 10.21: WSCCM

- **WSCCM** does not limit output voltage swing like cascode circuit.
- **WSCCM** maintains high R_O.
- All transistors are identical except for the different width-to-length ratios (as shown in **Figure 10.21**).
- M_3 and M_4 together act like a single diode connected-transistor to create V_{G3}.
- With M_4, V_{DS3} is matched to V_{DS2}.

4.2.3) Wide-Swing Current Mirror (Cont)

4.2.3.2) V_O(min) of Wide-swing cascode CM (Cont)

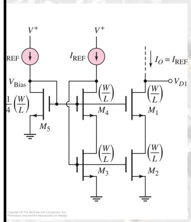


Figure 10.21: WSCCM

- Since M_5 is ¼ the size of M_1 ~ M_4 and since all drain currents are equal, then

$$(V_{GS5} - V_{TN}) = 2(V_{GSi} - V_{TN})$$

where V_{GSi} corresponds to gate-to-source voltage of M_1 ~ M_4

- The voltage at the gate of M_1 is

$$V_{G1} = V_{GS5} = (V_{GS5} - V_{TN}) + V_{TN}$$

4.2.3) Wide-Swing Current Mirror (Cont)

4.2.3.2) V_O(min) of Wide-swing cascode CM (Cont)

- The minimum V_O at the drain of M_1 is

$$V_{D1}(\min) = V_{G1} - V_{GS1} + V_{DS1}(\text{sat})$$

$$V_{D1}(\min) = \left[(V_{GS5} - V_{TN}) + V_{TN}\right] - V_{GS1} + (V_{GS1} - V_{TN})$$

or

$$V_{D1}(\min) = V_{GS5} - V_{TN} = 2(V_{GSi} - V_{TN}) = 2V_{DSi}(\text{sat})$$

- If V_{GSi} = 0.75V and V_{TN} = 0.50V, then V_{D1}(min) = 0.50V, ➔ ½ of cascode circuit.

4.2.3) Wide-Swing Current Mirror (Cont)

4.2.3.3) Summary of V_O(min)

- For V_{GSi} = 0.75V and V_{TN} = 0.50V:

2TMCM ➔ V_O(min) = 0.25V above V^-

CMCM ➔ V_O(min) = 1.00V above V^-

WSCCM ➔ V_O(min) = 0.50V above V^-

4.3) Bias-Independent Current-Source

- Previous current sources:
  - ❑ I_{REF} is dependent on supply voltages.
  - ❑ So, I_O depends on supply voltages, which is undesirable in most cases.

- Circuit design in which the **load current is essentially independent of the bias** is shown in **Figure 10.22**, with width-to-length ratios given.

4.3) Bias-Independent Current-Source (Cont)

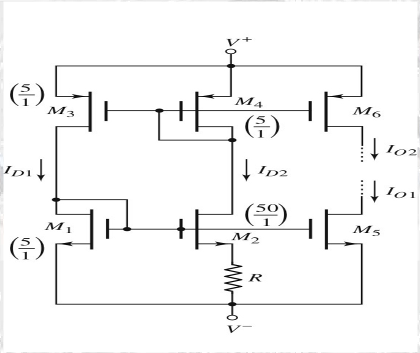


Figure 10.22: Bias-independent MOSFET current mirror.

4.3) Bias-Independent Current-Source (Cont)

- Since **PMOS devices** are matched, $I_{D1} = I_{D2}$

For M_1:

$$I_{D1} = \frac{k_n'}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TN})^2$$

For M_2:

$$I_{D2} = \frac{k_n'}{2}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TN})^2$$

KVL for M_1, M_2 and R →

$$V_{GS2} = V_{GS1} - I_{D2}R$$

Solving for R:

$$R = \frac{1}{\sqrt{k_{n1} I_{D1}}}\left(1 - \sqrt{\frac{(W/L)_1}{(W/L)_2}}\right)$$

4.3) Bias-Independent Current-Source (Cont)

- Value of R establishes $I_{D1} = I_{D2}$
- I_{D1} and I_{D2} then establishes V_{GS1} and V_{SG3}
- V_{GS1} and V_{SG3}, in turn, can be applied to M_5 and M_6 to establish load currents I_{O1} and I_{O2}

- I_{D1} and I_{D2} are independent of supply voltages V^+ and V^- as long as M_2 and M_3 are biased in the saturation region.

- As the difference, $V^+ - V^-$, increases, the values of V_{DS2} and V_{SD3} increase but the **currents remain essentially constant**.

4.4) MOSFET Active Load Circuit

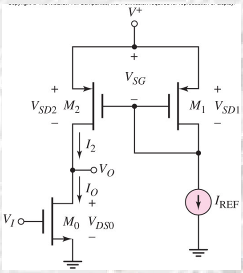


Figure 10.33: Simple MOSFET amplifier with active load, showing currents and voltages.

- M_1 and M_2 form a PMOS **active load** circuit.

- M_2 is the **active load device** for driver transistor M_0.

- Consider the voltage transfer function of V_O versus V_I for this circuit.

4.4.1) DC Analysis: MOSFET Active Load Circuit

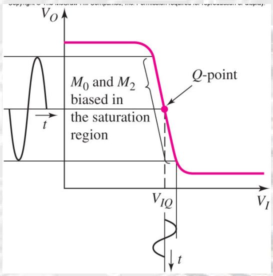


Fig 10.34: Voltage transfer characteristics of MOSFET circuit with active load.

- Establish Q-point in the region where M_0 and M_2 are biased in the saturation region mode.

⇒ Only small range of input voltage is available.

- Q-point corresponds to $V_I = V_{IQ}$

4.4.1) DC Analysis: MOSFET Active Load Circuit (Cont)

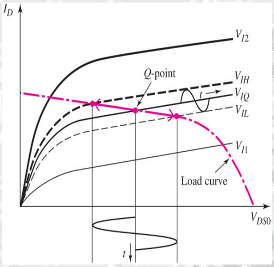


Fig 10.35: Driver transistor characteristics and load curve for MOSFET circuit with active load.

- As input changes between V_{IH} and V_{IL} ⇒ the Q-point moves up and down load curve producing a change in output voltage.
- When $V_I = V_{I2}$ ⇒ M_0 is driven into non-saturation region.
- When $V_I = V_{I1}$ ⇒ Q_2 is driven into non-saturation region.

Larger circuits

4.1) Basic Two-Transistor MOSFET Current Source

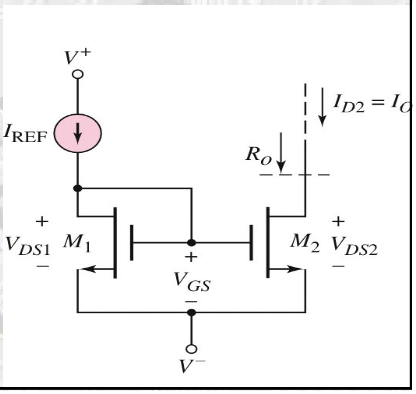


Fig 10.16: Basic two-transistor NMOS MOSFET current source.

4.1) Basic Two-Transistor MOSFET Current Source (Cont)

4.1.3) Reference Current, I_{REF}

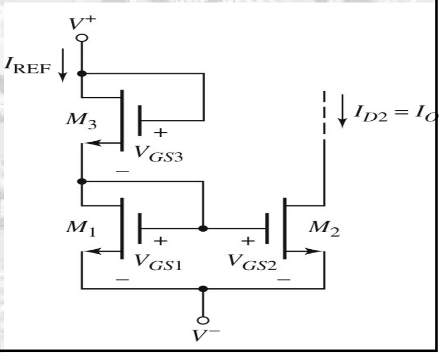


Fig 10.17: MOSFET current source.

4.2.1) Cascode Current Mirror

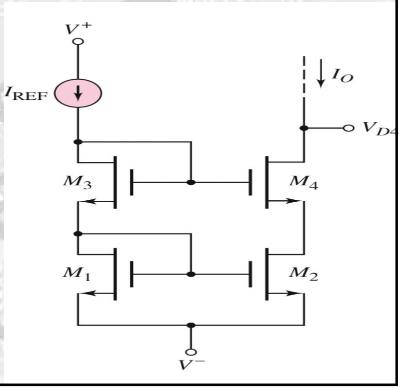
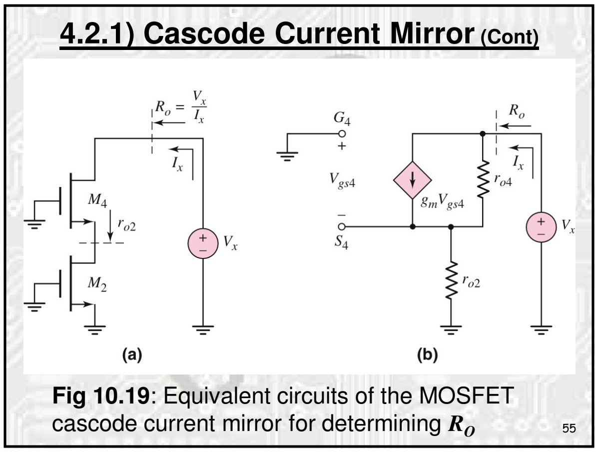
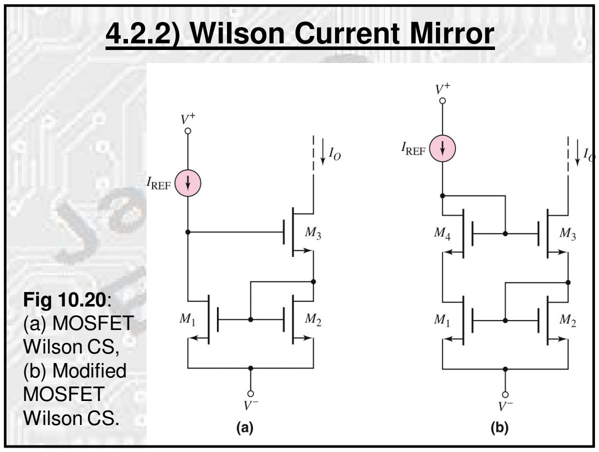


Fig 10.18: MOSFET cascode current mirror.



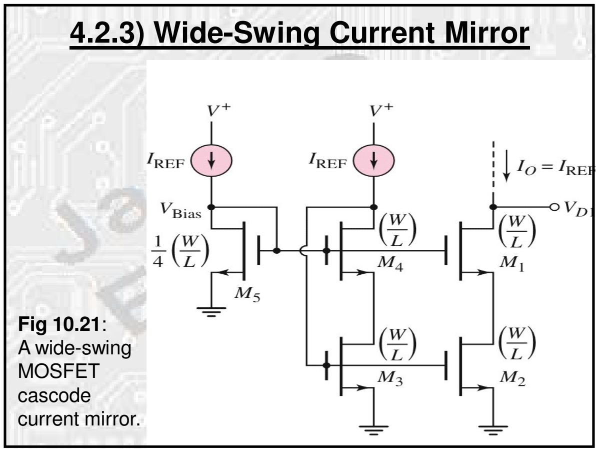
4.2.1) Cascode Current Mirror (Cont)

Fig 10.19: Equivalent circuits of the MOSFET cascode current mirror for determining R_O



4.2.2) Wilson Current Mirror

Fig 10.20:
(a) MOSFET Wilson CS,
(b) Modified MOSFET Wilson CS.



4.2.3) Wide-Swing Current Mirror

Fig 10.21: A wide-swing MOSFET cascode current mirror.