(10) Simplified BJT Op-Amp Circuit

Reference: Neamen, Chapter 11

Learning Outcome

Able to:

- Analyze a simplified BJT Op-amp circuit.

10.1) Simplified BJT Op-Amp Circuit

- **Figure 11.49** depicts a simple bipolar op-amp.

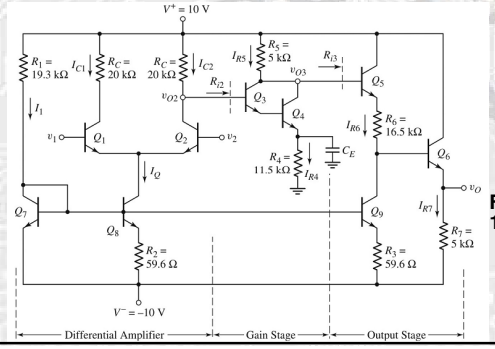

Figure 11.49

10.1) Simplified BJT Op-Amp Circuit (Cont)

- Simplified analysis and design ➔ only **resistive loads** are considered.
- Diff-amp is biased with **Widlar current source**.
- One-sided output of diff-amp is connected to **Darlington pair gain stage**.
- Bypass capacitor C_E is included to increase small-signal voltage gain.
- Output stage is an **emitter follower**.

- Generally, wanted the dc value of the output voltage v_O **= 0** when input voltage = 0 ➔ insert dc level shifting circuit between v_{O3} and v_O.

10.2) DC Characteristics

Example 11.15

Analyze the dc characteristics of BJT op-amp circuit. Neglect base currents. Assume V_{BE}**(on) =** 0.7V for all transistors except Q_8 and Q_9 in Widlar.

- Reference current I_1: $I_1 = \dfrac{10-0.7-(-10)}{19.3} = 1\text{mA}$
- Bias current I_Q (**from Widlar**):

$$I_Q R_2 = V_T \ln\left(\frac{I_1}{I_Q}\right) \quad \Rightarrow I_Q = 0.4\text{ mA}$$

- Collector currents:

$I_{C1} = I_{C2} = I_Q / 2 =$ **0.2 mA**

10. 2) DC Characteristics (Cont)

- DC voltage at collector Q_2

$V_{O2} = 10 - I_{C2} R_C = 10 - (0.2\text{m})(20\text{k})$

⇨ $V_{O2} = 6\text{V} = v_{cm}$**(max)**

- Common-mode input range: -8.6V ≤ v_{cm} ≤ 6V

v_{cm}**(min) =** -10 + V_{BE8} + V_{BE1} (ignoring $I_Q R_2$)

- Values for I_{R4} and I_{R5}:

$$I_{R4} = \frac{V_{O2} - 2V_{BE}(\text{on})}{R_4} = \frac{6-1.4}{11.5\text{k}} = 0.4\text{mA}$$

$I_{R5} \approx I_{R4} =$ **0.4 mA (neglecting base currents)**

10. 2) DC Characteristics (Cont)

• DC voltage at collectors of Q_3 and Q_4

$V_{O3} = 10 - I_{R5}R_5 = 10 - (0.4\text{m})(5\text{k})$

⇨ V_{O3} = 8V is midway between 10V supply voltage and 6V dc input voltage (V_{O2}) → This allows a maximum symmetrical swing for time-varying v_{O3}

• DC voltage level shifting by Q_5 and R_6:

$I_{R6} = I_Q$ = 0.4 mA, since $R_3 = R_2$

$V_{B6} = V_{O3} - V_{BE}(\text{on}) - I_{R6}R_6 = 8 - 0.7 - (0.4\text{m})(16.5\text{k})$

⇨ V_{B6} = 0.7 V produces **a zero dc output at v_O** (emitter of Q_6) for a zero diff-mode input voltage.

• Current I_{R7}: $I_{R7} = \dfrac{v_O - (-10)}{R_7} = \dfrac{10}{5\text{k}} = 2\text{mA}$

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10. 3) AC Characteristics

Example 11.16

Determine small-signal diff-mode voltage gain, A_d

Use **Fig 11.49**. Transistor parameters: $\beta = 100$, $V_A = \infty$.

• Overall differential-mode gain:

$$A_d = A_{d1}.A_2.A_3 = \left(\frac{v_{o2}}{v_1 - v_2}\right)\left(\frac{v_{o3}}{v_{o2}}\right)\left(\frac{v_o}{v_{o3}}\right)$$

A_d valid only if **load resistance of following stages are considered** in the calculation:

→ R_{i2}: input resistance to Darlington pair.

→ R_{i3}: input resistance to output stage.

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10. 3) AC Characteristics (Cont)

• **One-sided diff-mode** voltage gain of diff-amp:

$$A_{d1} = \left(\frac{V_{o2}}{v_d}\right) = \frac{g_m}{2}\left(R_C \| R_{i2}\right)$$

$$r_{\pi 4} = \beta V_T / I_{R4} = (100)(0.026)/0.4\text{m} = 6.5\text{k}\Omega$$

$$r_{\pi 3} \cong \beta^2 V_T / I_{R4} = (100)^2(0.026)/0.4\text{m} = 650\text{k}\Omega$$

$$R_{i2} = r_{\pi 3} + (1+\beta)r_{\pi 4} = 650\text{k} + (101)(6.5\text{k}) = 1307\text{k}\Omega$$

$$g_m = I_Q/(2V_T) = 0.4\text{m}/(2\times 0.026) = 7.70\text{mA/V}$$

$$\therefore A_{d1} = (7.70\text{m}/2)(20\text{k} \| 1307\text{k}) = 75.8$$

→ Since load resistance $R_{i2} >> R_C$, there is no significant loading effect of 2nd stage on diff-amp.

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10. 3) AC Characteristics (Cont)

• **The voltage gain** of the Darlington pair:

$$A_2 = \frac{I_{R4}}{2V_T}\left(R_5 \| R_{i3}\right)$$

$$r_{\pi 5} = \beta V_T / I_{R6} = (100)(0.026)/0.4\text{m} = 6.5\text{k}\Omega$$

$$r_{\pi 6} = \beta V_T / I_{R7} = (100)(0.026)/2\text{m} = 1.3\text{k}\Omega$$

$$R_{i3} = r_{\pi 5} + (1+\beta)\left[R_6 + r_{\pi 6} + (1+\beta)R_7\right] = 52.8\text{M}\Omega$$

Since $R_{i3} >> R_5$, the output stage does not load down the gain stage, and small-signal voltage gain is approximately

$$\therefore A_2 \cong \frac{I_{R4}}{2V_T}(R_5) = \frac{0.4\text{m}}{2(0.026)}(5\text{k}) = 38.5$$

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10. 3) AC Characteristics (Cont)

• The combination of Q_5 **and** Q_6 forms an emitter follower, and the gain of the output stage is:

$$A_3 = v_o / v_{o3} \cong 1$$

• The overall small-signal voltage gain is therefore:

$$A_d = A_{d1}.A_2.A_3 = 75.8 \times 38.5 \times 1 = 2918$$

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Larger circuits

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10.1) Simplified BJT Op-Amp Circuit

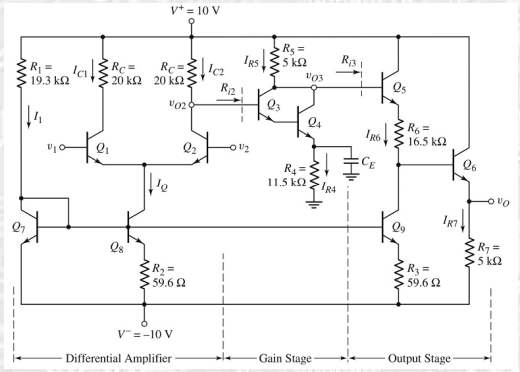

Figure 11.49: A simple bipolar op-amp.

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