(11)
Op-Amp Circuits: Bipolar Op-Amp

Reference: Neamen, Chapter 13

Learning Outcome

Able to:

- Describe and analyze the dc and ac characteristics of the classic 741 bipolar op-amp circuit.

11.0) 741 Op-Amp

- The 741 op-amp has been produced **since 1966** by many semiconductor device manufacturers.
- The 741 is still a **widely used general-purpose op-amp** although there have been many advances in op-amp design.
- Even though the 741 is a **fairly old design**, it still **provides a useful case study to describe the general circuit configuration** and to perform a detailed dc and small-signal analysis. From the ac analysis, usually **voltage gain and frequency response** of the circuit are determined.

11.1) Circuit Description

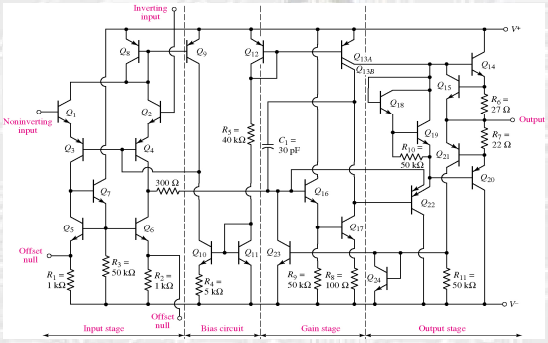
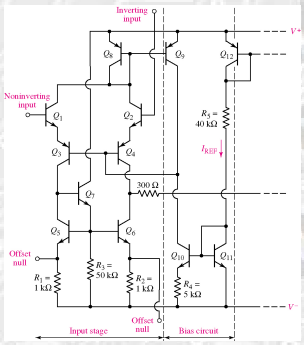


Figure 13.3: Equivalent circuit, 741 op-amp.

11.1) Circuit Description (Cont)

- The 741 consists of **input differential amplifier stage, gain stage, output stage and separate bias circuit** (which establishes the bias currents throughout the op-amp).
- Like most op-amp, the 741 is **biased with both positive and negative supply voltages**. This eliminates the need for input coupling capacitors, which in turn means that the circuit is also a dc amp.
- The dc output voltage is zero when the applied differential input signal is zero.
- Typical supply voltages are V^+=15V and V^- = -15V, although input voltages as low as 5V can be used.

11.1.1) Input Diff-Amp and Biasing



- Input stage: Q_1 to Q_7
- Biasing: Q_8 to Q_{12}
- Input transistors Q_1 and Q_2: act as emitter follower → high R_{id}
- Q_3 and Q_4: common-base amplifier (**large voltage gain**), with input currents from Q_1 and Q_2

Figure 13.5: Bias circuit and input stage of 741 op-amp.

11.1.1) Input Diff-Amp and Biasing (Cont)

• Q_5, Q_6 and Q_7 with R_1, R_2 and R_3: form **active load.**

• **Output (single-sided)** at collector of Q_4 and Q_6

• The dc output voltage at collector Q_6 is at lower potential than inputs at bases of Q_1 & Q_2. As signal passes through the op-amp, dc voltage level shifts several times. By design, when the signal reaches output terminal, **dc voltage should be zero if a zero diff input** signal is applied. **Two null terminals** on input stage are used to make appropriate adjustments to accomplish this design goal.

7

11.1.1) Input Diff-Amp and Biasing (Cont)

• Q_{12}, Q_{11} & R_5: dc current biasing → provides I_{REF}

• Q_{10}, Q_{11} & R_4: Widlar current source for common-base transistors (Q_3 & Q_4) and current mirror formed by Q_8 & Q_9.

• Q_3 & Q_4: are **lateral pnp device**, which refers to fabrication process and geometry of the transistors → **provide added protection against voltage breakdown**, although the current gain is smaller than in npn devices.

8

11.1.1) Input Diff-Amp and Biasing (Cont)

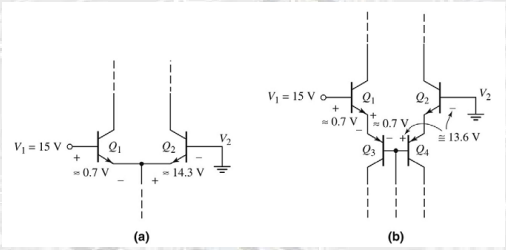


Figure 13.4: (a) Basic common-emitter diff-pair with a large differential voltage and (b) 741 input stage, with a large differential voltage.

9

11.1.1) Input Diff-Amp and Biasing (Cont)

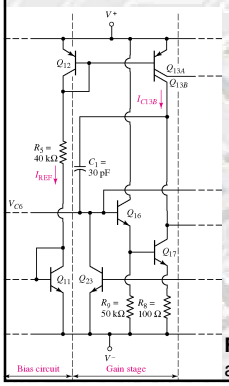
• For **Figure 13.4**: V_1 = 15 V, V_2 = 0 V.

❑ **Figure (a)**: Basic common-emitter diff-pair
- B-E of Q_2 is **reverse biased** by approx **14.3 V**
- Since an npn B-E junction has **breakdown voltage of 3 to 6 V** → Q_2 would probably enter breakdown and permanently damaged.

❑ **Figure (b)**: B-E of Q_1 & Q_3 are forward biased
- Series combination of B-E junction of Q_2 & Q_4 is **reverse biased** by approx **13.6 V**
- The **breakdown voltage** of lateral pnp is typically **on order of 50 V** → B-E of Q_4 provides breakdown protection for input diff-amp stage.

10

11.1.2) Gain Stage



• Q_{16} & Q_{17}: second (gain) stage.

• Q_{16}: emitter follower → large R_{in}

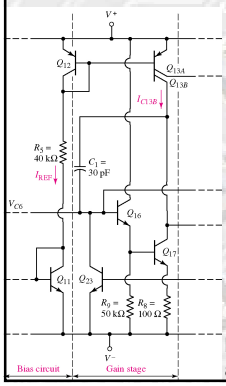
• Q_{13}: two transistors in parallel
→ Q_{13A}: ¼ area of Q_{12}
→ Q_{13B}: ¾ area of Q_{12}

• Q_{13B}: provides bias current for Q_{17}, and is also the **active load for high voltage gain**.

Figure 13.7: Reference circuit and gain stage of 741 op-amp.

11

11.1.2) Gain Stage (Cont)



• Q_{17}: common-emitter → voltage at collector of Q_{17} is input signal to output stage → signal undergoes another dc level shift in this gain stage.

• Capacitor C_1: internal **feedback compensation** (**Miller compensation**) **for stability** → connected between the output and input terminals of the gain stage.

Figure 13.7: Reference circuit and gain stage of 741 op-amp.

12

11.1.3) Output Stage

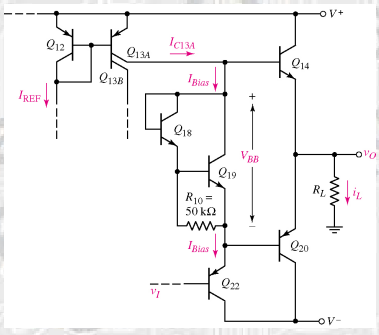


Figure 13.8: Basic output stage of 741 op-amp, showing currents and voltages.

11.1.3) Output Stage (Cont)

- Q_{14} & Q_{20}: **class-AB circuit** of complementary emitter-follower → to provide **low output resistance** and current gain (for driving large load currents).
- Output of gain stage is connected to the base of Q_{22} → emitter follower, **high input resistance**.
- Q_{13A}: provides a **bias current** for Q_{22}, Q_{18} & Q_{19}
- Q_{18} & Q_{19}: to establish a **quiescent bias current** in output transistors Q_{14} & Q_{20}.
- Q_{15} & Q_{21}: are **short-circuit protection devices** → normally off. Conducting only **when output is inadvertently connected to ground**, resulting in a very large output current.

11.1.4) Abbreviated Data Sheet

Table 13.1: Data for 741 at T = 300 °K and supply voltage of 15V

Parameters	Minimum	Typical	Maximum	Units
Input bias current		80	500	nA
Diff-mode input resistance	0.3	2.0		MΩ
Input capacitance		1.4		pF
Output short-circuit current		25		mA
Open-loop gain ($R_L \geq 2k\Omega$)	50,000	200,000		V/V
Output resistance		75		Ω
Unity-gain frequency		1		MHz

11.2) DC Analysis

- Purpose:
  - ❑ To determine dc bias currents.
- Assumptions:
  - ❑ Both non-inverting and inverting input terminals are at ground potentials.
  - ❑ dc supply voltages are V^+=15V and V^- = -15V.
- Approximations:
  - ❑ Assume V_{BE} for npn = V_{EB} for pnp = 0.6V.
  - ❑ In most cases dc **base currents are neglected**.

11.2) DC Analysis (Cont)

Steps in DC Analysis:

- Identify the bias portion of op-amp circuit.
- Determine the reference current.
- Determine the bias currents in the individual building blocks of the overall circuit.

11.2.1) Bias Circuit and Input Stage

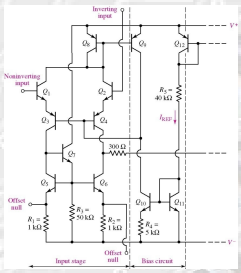


Figure 13.5: Bias circuit and input stage of 741 op-amp.

- The reference current established by Q_{12}, Q_{11} & R_5:

$$I_{REF} = \frac{V^+ - V_{EB12} - V_{BE11} - V^-}{R_5} \quad (13.1)$$

- Current I_{C10} from Widlar current source (Q_{11}, Q_{10} & R_4):

$$I_{C10} R_4 = V_T \ln(I_{REF} / I_{C10}) \quad (13.2)$$

11.2.1) Bias Circuit and Input Stage (Cont)

• **Neglecting base currents** → $I_{C8} = I_{C9} = I_{C10}$
Then, quiescent collector currents in Q_1 through Q_4:

$$I_{C1} = I_{C2} = I_{C3} = I_{C4} = I_{C10}/2 \qquad (13.3)$$

• Assuming dc currents in the input stage are exactly balanced, dc voltage at collector of Q_6 = input to the second stage = dc voltage at collector of Q_5 (or V_{C5})

$$V_{C6} = V_{C5} = V_{BE7} + V_{BE6} + I_{C6}R_2 + V^- \qquad (13.4)$$

→ The dc level shifts through the op-amp.

11.2.1) Bias Circuit and Input Stage (Cont)

Example 13.1

Objective: Calculate dc bias currents in the bias circuit and input stage of the 741 op-amp.

The bias circuit and input stage are shown in Figure 13.5.

11.2.1) Bias Circuit and Input Stage (Cont)

Example 13.1 (Cont)

Solution: From Equation (13.1), the reference current is

$$I_{REF} = \frac{V^+ - V_{EB12} - V_{BE11} - V^-}{R_5}$$

$$\Rightarrow I_{REF} = \frac{15 - 0.6 - 0.6 - (-15)}{40\text{k}} = 0.72\text{mA}$$

11.2.1) Bias Circuit and Input Stage (Cont)

Example 13.1 (Cont)

Current I_{C10} is found from Equation (13.2), as follows:

$$I_{C10}R_4 = V_T \ln(I_{REF}/I_{C10})$$

$$\Rightarrow I_{C10}(5\text{k}) = (0.026)\ln(0.72\text{m}/I_{C10})$$

By trial and error, can find I_{C10} **= 19 µA**

The bias currents in the input stage are then

$I_{C1} = I_{C2} = I_{C3} = I_{C4} = I_{C10}/2 =$ **9.5 µA**

11.2.1) Bias Circuit and Input Stage (Cont)

Example 13.1 (Cont)

From Equation (13.4), the voltage at the collector of Q_6 is

$$V_{C6} = V_{BE7} + V_{BE6} + I_{C6}R_2 + V^-$$

→ $V_{C6} = 0.6 + 0.6 + (9.5\mu)(1\text{k}) + (-15)$

or $V_{C6} \approx -13.8$ V

11.2.1) Bias Circuit and Input Stage (Cont)

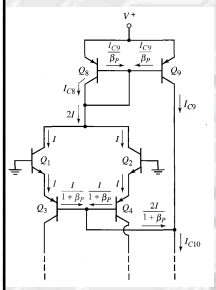


Figure 13.6: Expanded input stage, 741 op-amp, showing base currents.

Effect of the base currents

• β of Q_3, Q_4, Q_8 & Q_9 (pnp) may be **small**, hence **not negligible**. Still assume β of npn negligible.

• I_{C10} establishes base currents in Q_3 & Q_4 → which then establish emitter currents I. At collector of Q_8:

$$2I = I_{C8} + \frac{2I_{C9}}{\beta_p} = I_{C9}\left(1 + \frac{2}{\beta_p}\right)$$

11.2.1) Bias Circuit and Input Stage (Cont)

Effect of the base currents (Cont)

• Since Q_8 and Q_9 are matched: ➔ $I_{C8} = I_{C9}$. Then,

$$I_{C10} = \frac{2I}{1+\beta_p} + I_{C9} = \frac{2I}{1+\beta_p} + \frac{2I}{\left(1+\frac{2}{\beta_p}\right)}$$

$$\Rightarrow I_{C10} = 2I\left[\frac{\beta_p^2+2\beta_p+2}{\beta_p^2+3\beta_p+2}\right] \qquad (13.6)$$

25

11.2.1) Bias Circuit and Input Stage (Cont)

Effect of the base currents (Cont)

• With approximation $\left[\frac{\beta_p^2+2\beta_p+2}{\beta_p^2+3\beta_p+2}\right] \cong 1$

$$\Rightarrow I_{C10} = 2I$$

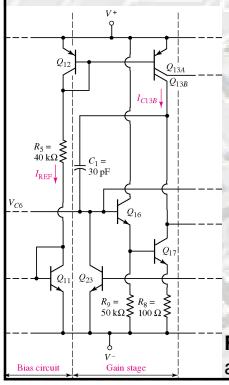
➔**Even if base currents in pnp are not negligible, bias current in Q_1 and Q_2 are very nearly**

$$I = I_{C10}/2 \qquad (13.7)$$

Bias current is essentially the same as originally assumed in Equation (13.3).

26

11.2.2) Gain Stage



• Q_{12} & Q_{13} form the current mirror, Q_{13B} scaled to 0.75 of Q_{12}. Neglecting base currents:

$$I_{C13B} = 0.75\, I_{REF} \qquad (13.8)$$

• Collector current in Q_{16}:

$$I_{C16} \cong I_{E16} = I_{B17} + \frac{I_{E17}R_8 + V_{BE17}}{R_9} \qquad (13.9)$$

Figure 13.7: Reference circuit and gain stage of 741 op-amp.

27

11.2.2) Gain Stage (Cont)

Example 13.2

Objective: Calculate the bias currents in the gain stage of the 741 op-amp in **Figure 13.7**. Assume bias voltages of 15 V.

28

11.2.2) Gain Stage (Cont)

Example 13.2 (Cont)

Solution: From **Example 13.1**, $I_{REF} = 0.72$ mA.

From Equation (13.8), the collector current in Q_{17} is

$$I_{C17} = I_{C13B} = 0.75 I_{REF} = (0.75)(0.72\text{m}) = 0.54 \text{ mA}$$

Assuming $\beta = 200$ for the npn transistor, the collector current in Q_{16} is, from Equation (13.9),

$$I_{C16} \approx I_{B17} + (I_{E17}R_8 + V_{BE17})/R_9$$
$$= 0.54\text{m}/200 + [(0.54\text{m})(100) + 0.6]/50\text{k}$$

or

$$I_{C16} = 15.8\ \mu\text{A}$$

29

11.2.3) Output Stage

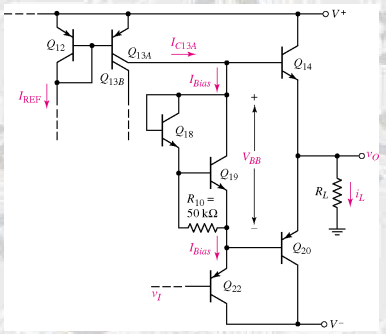


Figure 13.8: Basic output stage of 741 op-amp, showing currents and voltages.

30

11.2.3) Output Stage (Cont)

• I_{Bias} is supplied by Q_{13A} and input signal is applied to base of Q_{22} (emitter follower).

• Q_{18} & Q_{19} → Establishes $2V_{BE}$ drops between base terminals of Q_{14} & Q_{20} → This V_{BB} produces quiescent collector currents in Q_{14} & Q_{20} ➔ Biasing both Q_{14} & Q_{20} "on" with no signal present at the input, **to remove crossover distortion**.

• Q_{13A} is scaled to 0.25 of Q_{12}. Neglecting base currents,

$$I_{C13A} = 0.25\, I_{REF} = I_{Bias} \qquad (13.10)$$

31

11.2.3) Output Stage (Cont)

• Neglecting base currents,

$$I_{C22} = I_{Bias}$$

• Collector current in Q_{18} is

$$I_{C18} \approx V_{BE19} / R_{10} \qquad (13.11)$$

• Therefore,

$$I_{C19} = I_{Bias} - I_{C18} \qquad (13.12)$$

32

11.2.3) Output Stage (Cont)

• Since V_{BB} remains almost constant:

- ❑ As v_I increases, base voltage of Q_{14} increases and v_O increases
- ❑ As v_I decreases, base voltage of Q_{20} decreases and v_O decreases

• The small-signal voltage gain of output stage is essentially unity.

33

11.2.3) Output Stage (Cont)

Example 13.3

Objective: Calculate the bias currents in the output stage of the 741 op-amp.

Consider the output stage in Figure 13.8. Assume the reverse saturation currents of Q_{18} and Q_{19} are $I_S = 10^{-14}$ A, and the reverse saturation currents of Q_{14} and Q_{20} are $I_S = 3 \times 10^{-14}$ A. Neglect base currents.

34

11.2.3) Output Stage (Cont)

Example 13.3 (Cont)

Solution: The reference current, **from Example 13.1**, is $I_{REF} = 0.72$ mA. Current I_{C13A} is then

$I_{C13A} = 0.25\, I_{REF} = (0.25)(0.72\text{m}) = 0.18$ mA $\approx I_{Bias}$

If we **assume** $V_{BE19} = 0.6$ V, then the current in R_{10} is

$I_{R10} = V_{BE19} / R_{10} = 0.6 / 50\text{k} = 0.012$ mA

The current in Q_{19} is

$I_{C19} \approx I_{E19} = I_{C13A} - I_{R10} = 0.18\text{m} - 0.012\text{m}$

→ $I_{C19} = 0.168$ mA

35

11.2.3) Output Stage (Cont)

Example 13.3 (Cont)

For that value of collector current, the B-E voltage of Q_{19} is

$V_{BE19} = V_T \ln(I_{C19} / I_S)$

→ $V_{BE19} = (0.026)\ln(0.168\text{m}/10^{-14}) = 0.612$ V

which is close to the assumed value of 0.6 V.

Assuming $\beta_n = 200$ for the npn devices, the base current in Q_{19} is

$I_{B19} = I_{C19} / \beta_n = 0.168\text{m} / 200 = 0.84\ \mu$A

36

11.2.3) Output Stage (Cont)

Example 13.3 (Cont)

The current in Q_{18} is now

$I_{C18} \approx I_{E18} = I_{R10} + I_{B19}$ **= 0.012m + 0.84μ**

→ I_{C18} **= 12.84 μA**

The B-E voltage of Q_{18} is therefore

$V_{BE18} = V_T \ln(I_{C18} / I_S)$

→ $V_{BE19} = (0.026) \ln(12.84\mu/10^{-14})$ **= 0.545 V**

The voltage difference V_{BB} is thus

$V_{BB} = V_{BE18} + V_{BE19}$ = 0.545 + 0.612 **= 1.157 V**

11.2.3) Output Stage (Cont)

Example 13.3 (Cont)

Since the output transistors Q_{14} and Q_{20} are identical, one-half of V_{BB} is across each B-E junction.

The quiescent currents in Q_{14} and Q_{20} are

$I_{C14} = I_{C20} = I_S \exp((V_{BB}/2) / V_T)$

→ $I_{C14} = I_{C20} = (3 \times 10^{-14}) \exp((1.157/2) / 0.026)$

or $I_{C14} = I_{C20} = 138\ \mu A$

11.2.4) Short-Circuit Protection Circuitry

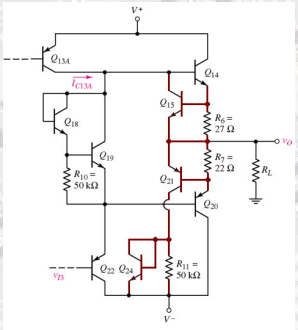


Figure 13.9: Output stage, 741 op-amp with short-circuit protection devices.

11.2.4) Short-Circuit Protection Circuitry (Cont)

➔ To protect Q_{14} from burnout due to large current induced **if the output is shorted to ground** during a positive signal.

• R_6 and Q_{15} limit the current in Q_{14} in the event of a short circuit.

- ❑ If current in Q_{14} reaches 20 mA, V_{R6} is 540 mV
- ❑ Q_{15} turns on, and conducts excess base current in Q_{14} into its collector.
- ❑ Thus, base current into Q_{14} is limited to a maximum value, which limits the collector current.

11.2.4) Short-Circuit Protection Circuitry (Cont)

• The maximum current in Q_{20} is limited by components R_7, Q_{21} & Q_{24}.

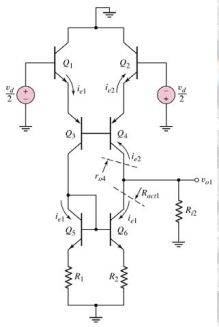
- ❑ A large output current results in a voltage drop across R_7 (V_{R7}), sufficient to turn on Q_{21}.
- ❑ Excess current in Q_{20} will be shunted by Q_{21} and Q_{24}. This protects output transistor Q_{20}.

11.3) Small-Signal Analysis

Steps in AC Analysis:

- Analyze the small-signal properties of the building blocks individually.
- Loading effects of follow-on stages must be taken into account in the analysis of each building block.

11.3.1) Input Stage



- Effective impedance at base of Q_3 & Q_4 is ideally infinite, i.e. open circuit, due to constant-current biasing at base of Q_3 & Q_4
- R_{act1} is the effective resistance of active load.
- R_{i2} is the input resistance of gain stage.

Figure 13.10: The **ac equivalent** circuit, input stage of 741 op-amp.

11.3.1) Input Stage (Cont)

- The small-signal differential voltage gain is

$$A_d = \frac{v_{o1}}{v_d} = -g_m\left(r_{o4} \| R_{act1} \| R_{i2}\right)$$

$$\Rightarrow A_d = -\left(\frac{I_{CQ}}{V_T}\right)\left(r_{o4} \| R_{act1} \| R_{i2}\right) \quad (13.13)$$

where I_{CQ} = quiescent collector current in each of the transistors Q_1 to Q_4

and r_{o4} = small-signal output resistance looking into the collector of Q_4

11.3.1) Input Stage (Cont)

- Effective resistance of active load (for output resistance of a Widlar current source):

$$R_{act1} = r_{o6}\left[1 + g_{m6}\left(R_2 \| r_{\pi 6}\right)\right] \quad (13.14)$$

- Input resistance of gain stage:

$$R_{i2} = r_{\pi 16} + (1+\beta_n)R_E' \quad (13.15)$$

where $$R_E' = R_9 \| \left[r_{\pi 17} + (1+\beta_n)R_8\right] \quad (13.16)$$

is effective resistance in emitter of Q_{16}

11.3.1) Input Stage (Cont)

Example 13.4

Objective: Determine the small-signal differential voltage gain of the 741 op-amp input stage.

Assume npn transistor gains of β_n = 200 and Early voltages of V_A = 50 V.

11.3.1) Input Stage (Cont)

Example 13.4 (Cont)

Solution: The quiescent collector currents were **determined previously** from previous examples. The input resistance to the gain stage is found from Equation (13.15) and (13.16), as follows:

$$r_{\pi 17} = \frac{\beta_n V_T}{I_{C17}} = \frac{(200)(0.026)}{0.54\text{m}} = 9.63\text{k}\Omega$$

$$R_E' = R_9 \| \left[r_{\pi 17} + (1+\beta_n)R_8\right]$$

$$\Rightarrow R_E' = 50\text{k} \| \left[9.63\text{k} + (1+200)(0.1\text{k})\right] = 18.6\text{k}\Omega$$

11.3.1) Input Stage (Cont)

Example 13.4 (Cont)

Also,

$$r_{\pi 16} = \frac{\beta_n V_T}{I_{C16}} = \frac{(200)(0.026)}{15.8\mu} = 329\text{k}\Omega$$

Consequently,

$$R_{i2} = r_{\pi 16} + (1+\beta_n)R_E'$$

$$\Rightarrow R_{i2} = 329\text{k} + (201)(18.6\text{k}) = 4.07\text{M}\Omega$$

11.3.1) Input Stage (Cont)

Example 13.4 (Cont)

The resistance of the active load is determined from Equation (13.14). Can be found

$$r_{\pi 6} = \frac{\beta_n V_T}{I_{C6}} = \frac{(200)(0.026)}{9.5\mu} = 547\text{k}\Omega$$

$$g_{m6} = \frac{I_{C6}}{V_T} = \frac{9.5\mu}{0.026} = 0.365\text{mA/V}$$

and $$r_{o6} = \frac{V_A}{I_{C6}} = \frac{50}{9.5\mu} = 5.26\text{M}\Omega$$

49

11.3.1) Input Stage (Cont)

Example 13.4 (Cont)

Then,

$$R_{act1} = r_{o6}\left[1 + g_{m6}\left(R_2 \| r_{\pi 6}\right)\right]$$

$$\Rightarrow R_{act1} = 5.26\text{M}\left[1 + (0.365\text{m})\left(1\text{k}\|547\text{k}\right)\right]$$

$$\Rightarrow R_{act1} = 7.18\text{M}\Omega$$

Resistance r_{o4} is

$$r_{o4} = \frac{V_A}{I_{C4}} = \frac{50}{9.5\mu} = 5.26\text{M}\Omega$$

50

11.3.1) Input Stage (Cont)

Example 13.4 (Cont)

Finally, from Equation (13.13), the small-signal voltage gain is

$$A_d = -\left(\frac{I_{CQ}}{V_T}\right)\left(r_{o6}\|R_{act1}\|R_{i2}\right)$$

$$\Rightarrow A_d = -\left(\frac{9.5\mu}{0.026}\right)\left(5.26\text{M}\|7.18\text{M}\|4.07\text{M}\right)$$

$$\Rightarrow A_d = -636$$

51

11.3.2) Gain Stage

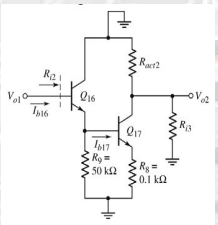


Figure 13.11: The ac equivalent circuit, gain stage of 741 op-amp.

- R_{act2} is the effective resistance of active load.
- R_{i3} is **input resistance of the output stage**.
- Use **Fig 13.11** to develop small-signal voltage gain.
- Input base current to Q_{16} is:

$$i_{b16} = v_{o1} / R_{i2} \quad (13.17)$$

where R_{i2} is **the input resistance of gain stage**.

52

11.3.2) Gain Stage (Cont)

- Base current into Q_{17} is:

$$i_{b17} = \frac{R_9}{R_9 + \left[r_{\pi 17} + (1+\beta_n)R_8\right]} \times i_{e16} \quad (13.18)$$

where i_{e16} = emitter current from Q_{16}

- The output voltage is:

$$v_{o2} = -i_{c17}\left(R_{act2}\|R_{i3}\|R_{o17}\right) \quad (13.19)$$

where i_{c17} = ac collector current in Q_{17}
and R_{o17} = output impedance looking into the collector of Q_{17}

53

11.3.2) Gain Stage (Cont)

- Combining (13.17), (13.18), and (13.19):

$$A_{v2} = \frac{v_{o2}}{v_{o1}} = \frac{-\beta_n(1+\beta_n)R_9\left(R_{act2}\|R_{i3}\|R_{o17}\right)}{R_{i2}\left(R_9 + \left[r_{\pi 17} + (1+\beta_n)R_8\right]\right)}$$

- The **effective resistance of active load** is the resistance looking into collector of Q_{13B}, or:

$$R_{act2} = r_{o13B} = \frac{V_A}{I_{C13B}} \quad (13.21)$$

54

11.3.3) Output Stage

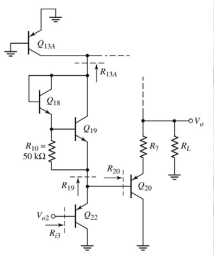


Figure 13.12: The ac equivalent circuit, 741 op-amp output stage, for calculating input resistance.

Finding Input Resistance:

• Use **Fig 13.12** to determine the **input resistance** of the output stage, i.e. R_{i3}.

• Assume that pnp output Q_{20} is active and npn output Q_{14} is cut-off. R_L is included.

• Since Q_{22} operates as an emitter follower, the input resistance R_{i3} is:

$$R_{i3} = r_{\pi 22} + (1+\beta_p)[R_{19} \| R_{20}]$$

11.3.3) Output Stage (Cont)

• Resistance R_{19} is series combination of resistance looking into emitter of Q_{19} and Q_{18}, and resistance looking into collector of Q_{13A}. Effective resistance of the combination of Q_{18} and Q_{19} is small compared to R_{13A}; therefore,

$$R_{19} \cong R_{13A} = r_{o13A} = V_A / I_{C13A} \qquad (13.23)$$

• Q_{20} is also an emitter follower, therefore,

$$R_{20} = r_{\pi 20} + (1+\beta_p)R_L \qquad (13.24)$$

with the assumption that $R_L >> R_7$

11.3.3) Output Stage (Cont)

Example 13.5

11.3.3) Output Stage (Cont)

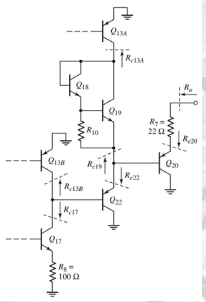


Figure 13.13: The ac equivalent circuit, 741 op-amp output stage, for calculating output resistance.

Finding Output Resistance:

• Use Fig 13.13 to determine the **output resistance** of the output stage, i.e. R_o.

• Assume that Q_{20} is conducting and Q_{14} is cut-off. Same basic result is obtained when Q_{14} is conducting and Q_{20} is cut-off.

• The output resistance R_o is:

$$R_o = R_7 + R_{e20} \qquad (13.27)$$

11.3.3) Output Stage (Cont)

• Resistance R_{e20} is:

$$R_{e20} = \frac{r_{\pi 20} + R_{e22} \| R_{c19}}{(1+\beta_p)} \qquad (13.28)$$

• Series resistance due to Q_{18} and Q_{19} is small compared to R_{c13A}, so that $R_{c19} \approx R_{c13A}$.

• Also,

$$R_{e22} = \frac{r_{\pi 22} + R_{c17} \| R_{c13B}}{(1+\beta_p)} \qquad (13.29)$$

where $R_{c13B} = r_{o13B}$ and $R_{c17} = r_{o17}\left[1 + g_{m17}(R_8 \| r_{\pi 17})\right]$

11.3.3) Output Stage (Cont)

Example 13.6

11.3.4) Overall Gain

- In calculating voltage gain of each stage, loading effect of the following stage is accounted.
- Therefore, the overall voltage gain is the product of the individual gain factors, or

$$A_v = A_d A_{v2} A_{v3}$$

where A_{v3} is voltage gain of the output stage. It is assumed that $A_{v3} \approx 1$ because output stage is emitter follower.

- **Typical voltage gain values of the 741 op-amp is in the range of 200,000.**

Larger circuits

11.1) Circuit Description

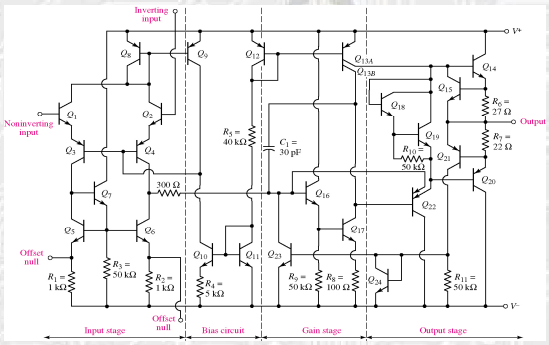


Figure 13.3: Equivalent circuit, 741 op-amp.

11.1.1) Input Diff-Amp and Biasing

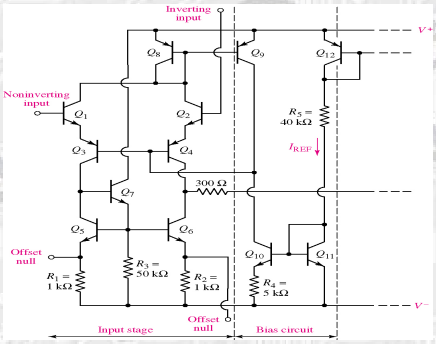


Figure 13.5: Bias circuit and input stage of 741 op-amp.

11.1.2) Gain Stage

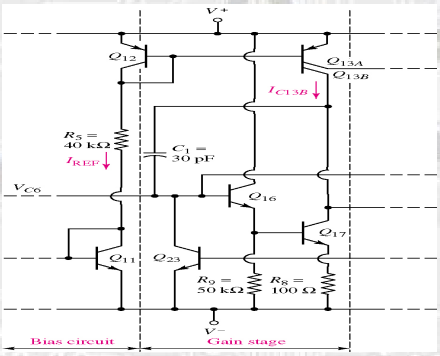


Figure 13.7: Reference circuit and gain stage of 741 op-amp.

11.1.3) Output Stage

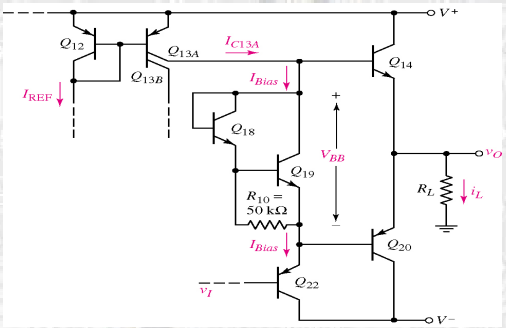


Figure 13.8: Basic output stage of 741 op-amp, showing currents and voltages.

11.2.4) Short-Circuit Protection Circuitry

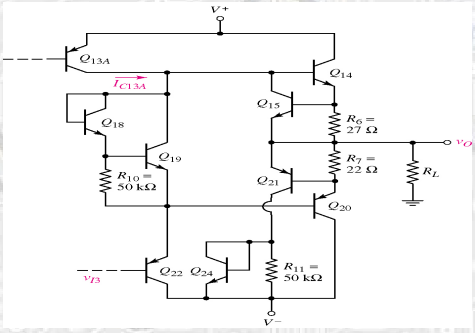


Figure 13.9: Output stage, 741 op-amp with short-circuit protection devices.

67