(12)
Op-Amp Circuits: CMOS Op-Amp

Reference: Neamen, Chapter 13

1

Learning Outcome

Able to:

- Describe and analyze the dc and ac characteristics of CMOS op-amp circuits.

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12.0) CMOS Op-Amp Circuits

- Most CMOS op-amps:
  - ❑ are designed for specific on-chip applications
  - ❑ only required to drive capacitive loads of few pF
  - ❑ do not need low-resistance output stage
  - ❑ do not need electrostatic input protection devices if the op-amp inputs are not connected directly to IC external terminals
- Two designs will be considered:
  1) **MC14573 CMOS op-amp circuit**
  2) **Folded-cascode op-amp**
- DC and small-signal analysis will be performed.

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12.1) MC14573 CMOS Op-Amp Circuit

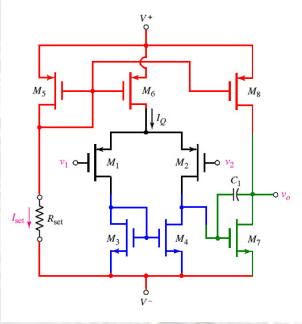

Figure 13.14: MC14573 CMOS op-amp equivalent circuit.

- **Input Stage:**
  - ❑ **M_1 and M_2: PMOS input differential pair.**
  - ❑ **M_3 and M_4: NMOS active load.**
  - ❑ **M_5 and M_6: current mirror for input stage biasing, reference current I_{set} can be determined by R_{set}**

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12.1) MC14573 CMOS Op-Amp Circuit (Cont)

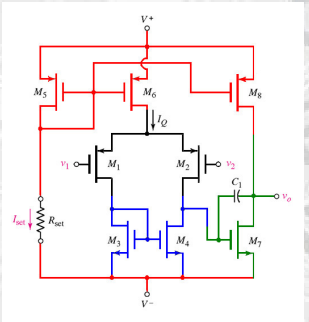

Figure 13.14: MC14573 CMOS op-amp equivalent circuit.

- **Second Stage (also Output Stage):**
  - ❑ **M_7**: common-source -connected transistor.
  - ❑ **M_8**: provides bias current for **M_7**, also acts as **active load**.
  - ❑ Capacitor **C_1**: internal feedback compensation (**Miller compensation**) to provide stability.

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12.1) MC14573 CMOS Op-Amp Circuit (Cont)

12.1.1) DC Analysis

- Assuming M_5 and M_6 are matched, the reference and input-stage bias currents are given by:

$$I_{set} = I_Q = \frac{V^+ - V^- - V_{SG5}}{R_{set}} \qquad (13.36)$$

- The reference current and source-to-gate voltage V_{SG5} are also related by:

$$I_{set} = K_{p5}(V_{SG5} + V_{TP})^2 \qquad (13.37)$$

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12.1) MC14573 CMOS Op-Amp Circuit (Cont)

12.1.1) DC Analysis (Cont)

• The quiescent bias currents can be changed by changing resistor R_{set}.

• If transistors M_6 and M_8 are identical to M_5, then their currents:

$$I_{D6} = I_{D8} = I_{D5} = I_{set}$$

since $V_{SG6} = V_{SG8} = V_{SG5}$.

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12.1) MC14573 CMOS Op-Amp Circuit (Cont)

12.1.1) DC Analysis (Cont)

Example 13.8

Objective: Determine the dc bias currents in the MC14573 op-amp.

Assume transistor parameters of $|V_T| = 0.5$ V (all transistors), $k'_n = 100\ \mu A/V^2$, $k'_p = 40\ \mu A/V^2$, and the circuit parameters of $V^+ = 5$ V, $V^- = -5$ V, and $R_{set} = 225$ kΩ.

Assume transistor width-to-length ratios of **6.25** for M_3 and M_4, and **12.5** for all other transistors.

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12.1) MC14573 CMOS Op-Amp Circuit (Cont)

12.1.1) DC Analysis (Cont)

Example 13.8 (Cont)

Solution: For M_5 and M_6, the conduction parameters are:

$$K_p = (k'_p/2)(W/L)_5 = (40\mu/2)(12.5) = 0.25\ mA/V^2$$

Combining Equations (13.36) and (13.37) yields the source-to-gate voltage of M_5:

$$K_p (V_{SG5} + V_{TP})^2 = (V^+ - V^- - V_{SG5}) / R_{set}$$

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12.1) MC14573 CMOS Op-Amp Circuit (Cont)

12.1.1) DC Analysis (Cont)

Example 13.8 (Cont)

or $(0.25m)(V_{SG5} - 0.5)^2 = (5 - (-5) - V_{SG5}) / 225k$

which yields $V_{SG5} = 0.9022$ V $\quad \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$

From Equation (13.36),

$I_{REF} = I_Q = (10 - 0.9022)/225k = 40.4\ \mu A$

The quiescent drain currents in M_7 and M_8 are then also **40.4 μA**, and the currents in M_1 through M_4 are **20.2 μA.**

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12.1) MC14573 CMOS Op-Amp Circuit (Cont)

12.1.1) DC Analysis (Cont)

Do Ex 13.8

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12.1) MC14573 CMOS Op-Amp Circuit (Cont)

12.1.2) Small-Signal Analysis

• The small-signal differential **voltage gain of input stage**:

$$A_d = \sqrt{2K_{p1}I_Q}\left(r_{o2} \| r_{o4}\right) \qquad (13.38)$$

where r_{o2} and r_{o4} are output resistances of M_2 and M_4 respectively.

• Input impedance to the 2nd stage is essentially infinite. Hence, no loading effect due to 2nd stage.

• Assuming λ is identical for all transistors,

$$r_{o2} = r_{o4} = \frac{1}{\lambda I_D} = \frac{1}{\lambda(I_Q/2)} \qquad (13.39)$$

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12.1) MC14573 CMOS Op-Amp Circuit (Cont)

12.1.2) Small-Signal Analysis (Cont)

• The **magnitude** of the **gain of the second stage**:

$$A_{v2} = g_{m7}\left(r_{o7} \| r_{o8}\right) \qquad (13.40)$$

where $g_{m7} = 2\sqrt{K_{n7} I_{D7}}$

and $r_{o7} = r_{o8} = 1/\lambda I_{D7}$

➔Equation (13.40) implies that there is no loading effect due to an external load connected at output.

Note: The open-loop gain of a CMOS op-amp is generally less than that of a bipolar op-amp, but the use of active loads provides acceptable results.

12.1) MC14573 CMOS Op-Amp Circuit (Cont)

12.1.2) Small-Signal Analysis (Cont)

Example 13.9

Objective: Determine the small-signal voltage gains of the input and second stages, and the overall voltage gain, of the **MC14573 op-amp**.

Assume the same transistor and circuit parameters as in **Example 13.8**. Let **λ = 0.02 V^{-1}** for all transistors.

12.1) MC14573 CMOS Op-Amp Circuit (Cont)

12.1.2) Small-Signal Analysis (Cont)

Example 13.9 (Cont)

Solution: The conduction parameters of M_1 and M_2 are

$K_{p1} = K_{p2} = (k'_p/2)(W/L)_1$

➔ $K_{p1} = K_{p2} = (40\mu/2)(12.5) = 0.25$ mA/V^2

and the output resistances are

$r_{o2} = r_{o4} = 1 / (\lambda I_D)$

➔ $r_{o2} = r_{o4} = 1 / ((0.02)(20.2\mu)) = 2.475$ MΩ

12.1) MC14573 CMOS Op-Amp Circuit (Cont)

12.1.2) Small-Signal Analysis (Cont)

Example 13.9 (Cont)

From Equation (13.38), the gain of the input stage is then

$$A_d = \sqrt{2K_{p1}I_Q}\left(r_{o2} \| r_{o4}\right)$$

$$\Rightarrow A_d = \sqrt{2(0.25\text{m})(40.4\mu)}\left(2475 \| 2475\right) = 176$$

The transconductance of M_7 is

$$g_{m7} = 2\sqrt{(k_n'/2)(W/L)_7 I_{D7}}$$

$$\Rightarrow g_{m7} = 2\sqrt{(100\mu/2)(12.5)(40.4\mu)} = 0.3178\text{mA/V}$$

12.1) MC14573 CMOS Op-Amp Circuit (Cont)

12.1.2) Small-Signal Analysis (Cont)

Example 13.9 (Cont)

and the output resistances of M_7 and M_8 are

$r_{o7} = r_{o8} = 1 / (\lambda I_{D7})$

➔ $r_{o7} = r_{o8} = 1 / ((0.02)(40.4\mu)) = 1.238$ MΩ

From Equation (13.40), the gain of the second stage is then

$A_{v2} = g_{m7}(r_{o7} \| r_{o8})$

➔ $A_{v2} = (0.3178\text{m})(1.238\text{M}\|\|1.238\text{M}) = 197$

Finally, the overall voltage gain of the op-amp is

$A_v = A_d A_{v2} = (176)(197) = 34{,}672$

12.1) MC14573 CMOS Op-Amp Circuit (Cont)

12.1.2) Small-Signal Analysis (Cont)

Problem 13.29

12.1) MC14573 CMOS Op-Amp Circuit (Cont)

12.1.2) Small-Signal Analysis (Cont)

Do Ex 13.9

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Skip 12.2) Cascade CMOS Op-Amp Circuits

• The voltage gain of an amplifier can be increased by using a cascode configuration.

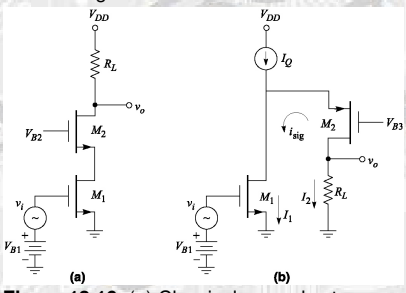

Figure 13.16: (a) Classical cascode stage (b) Folded-cascode stage

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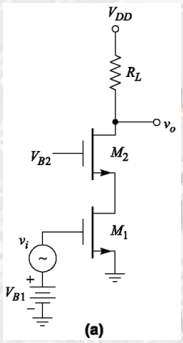
12.2) Cascode CMOS Op-Amp Circuits (Cont)



• Figure 13.16 (a) ➔Conventional cascode configuration

- ❑ Consists of 2 transistors in series.
- ❑ M_1 = common-source amplifying device, dc current I_{D1} is determined by input voltage v_i
- ❑ M_2 = common-gate configuration.
- ❑ I_{D1} is input signal to M_2
- ❑ Output is taken off the drain of cascode transistor.
- ❑ AC current is through both transistors and dc power supply.

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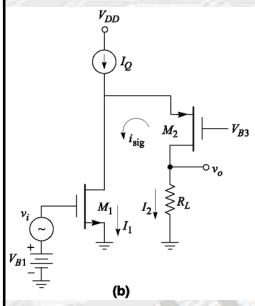
12.2) Cascode CMOS Op-Amp Circuits (Cont)



• Figure 13.16 (b) ➔Folded-cascode configuration

- ❑ DC current I_1 in M_1 determined by input voltage v_i
- ❑ DC current in $M_2 = I_2$
  ➔ $I_2 = I_Q - I_1$
- ❑ AC current is through both transistors and ground.
- ❑ AC currents in M_2 & M_1, **equal in magnitude but opposite in directions**

→ **current is folded back**
➔ **folded cascode circuit**

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12.3) CMOS Folded-Cascode Op-Amp

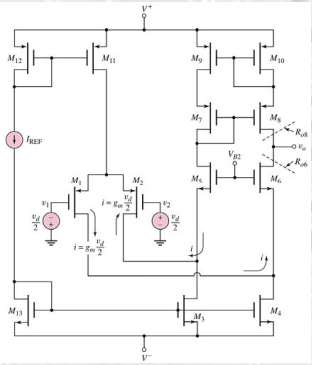

Figure 13.17: CMOS folded-cascode amplifier.

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12.3) CMOS Folded-Cascode Op-Amp (Cont)

• Folded-cascode configuration can be applied to the diff-amp as shown in **Figure 13.17**

- ❑ M_1 and M_2: PMOS input differential pair.
- ❑ M_5 and M_6: cascode transistors.
- ❑ M_7 to M_{10}: form a modified Wilson current mirror acting as active load.
- ❑ The biasing V_{B1} and V_{B2} must be provided by a separate network.

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12.3) CMOS Folded-Cascode Op-Amp (Cont)

• Assuming that transistors M_3, M_4 and M_{11} - M_{13} are all matched, then:
- ❑ dc currents in M_1 and M_2 are I_{REF} / 2
- ❑ dc currents in M_3 and M_4 are I_{REF}
- ➔ dc currents in M_5 and M_6 are I_{REF} / 2

• If a differential-mode input voltage v_d is applied, then ac currents are induced in the differential pair as shown in **Figure 13.17**
- ❑ AC current in M_1 flows through M_6 to output.
- ❑ AC current in M_2 flows through M_5 and is induced in M_8 by current-mirror action of the active load.

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12.3) CMOS Folded-Cascode Op-Amp (Cont)

• Hence, from previous work on diff-amps, **the differential-mode voltage gain** is:

$$A_d = g_{m1}\left(R_{o6} \| R_{o8}\right) \qquad (13.41)$$

where $R_{o6} = g_{m6}\left(r_{o6}\right)\left(r_{o4} \| r_{o1}\right)$

and $R_{o8} = g_{m8}\left(r_{o8} r_{o1}\right)$

• Note: Body effect is neglected. Normally the substrates of all NMOS devices are tied to V- and the substrates of all PMOS devices are tied to V+

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12.3) CMOS Folded-Cascode Op-Amp (Cont)

• Study Example 13.11

• Comments from the example:

❑ Very high differential-mode voltage gains can be achieved in a folded-cascode CMOS circuit compared to simple diff-amp circuits.

❑ Output resistance may be limited by leakage currents in actual circuits, so actual gain is less than ideal gain.

• Do Ex 13.11

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Larger circuits

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12.1) MC14573 CMOS Op-Amp Circuit

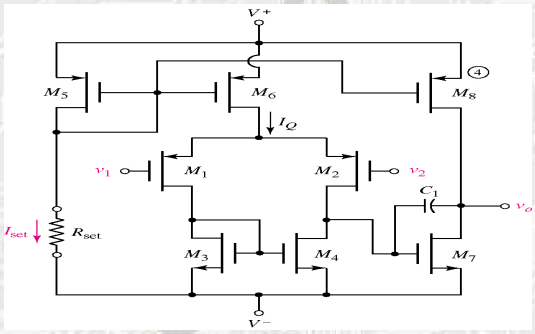

Figure 13.14: MC14573 CMOS op-amp equivalent circuit

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12.1) MC14573 CMOS Op-Amp Circuit (Cont)

Problem 13.29 (Cont)

A simple CMOS op-amp circuit as shown in **Figure P13.29** is biased with I_Q **= 200 µA**. The transistor parameters are k'_n **= 100 µA/V²**, k'_p **= 40 µA/V²**, V_{TN} **= 0.4 V**, V_{TP} **= -0.4 V**, and $\lambda_n = \lambda_p$ **= 0**. The transistor width-to-length ratios are $(W/L)_1 = (W/L)_2$ **= 20,** $(W/L)_3$ **= 50,** and $(W/L)_4$ **= 40**.

i) Design the circuit (i.e. find the values of R_{D1}, R_{D2}, and R_S) such that I_{D3} **= 150 µA,** I_{D4} **= 200 µA,** and v_o **= 0** for $v_1 = v_2$ **= 0.**
ii) Find the overall small-signal voltage gain if the gain of the gain stage is **-19.21**.

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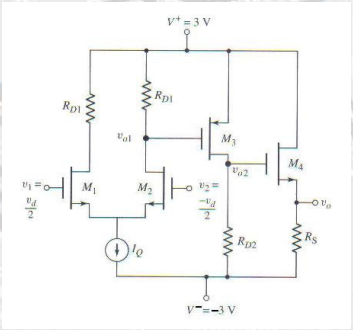
12.1) MC14573 CMOS Op-Amp Circuit (Cont)

Problem 13.29 (Cont)



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12.1) MC14573 CMOS Op-Amp Circuit (Cont)

Problem 13.29 (Cont)

(i)

$I_{D3} = (k'_p/2)(W/L)_3(V_{SG3} + V_{TP})^2$

$150\mu = (40\mu/2)(50)(V_{SG3} - \mathbf{0.4})^2$

$V_{SG3} = 0.7873$ V

$R_{D1} = V_{SG3} / I_{D1}$
$= V_{SG3} / (I_Q/2)$
$= 0.7873 / (200\mu/2)$
$= \mathbf{7.87\ k\Omega}$

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12.1) MC14573 CMOS Op-Amp Circuit (Cont)

Problem 13.29 (Cont)

(i)

$I_{D4} = (k'_n/2)(W/L)_4(V_{GS4} - V_{TN})^2$

$200\mu = (100\mu/2)(40)(V_{GS4} - \mathbf{0.4})^2$

$V_{GS4} = 0.7162$ V

$V_{G4} = V_O + V_{GS4} = 0 + 0.7162 = \mathbf{0.7162\ V}$

$R_{D2} = (V_{G4} - (V^-)) / I_{D3}$
$= (0.7162 - (-3))/(150\mu) = \mathbf{24.8\ k\Omega}$

$R_S = (V_O - (V^-)) / I_{D4}$
$= (0 - (-3))/(200\mu) = \mathbf{15\ k\Omega}$

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12.1) MC14573 CMOS Op-Amp Circuit (Cont)

Problem 13.29 (Cont)

(ii)

$A_{d1} = (g_{m1} R_{D1})/2$

$g_{m1} = 2\ \text{SQRT}[(k'_n/2)(W/L)_1(I_Q/2)]$
$= 2\ \text{SQRT}[(100\mu/2)(20)(200\mu/2)]$
$= 0.6325$ mA/V

$A_{d1} = ((0.6325m)(7.87k))/2 = \mathbf{2.49}$

$A_2 = \mathbf{-19.21}$ (given)

$A_3 = \mathbf{1}$ (assume)

$A = A_{d1} \times A_2 \times A_3$
$= (2.49) \times (-19.21) \times (1) = \mathbf{-47.8}$

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