COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 1 2019 / 2020

PROGRAMME	: **Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	: **EEEB273/EEEB2014**
SUBJECT	: **ELECTRONIC ANALYSIS AND DESIGN II**
DATE	: **September 2019**
DURATION	: **3 hours**

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **FIVE** (5) questions in **TEN** (10) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided. **Use pen** to write your answer.
4. Write answer to different question on **a new page**.

THIS QUESTION PAPER CONSISTS OF TEN* (10) *PRINTED PAGES INCLUDING THIS COVER PAGE.

Question 1 [20 marks]

As a graduate IC design engineer, you are given a task to design a circuit that meet these specifications:

- BJT current source that utilizes **3 npn transistors** such that the output current (I_O) **= 0.25 mA**
- The circuit output current (I_O) must be **least affected** by change in output voltage (V_O)
- Transistor parameters are: β **= 60**, V_A **= 100 V**, and V_{BE}**(on) = 0.7 V**
- The power supplies: V^+ **= 5 V**, V^- **= -5**

(a) Name and draw the specified circuit with clear details of the Q_1, Q_2 placements, currents and voltages involved. **[5 marks]**

(b) Assume all transistors are matched, derive the relationship between output current (I_O) and the reference current (I_{REF}). **[5 marks]**

(c) Based on your drawing in part (a), **design** the circuit such that it meets the specification. **[4 marks]**

(d) What is the change in output current (I_O) as the output voltage changes from **1V to 5V**. **[6 marks]**

Question 2 [20 marks]

(a) Consider a MOSFET differential amplifier circuit with power supply V^{+}= **5 V**, V^{-}= **0**V as shown in **Figure 1**. Consider transistor parameters where **k' = 100 μA/V² and V_{TN} = 0.3V for all transistors.** It is given that **current I_{D1} = 150 μA** and **width-to-length ratio of transistor M_1, $\left(\frac{W}{L}\right)_1 = 2$**. The differential output voltage is taken at the drain of transistor M_2 with respect to the ground.

(i) Determine the value of R_D such that v_{O2} **is biased at 3.5V.** **[2 marks]**

(ii) Calculate the differential gain of the amplifier. **[3 marks]**

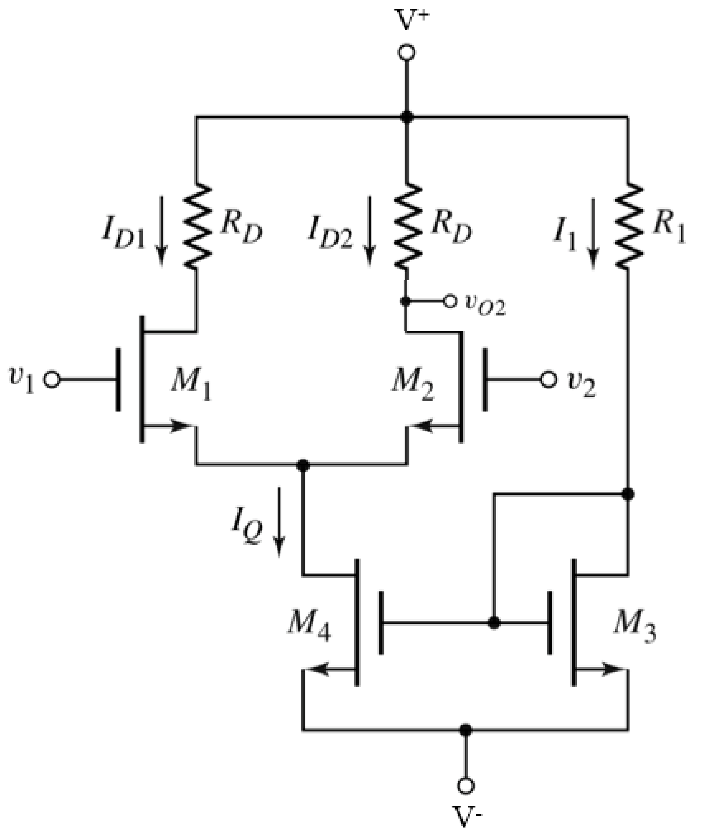


Figure 1

(b) Consider a MOSFET differential amplifier with active load shown in **Figure 2**, with power supply V^{+} **= 10 V** and V^{-} **= -10V**. Transistor parameters are: V_{TP} **= - 0.5 V**, V_{TN} **= 0.4V**, k_n' **= 80μA/V²**, k_p' **= 25μA/V²**, λ_n **= 0.015V⁻¹** and λ_p **= 0.03V⁻¹**.

The constant current source is implemented using a **cascode** current source. **Design** the differential amplifier with active load circuit such that **output voltage range is 80% of the power supply voltage**, and the **maximum power dissipation is 1mW**. Ignore the power dissipation in the biasing circuitry. State all your assumptions. **[15 marks]**

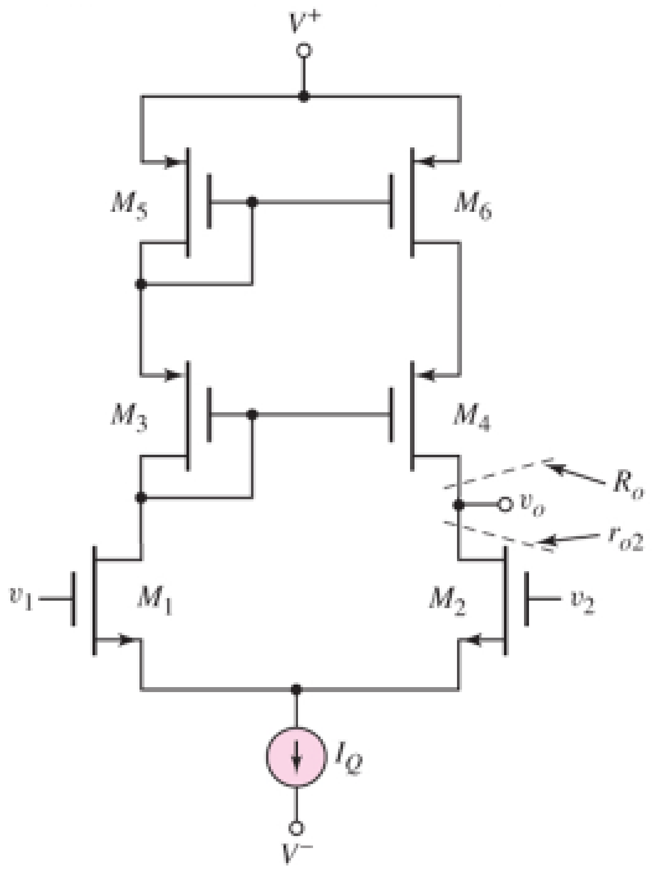


Figure 2

<u>Question 3 [15 marks]</u>

A simple bipolar op-amp is shown in **Figure 3**. Study **Figure 3** carefully.

Neglect base currents. Assume that parameters for all transistors are V_{BE}**(on) = 0.7 V**, β **= 200,** and $V_A = \infty$. **Bias current** for the differential amplifier is I_Q **= 1.4 mA.**

(a) What is the **name** of the amplifiers or circuits with transistors and resistors used in the **Gain Stage** and the **Output Stage**? Indicate the transistors and resistors used in each circuit.

[5 marks]

(b) With small-signal analysis, values of gain A_{d1} for the differential amplifier**,** $r_{\pi3}$**,** and gain A_{v2} for the Gain Stage can be found using the following **Equations (3.1) to (3.3)**.

$$A_{d1} = \frac{V_{o2}}{v_d} = \frac{g_{m2}}{2}(R_C||R_{i2}) \qquad \textbf{(3.1)}$$

$$r_{\pi3} \cong \beta r_{\pi4} \qquad \textbf{(3.2)}$$

$$A_{v2} \cong \frac{I_{R4}}{2V_T}(R_5) \qquad \textbf{(3.3)}$$

Calculate the **total overall small-signal voltage gain (**A_d**)** for the bipolar op-amp.

[10 marks]

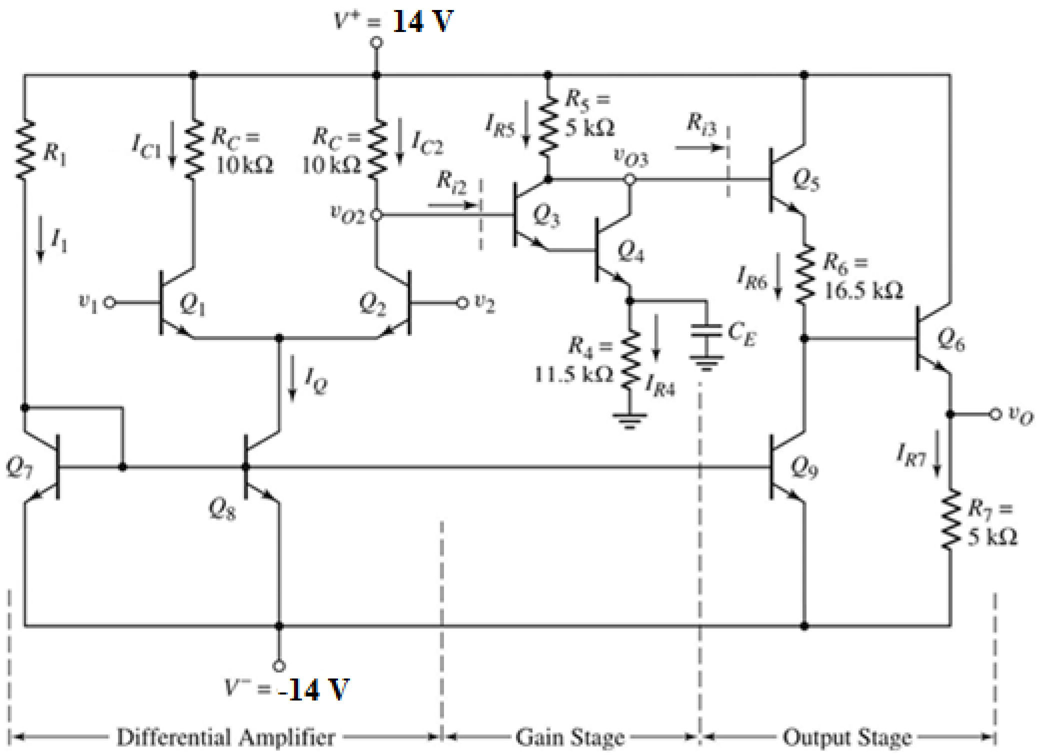


Figure 3

Question 4 [25 marks]

(a) Refer to **Figure 4** below for a **Class B** output stage implemented using the push-pull configuration of Q_n and Q_p transistors. Let $V_{BE}(on) = V_{EB}(on) = 0.6$V. **Sketch** the **voltage transfer characteristic** (v_o vs v_i) for the class B output stage. Clearly indicate the conducting and non-conducting transistors in the relevant zones. **[5 marks]**

(b) For the **class AB** output stage given in **Figure 5**, parameters are V_{CC} = **10V**, R_L=**100Ω**. For the transistors, $I_s = 5\text{x}10^{-15}$**A**, $\beta = \infty$.

(i) For the **quiescent condition** when $v_I = 0$, it is given that $V_{BEn} = V_{EBp} = 0.7$**V.** Calculate the **DC collector currents** of Q_n and Q_p. **[4 marks]**

(ii) For an output voltage of $v_o = -3$**V**, calculate load current i_L, transistor currents i_{Cn} and i_{Cp}. **[6 marks]**

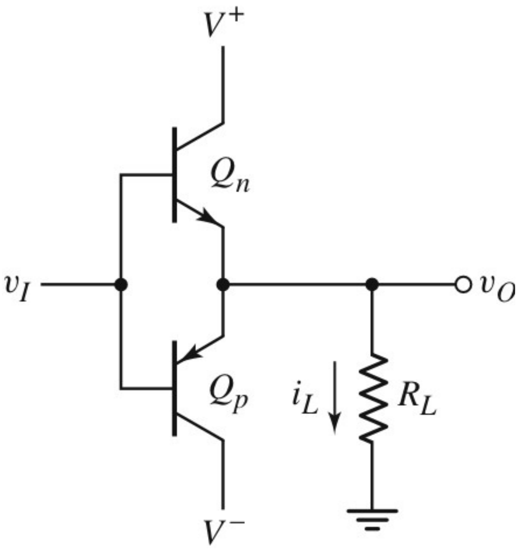


Figure 4

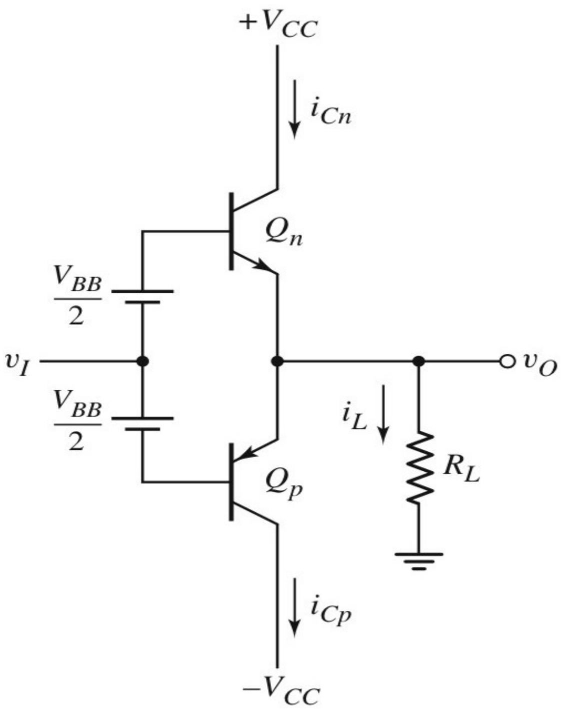


Figure 5

(c) Refer to the MC14573 opamp of **Figure 6.** It is given that for the circuit, V^+= **10V** and V^- = **-10V**. For all transistors, **|V_T|=0.8 V**, k_n'**=40μA/V²**, k_p'**=20μA/V²**, λ_n **= 0.01V⁻¹**, λ_p **= 0.02V⁻¹**. Also $\left(\frac{W}{L}\right)_{3,4}$ **= 10** and for **other transistors (except for the biasing circuitry),** $\left(\frac{W}{L}\right)_{others}$ **= 20.**

Design the biasing circuit such that $I_Q = I_{D8}$ **= 2mA** when $\left(\frac{W}{L}\right)_6 = 4\left(\frac{W}{L}\right)_5$. The **minimum voltage** for current source V_{IQ} is **1V**. What is the **maximum common mode input voltage** for the circuit? **[10 marks]**

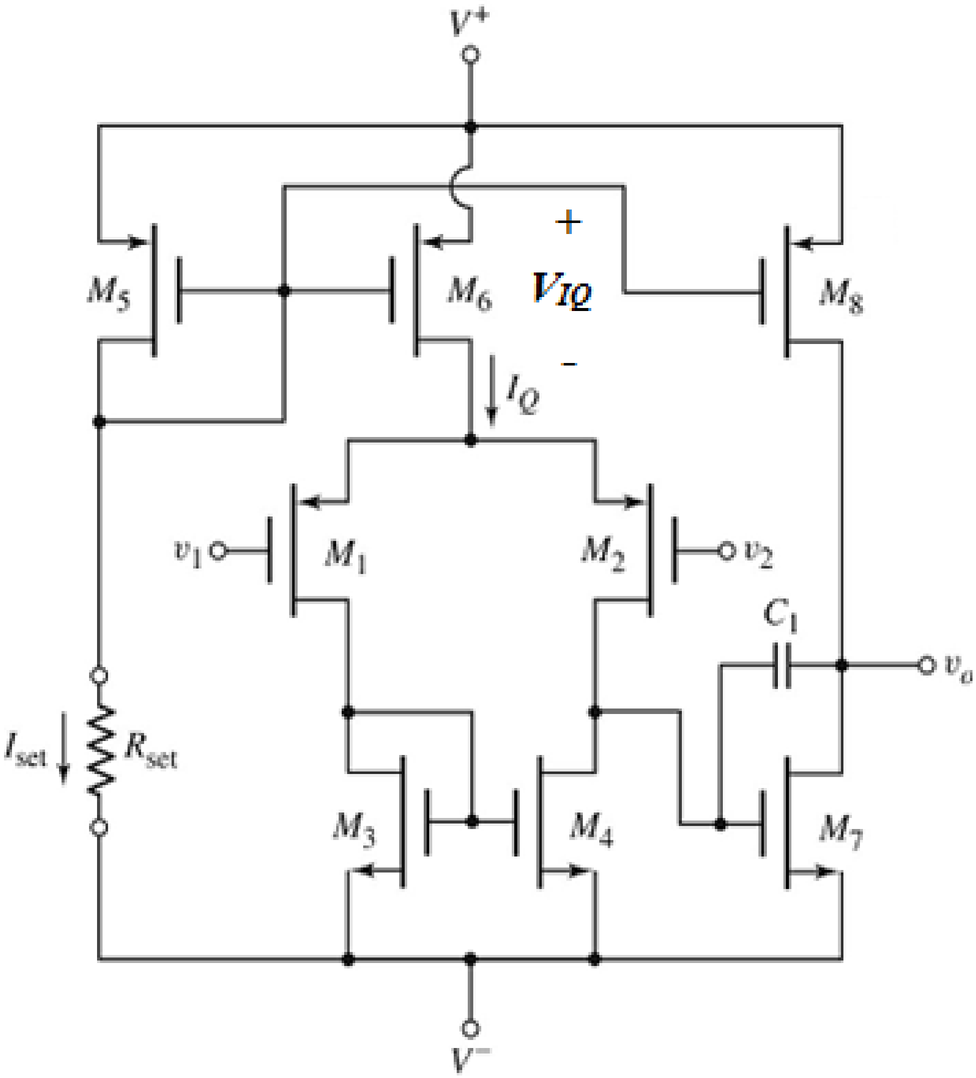


Figure 6

Question 5 [20 marks]

(a) Refer to **Figure 7** and **Figure 8** and answer the following questions.

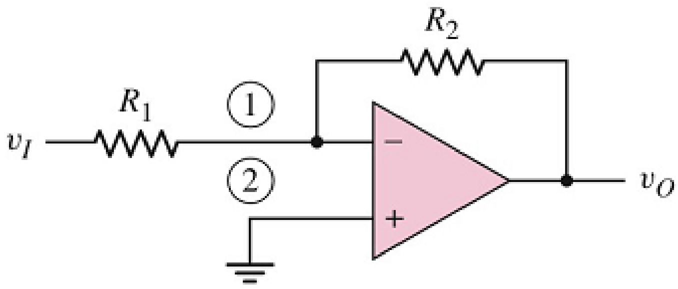


Figure 7

(i) **Identify** the ideal op-amp circuit in the **Figure 7** and **write the equation** that relates between its input voltage **(v_I)** and output voltage **(v_O)**. **Modify** the circuit in the **Figure 7** to make an **inverting summing amplifier** with two (2) inputs v_{I1} and v_{I2} and **draw** the inverting summing amplifier circuit. **[3 marks]**

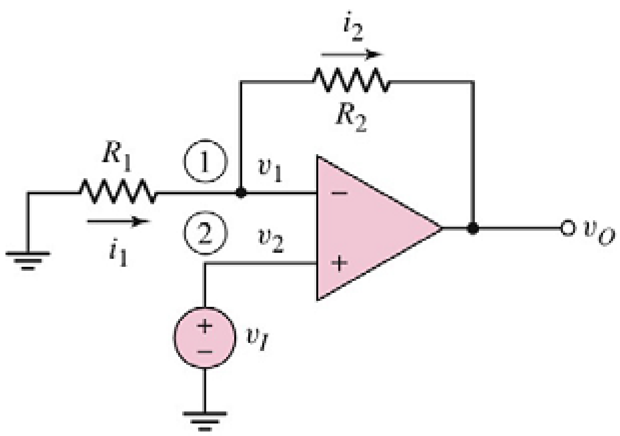


Figure 8

(ii) **Identify** the ideal op-amp circuit in the **Figure 8** and **write the equation** that relates between its input voltage **(v_I)** and output voltage **(v_O)**. **Calculate** v_O when v_I **= 1.5 V,** and $R_1 = R_2 =$ **25 kΩ**. **[3 marks]**

(b) **Consider** the ideal non-inverting op-amp circuit in **Figure 9. Derive** the expression for v_O as a function of v_{I1} and v_{I2}. Then, **calculate** v_O for v_{I1} **= 0.2 V** and v_{I2} **= 0.3 V**.

[6 marks]

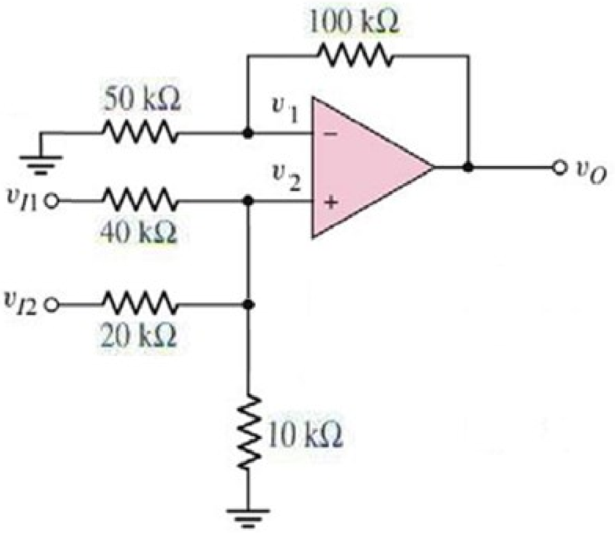


Figure 9

(c) **Assume** the instrumentation amplifier in **Figure 10** has ideal op-amps. The circuit parameters are R_1 **= 10 kΩ,** R_2 **= 40 kΩ,** R_3 **= 40 kΩ,** and R_4 **= 120 kΩ. Determine** the current in R_1 (i_1) and voltages v_{O1}, v_{O2}, and v_O when v_{I1} **= -0.65 + 0.05 sin** ωt **(V)** and v_{I2} **= -0.60 - 0.05 sin** ωt **(V).** **[8 marks]**

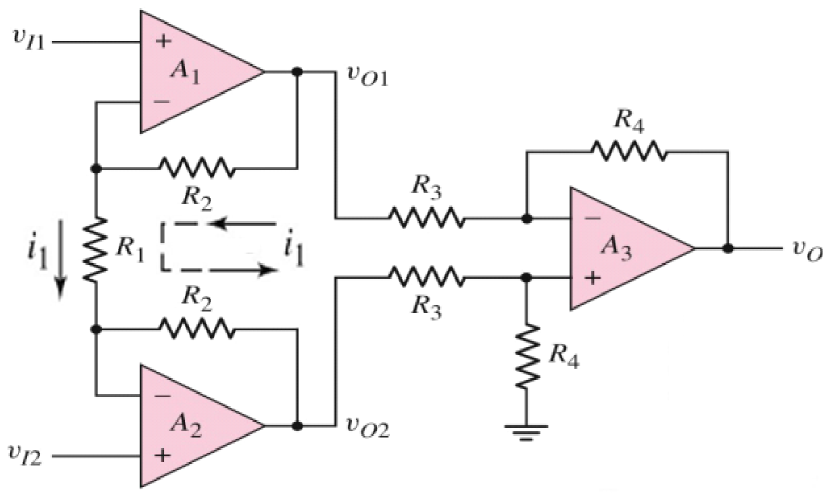


Figure 10

-END OF QUESTION PAPER-

APPENDIX:

A) BASIC FORMULA FOR TRANSISTOR

BJT

$$i_C = I_S e^{v_{BE}/V_T} \quad ;\text{NPN}$$

$$i_C = I_S e^{v_{EB}/V_T} \quad ;\text{PNP}$$

$$i_C = \beta i_B = \frac{\beta}{\beta+1} i_E$$

$$i_E = i_B + i_C$$

;Small signal

$$\beta = g_m r_\pi$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

$$V_T = 26\,\text{mV}$$

MOSFET

;N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n[v_{GS} - V_{TN}]^2$$

$$K_n = \frac{\mu_n C_{ox} W}{2L} = \frac{k_n'}{2} \cdot \frac{W}{L}$$

;P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p[v_{SG} + V_{TP}]^2$$

$$K_p = \frac{\mu_p C_{ox} W}{2L} = \frac{k_p'}{2} \cdot \frac{W}{L}$$

;Small signal

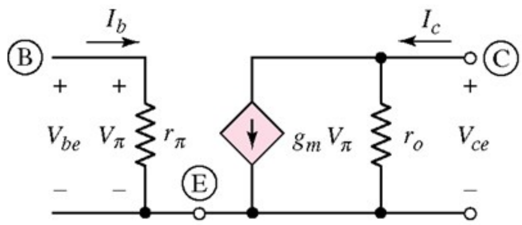
$$g_m = 2\sqrt{K_n I_{DQ}} \quad ;\text{N – MOSFET}$$

$$g_m = 2\sqrt{K_p I_{DQ}} \quad ;\text{P – MOSFET}$$

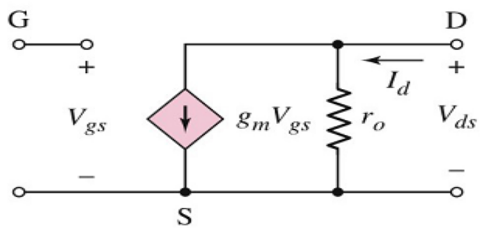
$$r_o \cong \frac{1}{\lambda I_{DQ}}$$

B) HYBRID-π EQUIVALENT CIRCUITS

BJT



MOSFET



C) QUADRATIC FORMULA

$$Ax^2 + Bx + C = 0 \qquad \rightarrow \qquad x = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$