Name:
Student ID Number:
Section Number: 01/02/03 A/B
Lecturer: Dr Fazrena Azlee/ Dr Jamaludin/
Dr Ahmad Wafi
Table Number:

UNIVERSITI TENAGA NASIONAL
The Energy University

College of Engineering
Department of Electrical and Electronics Engineering

Test 2

SEMESTER 1, ACADEMIC YEAR 2019/2020

Subject Code	:	**EEEB2014/EEEB273**
Course Title	:	**Electronics Analysis & Design II**
Date	:	**17 August 2019**
Time Allowed	:	**2 hours**

Instructions to the candidates:

1. Write your Name and Student ID Number. Indicate your Section Number and Lecturerôs Name. Write also your Table Number.
2. **Write all your answers using pen**. **DO NOT USE PENCIL** except for the diagram.
3. **ANSWER ALL QUESTIONS. Show clearly** all your calculations. Every value **must** be written with its correct Unit.
4. **WRITE YOUR ANSWER ON THIS QUESTION PAPER.**

NOTE: DO NOT OPEN THE QUESTION PAPER UNTIL INSTRUCTED TO DO SO.

☺ **GOOD LUCK!** ☺

Question Number	Q1 (abc)	Q1 (d)	Q2 (a)	Q2 (b)	Q3 (ab)	Q4 (a)	Q4 (b)	Total
Marks								

BASIC FORMULA FOR TRANSISTOR

BJT

$i_C = I_S e^{v_{BE}/V_T}$; npn

$i_C = I_S e^{v_{EB}/V_T}$; pnp

$i_C = \alpha i_E = \beta i_B$

$i_E = i_B + i_C$

$$\alpha = \frac{\beta}{\beta + 1}$$

; Small signal

$\beta = g_m r_\pi$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

$V_T = 26\,\text{mV}$

MOSFET

; N – MOSFET

$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$

$i_D = K_n[v_{GS} - V_{TN}]^2$

$$K_n = \frac{k_n'}{2} \cdot \frac{W}{L}$$

; P – MOSFET

$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$

$i_D = K_p[v_{SG} + V_{TP}]^2$

$$K_p = \frac{k_p'}{2} \cdot \frac{W}{L}$$

; Small signal

$g_m = 2\sqrt{K_n I_{DQ}}$; N - MOSFET

$g_m = 2\sqrt{K_p I_{DQ}}$; P - MOSFET

$$r_o \cong \frac{1}{\lambda I_{DQ}}$$

Quadratic formula :

$$Ax^2 + Bx + C = 0 \quad \rightarrow \quad x = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$

QUESTION 1 [30 marks]

The differential amplifier with active load shown in **Figure 1** has a pair of **npn bipolar differential amplifier** as input devices and a pair of **pnp bipolar connected as an active load**. It is given that $V^+ = 5$ **V,** $V^- = -5$ **V,** and $I_Q = 0.4$ **mA.** The transistor parameters are shown in Table 1 below.

Table 1: BJT parameters

npn transistor	**pnp** transistor
$\beta_n = 200$	$\beta_p = 150$
V_{BE} **(on)= 0.67 V**	V_{EB} **(on)=0.65 V**
$V_{An} = 100$ **V**	$V_{Ap} = 70$ **V**

(a) **Calculate** the voltages V_{EC4} and V_{CE2} such that the DC voltages are balanced. It is given that $v_{B1} = v_{B2} = 0$. [8 marks]

(b) **Find** the open-circuit differential-mode voltage gain, A_d. [6 marks]

(c) **Calculate** the value of a load resistance R_L connected to the output v_O if the differential mode voltage gain A_d is to be **reduced to 90%** of the open-circuit gain. [6 marks]

(d) **Draw pnp bipolar differential amplifier** with **npn two-transistor active load**. The current source I_Q is implemented with a **Widlar current source**. **Label the diagram clearly**, showing all necessary currents, resistors, and BJTs used in the circuit. [10 marks]

Answers for Question 1

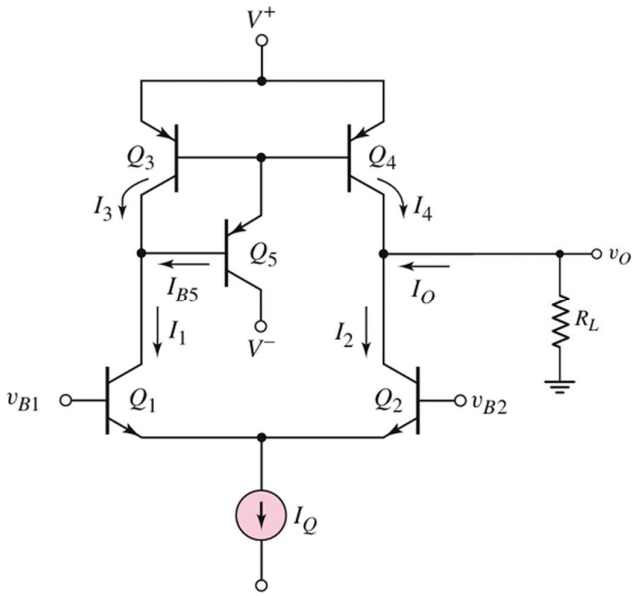

Figure 1

Answers for Question 1 (Continued)

QUESTION 2 [35 marks]

(a) Consider an **NMOS differential amplifier with cascode active load,** where the bias current (I_Q) is generated using a **Wilson Current Mirror**. Draw the **NMOS cascode active load differential amplifier**. Label M_1 **and** M_2 **for differential pair**, $M_3 - M_6$ **for load** and $M_7 - M_9$ **for current biasing circuit**. Also clearly label the input (v_1, v_2) and output v_o. [8 Marks]

Answers for Question 2(a)

(b) Consider the differential amplifier circuit in **Figure 2**. All the NMOS transistors have the same K_n **= 0.2 mA/V^2**, V_{TN} **= 2 V**, and λ_n **= 0.015 V^{-1}**. The active load transistors are matched with parameters K_p **= 0.1 mA/V^2**, V_{TP} **= -2 V**, and λ_p **= 0.02 V^{-1}**. The biasing current, I_Q is **12.8 mA**.

(i) Calculate the **output resistance R_O** of the differential amplifier [5 marks]

(ii) Calculate the **open circuit differential-mode gain** [5 marks]

(iii) The output of the amplifier is connected with **10kΩ load**. Find the differential mode voltage gain. [5 marks]

(iv) The **Common-Mode Rejection Ratio (CMRR)** was measured to be **27.7 dB**. **Using CMRR equation**, calculate the **common-mode voltage gain,** A_{CM} of the amplifier? [5 marks]

(v) Calculate the output voltage, v_O if the differential input voltage is v_1 **= 10.5 sin (ωt) V** and v_2 **= - 9.5 sin (ωt) V.** [7 marks]

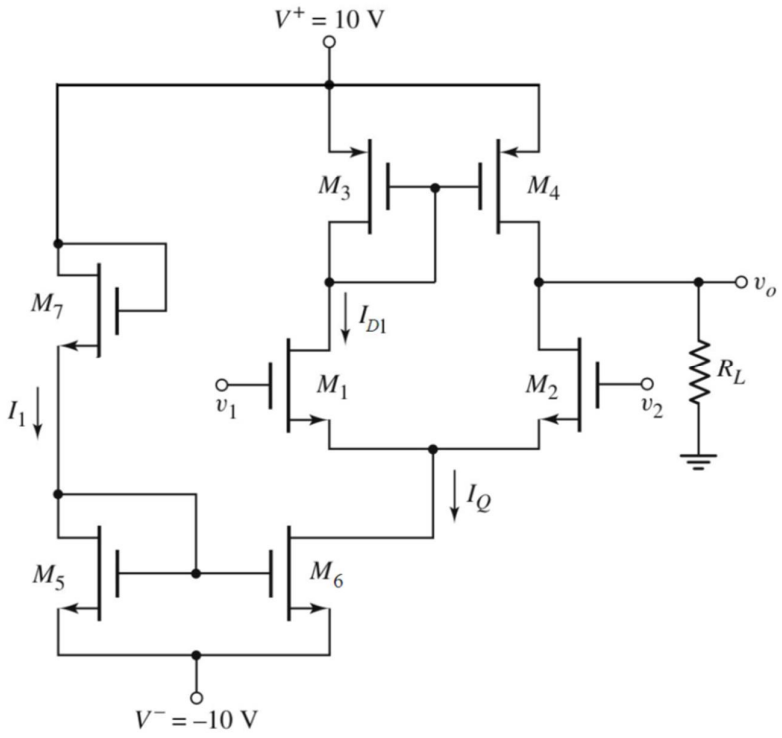

Figure 2

Answers for Question 2(b)

QUESTION 3 [20 marks]

The circuit in **Figure 3** shows a simple multi-stage BJT op-amp, **consisting of 3 different stages** and bias circuit. It is given that V_{BE}**(on) = 0.6 V,** V_A **= 120 V,** and β **= 120 for all transistors**. **Assume** $I_{C7} = I_Q$ **= 45 µA. Also, the output voltage,** v_o **= 0V for** $v_1 = v_2$ **= 0V.**

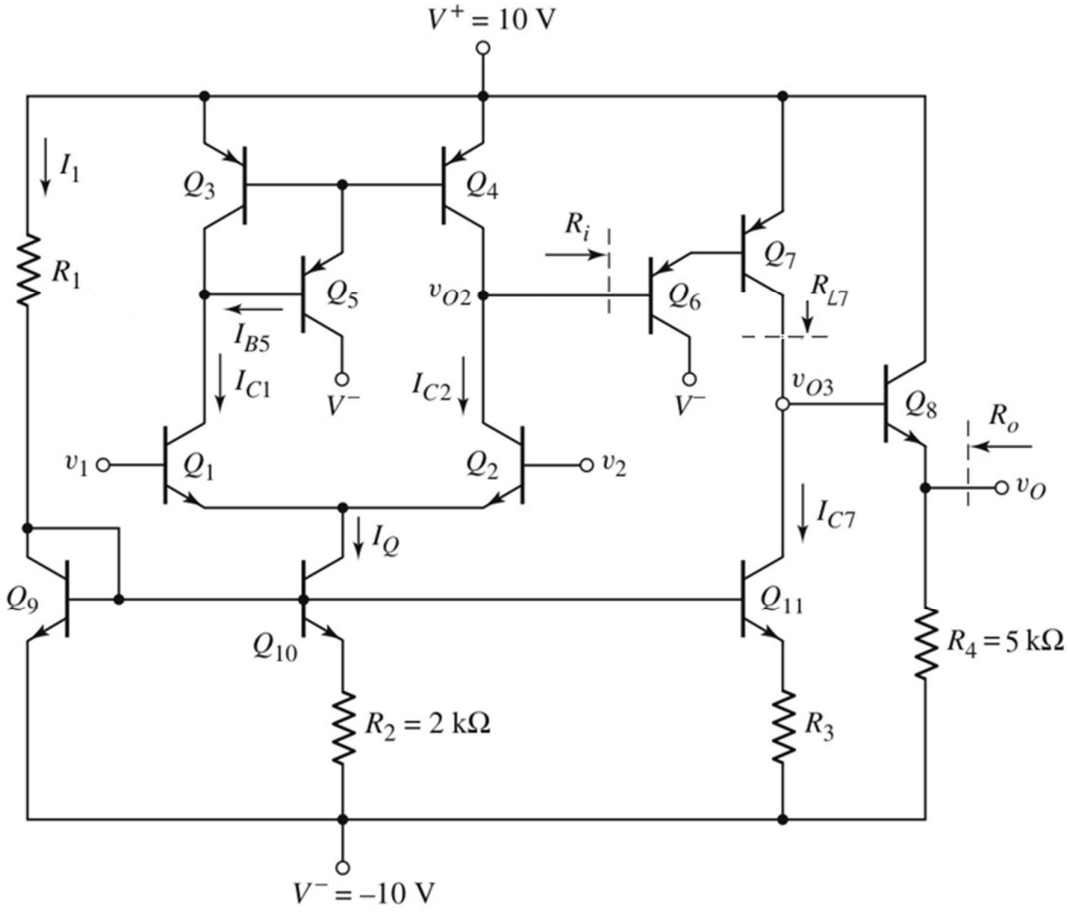

Figure 3

(a) **Calculate** the input resistance (R_i) and the load resistance (R_{L7}) for **the Darlington Pair** in the gain stage as indicated in the **Figure 3.** [15 marks]

(b) **Calculate** the voltage gain of the gain stage (A_2), where $A_2 = v_{O3}/v_{O2}$ is derived from the following relationships:

$$v_{O3} = I_{C7}\,(r_{o7} \parallel R_{L7})$$

$$v_{O2} = I_{B6}\,R_i$$ [5 marks]

Answers for Question 3

QUESTION 4 [15 marks]

(a) **Compare** the performance of both **Class-A** and **Class-B** output stages in terms of **power conversion efficiency, η**. [3 marks]

(b) Consider the **Class-A emitter-follower** circuit shown in **Figure 4**. Study the **Figure 4 thoroughly**. Assume all transistors are matched with V_{BE}**(on) = 0.6 V**, V_{CE}**(sat) = 0.2 V**, and $V_A = \infty$**. Neglect** base currents.

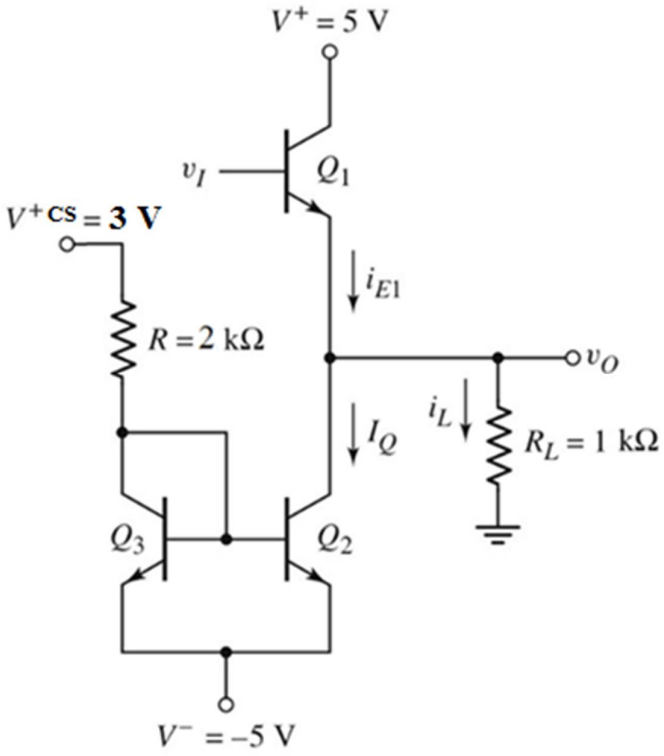

Figure 4

(i) **Find** the value of I_Q. [2 marks]

(ii) For v_O **= 0 V**, **calculate** the power dissipated individually in transistor Q_1, Q_2, and Q_3, and also the power dissipated in resistor R. [6 marks]

(iii) **Determine** the power conversion efficiency (η) for a symmetrical sine-wave output voltage (v_O) with peak value of **4 V**. [4 marks]

Answers for Question 4

This is extra page for answers. Please indicate question number clearly.