COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER I   2010/2011

PROGRAMME   : Bachelor of Electrical & Electronics Engineering (Honours) &
                     Bachelor of Electrical Power Engineering (Honours)

SUBJECT CODE   : EEEB273

SUBJECT   : ELECTRONIC ANALYSIS AND DESIGN II

DATE   : 31 October 2010

TIME   : 9.00 am – 12.00 pm (**3 hours**)

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INSTRUCTIONS TO CANDIDATES:

1.   This question paper contains **Six** (6) questions in **Twelve** (12) pages.

2.   Answer **ALL** questions.

3.   Write **all** answers in the answer booklet provided.

4.   Write answer to each question on **a new page**.

5.   For all calculations, assume that V_T **= 26 mV**.

6.   Write all your answers using pen. **DO NOT USE PENCIL** except for the
        diagram

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THIS QUESTION PAPER CONSISTS OF 12 PRINTED PAGES INCLUDING
THIS COVER PAGE.

Question 1   [16 marks]

(a) **Figure 1a** shows a pnp current source with transistor parameters $\beta = \infty$, $V_A = 450$ **V**, and V_{EB}(on) = **0.7 V**. Study **Figure 1a** carefully.

   (i)   **Design** the circuit such that I_{REF} = **1.5 mA.**

[3 marks]

   (ii)   **What** is the value of I_O?

[3 marks]

   (iii) **Find** the output resistance (R_O) of the current source.
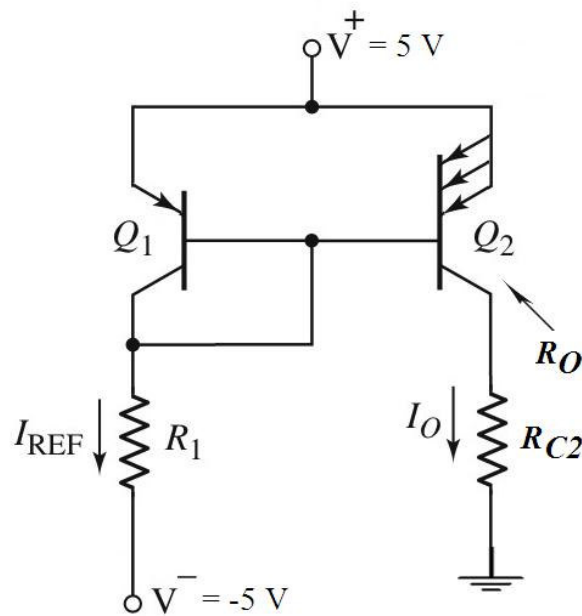
[2 marks]

Figure 1a

(b) For a MOSFET current source shown in **Figure 1b**, find the width-to-length ratio (**W/L**) for all the transistors in the circuit. Given I_{REF} = **100 μA**, I_O = **60 μA**, and V_{DS2} (**sat**) = **0.4 V**. Transistor parameters are k'_n = **100 μA/V^2**, V_{TN} = **0.4 V** and λ = **0.**
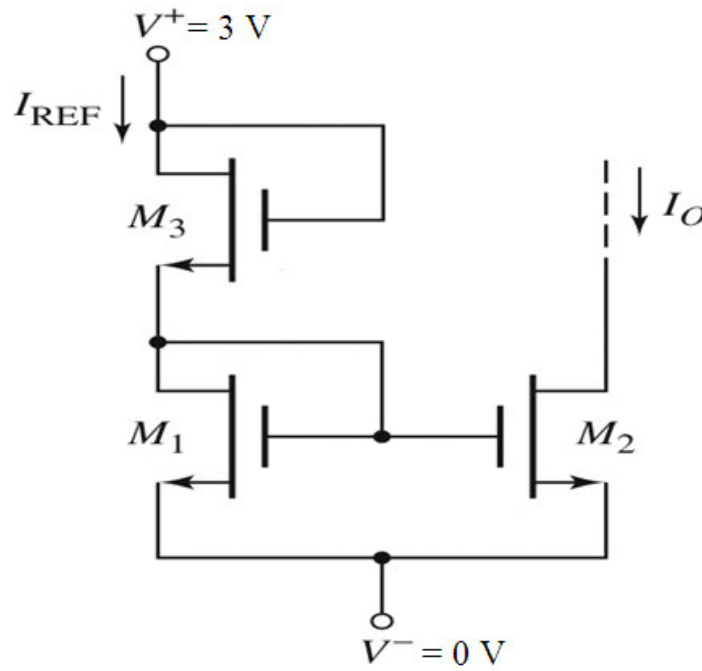
[8 marks]

Figure 1b

Question 2   [18 marks]

(a)   Consider the BJT differential amplifier in **Figure 2a**. The circuit and transistor parameters are $V^+ = 10$ V, $V^- = -10$ V, $\beta = 100$, $V_T = 26$ mV, $I_Q = 1$ mA, and early voltage $V_A = \infty$.

   (i)   **Redesign** the circuit such that the differential-mode output voltage of $v_{c2} = 8$ V when a differential-mode input voltage of $v_d = 0.05$ V is applied.

[4 marks]

   (ii)   **Determine** the differential-mode input resistance.

[2 marks]

   (iii)   **Determine** the **CMRR** when the common-mode voltage gain (A_{cm}) = -0.2

[2 marks]

   (iv)   **Suggest** a practical method to increase the differential-mode voltage gain, **draw** the suggested circuit diagram.

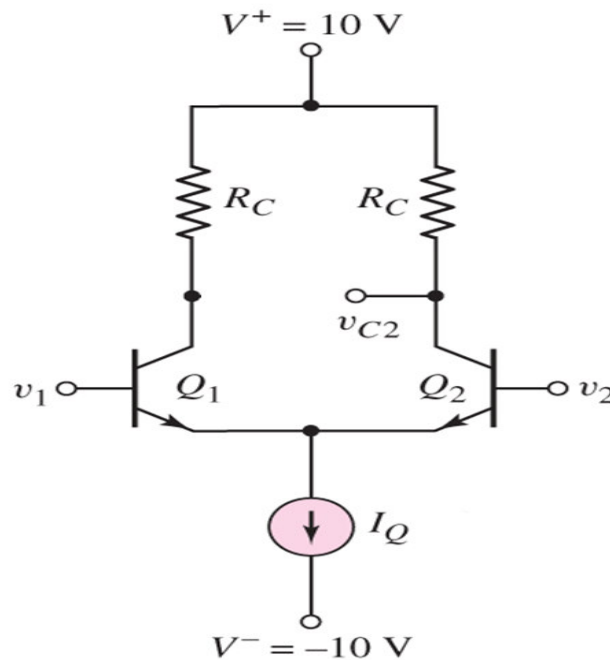[3 marks]

Figure 2a

(b) The MOSFET differential amplifier with cascode active load shown in **Figure 2b** is to be designed to achieve the desired differential-mode voltage gain. The circuits parameters are to be **V$^+$ = 10 V**, **V$^-$ = -10 V**, and **I$_Q$ = 0.4 mA**. The **NMOS** transistors parameters are λ_n = **0.02 V^{-1}**, k'_n = **100 μA/V^2**, V_{TN} = **1 V** and transconductance g_m = **0.5 mA/V**. The **PMOS** transistors parameters are λ_p = **0.01 V^{-1}**, k'_p = **200 μA/V^2**, V_{TP} = **-1 V** and the transconductance g_m = **0.5 mA/V**.

(i) **Determine** the output resistance of the amplifier.

[4 marks]

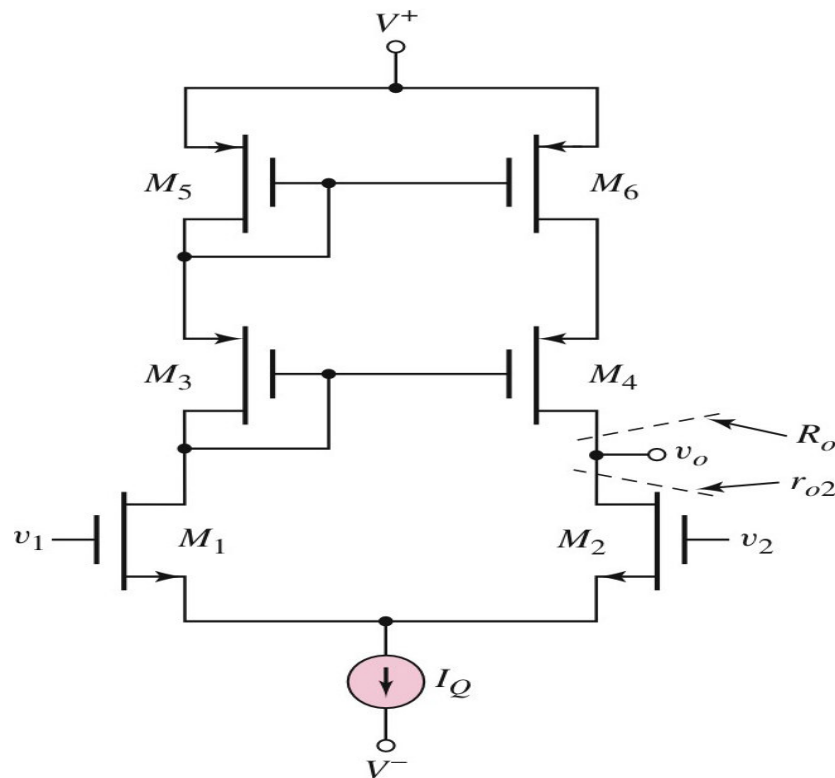(ii) **Determine** the differential-mode voltage gain.

[3 marks]

Figure 2b

Question 3   [16 marks]

Consider the circuit shown in **Figure 3**. The circuit and transistor parameters are V^+ = 12 V, V^- = -12 V, V_{GS4} = 3.37 V, $\lambda = \infty$, K_n = 0.2 mA/V², and V_{TN} = 1 V.

(i)   **Calculate** the output voltage v_{O2} and v_{O3}.

[6 marks]

(ii)   **Calculate** the overall voltage gain (v_{O3}/v_d).

[6 marks]

(iii)   **Determine** V_{GS2} and the maximum common-mode input voltage (v_{CM}(**max**)) of M_2.
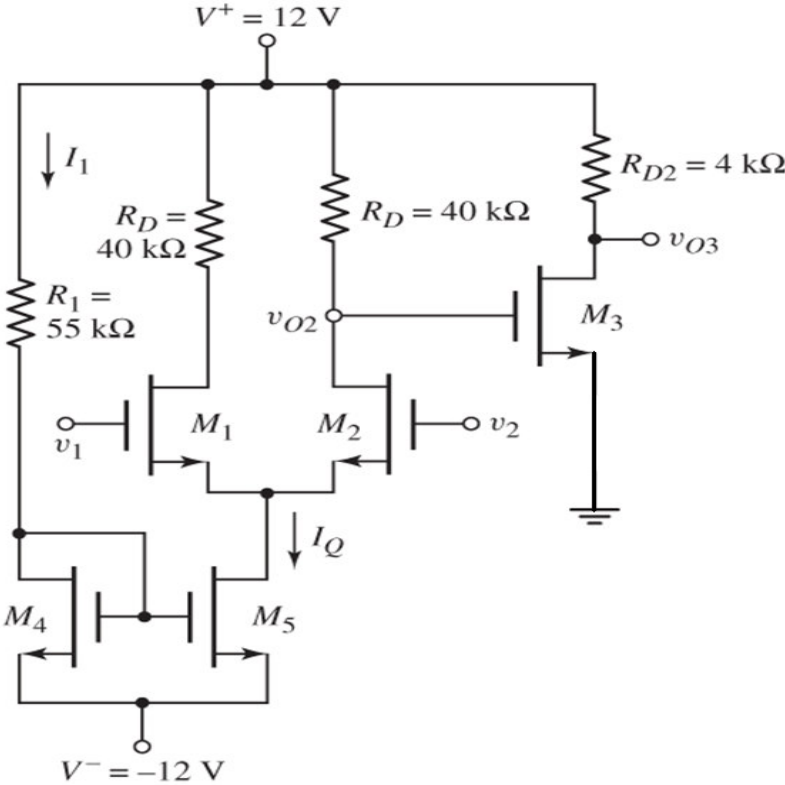
[4 marks]

Figure 3

Question 4   **[17 marks]**

(a)   **Figure 4a** shows a basic complimentary push-pull output stage circuit. Assume the B-E cut-in voltage of **0.6 V** such that v_O remains zero for the interval **-0.6 V $\leq v_I \leq$ 0.6 V**.

     (i)   **Sketch** the voltage transfer characteristic of the circuit. Indicate when Q_n is conducting and when it is not conducting.

                         [3 marks]

     (ii)   **Sketch** the current i_{Cn} for two input cycles corresponds to a sinusoidal input voltage $v_I = V_p \, sin \, \omega t$ **(V)**.

                         [4 marks]
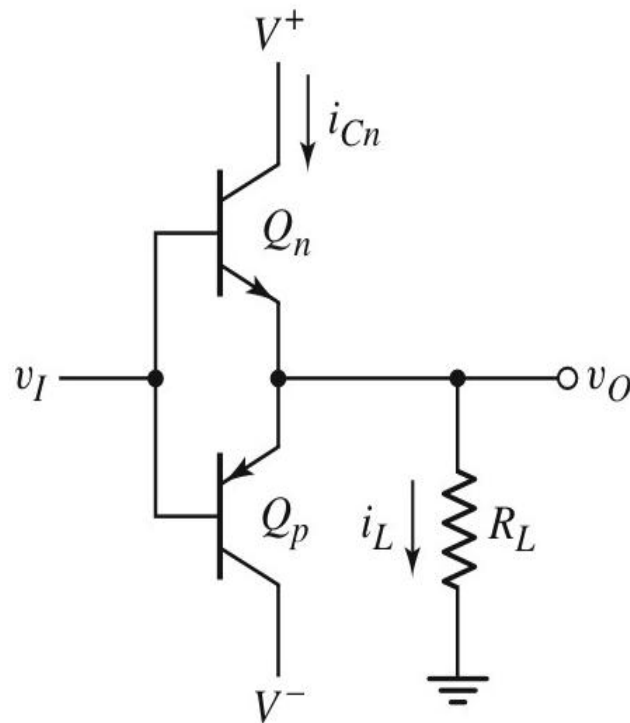
Figure 4a

(b) Consider the circuit in **Figure 4b**. The circuit parameters are $V_{CC} = 12$ V, $R_L = 100\Omega$, and Q_n and Q_p are matched with $I_S = 4\times10^{-13}$ A. Let $V_{BB} = 1.2$ V, and $\beta \gg 1$.

(i) For the case of the input voltage $v_I = 0$, calculate the quiescent collector currents, i_{Cn} and i_{Cp}, and the power dissipated in transistors Q_p and Q_n.

[3 marks]

(ii) What is the maximum amplitude of the output voltage, v_O, and the corresponding maximum power that can be delivered to the load?

[2 marks]

(iii) For the case of $v_O = -4 \sin \omega t$ (V), determine i_L, i_{Cn}, i_{Cp}, and v_I.
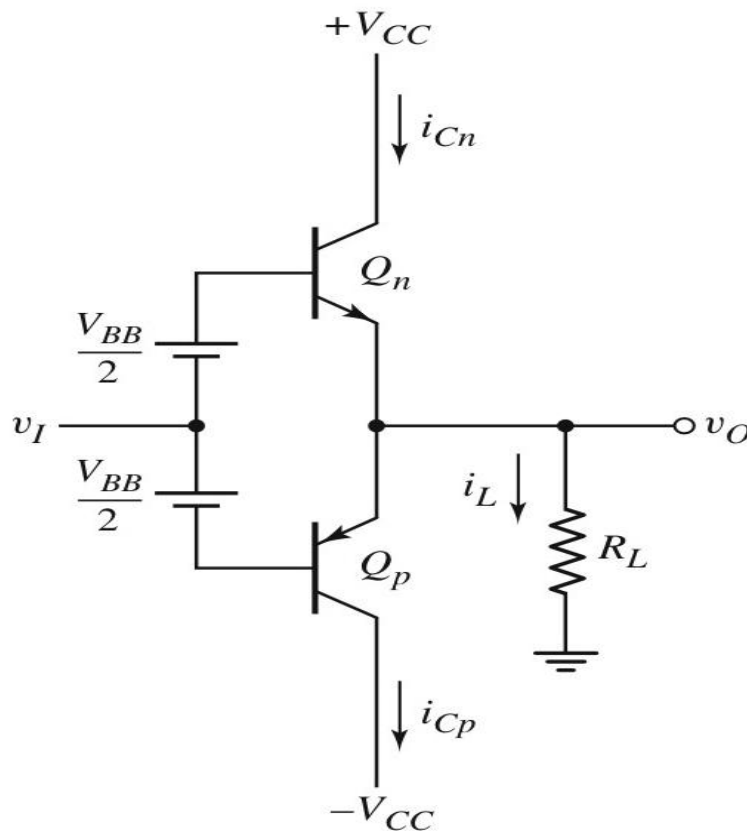
[5 marks]

Figure 4b

Question 5   [17 marks]

(a) **Figure 5a** shows reference circuit and gain stage of **741 op-amp**. Transistors Q_{12} and Q_{13} form a current mirror, and Q_{13B} has a scale factor **0.70** times that of Q_{12}. I_{REF} is given as **0.72 mA**. Assume $V_{BE} = 0.6$ V and $\beta = 200$ for npn transistors. Find I_{C16}.
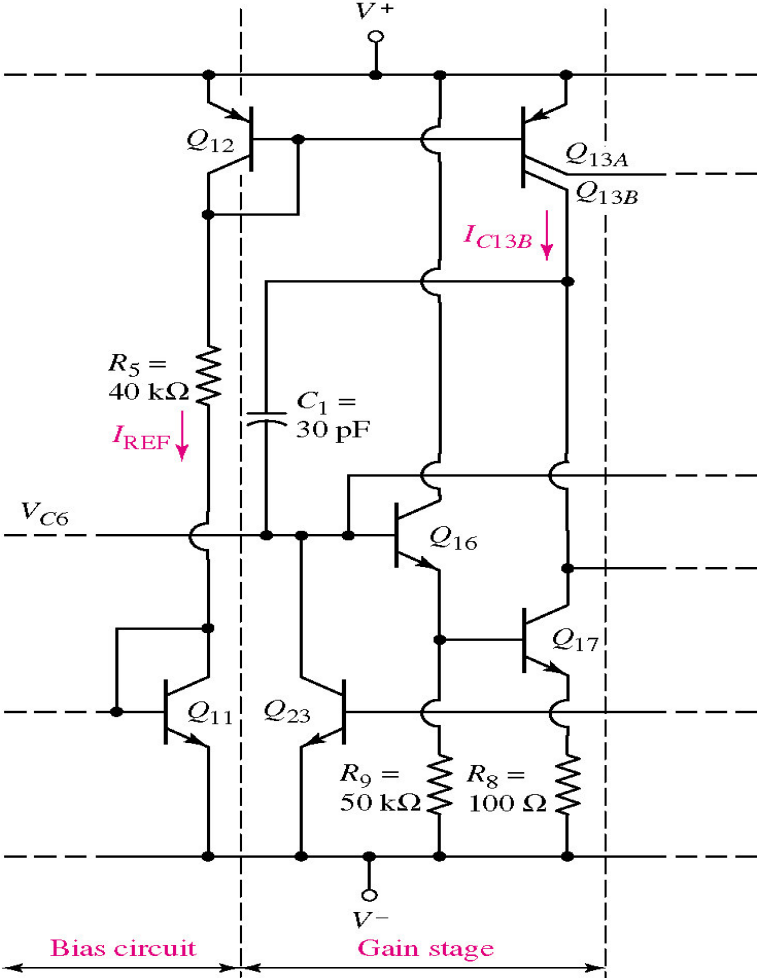
[7 marks]

Figure 5a

(b) A simple CMOS op-amp circuit as shown in **Figure 5b** is biased with $I_Q =$ **200 μA**. The transistor parameters are $k'_n = $ **100 μA/V²**, $k'_p = $ **40 μA/V²**, $V_{TN} = $ **0.4 V**, $V_{TP} = $ **-0.4 V**, and $\lambda_n = \lambda_p = $ **0**. The transistor width-to-length ratios are $(W/L)_1 = (W/L)_2 = $ **20**, $(W/L)_3 = $ **50**, and $(W/L)_4 = $ **40**.

    (i)   **Design** the circuit (i.e. find the values of R_{D1}, R_{D2}, and R_S) such that $I_{D3} = $ **150 μA**, $I_{D4} = $ **200 μA**, and $v_o = $ **0** for $v_1 = v_2 = $ **0.**

[6 marks]

    (ii)   Find the overall small-signal voltage gain if the gain of the gain stage is **-19.21**.

[4 marks]

Figure 5b

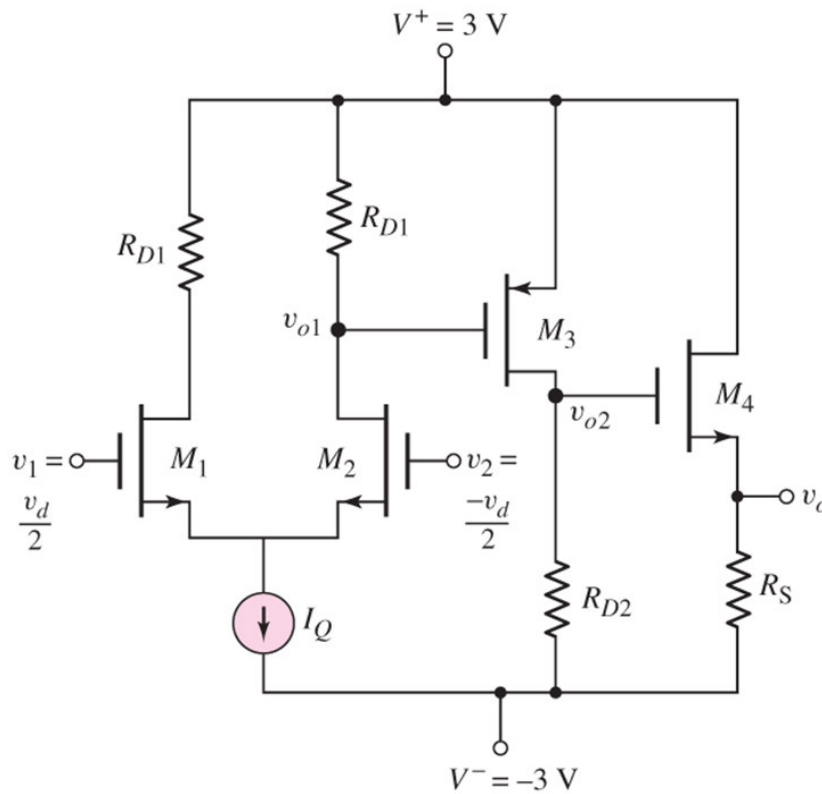## Question 6   [16 marks]

(a)   **State** four **(4)** applications of an ideal operational amplifier.

[4 marks]

(b)   A general output equation for a difference amplifier is

$$v_O = A_d v_d + A_{cm} v_{cm}$$

For the difference amplifier in **Figure 6a**, the circuit parameters are $R_1 = R_3 = 10 \ k\Omega$, $R_2 = 100 \ k\Omega$, and $R_4 = 110 \ k\Omega$ and the output voltage equation is as follows:

$$v_O = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4/R_3}{1 + R_4/R_3}\right)v_{I2} - \left(\frac{R_2}{R_1}\right)v_{I1}$$

where $v_{I1} = v_{cm} - \dfrac{v_d}{2}$

and $v_{I2} = v_{cm} + \dfrac{v_d}{2}$

Find A_d, A_{cm}, and calculate the **CMRR in dB**.
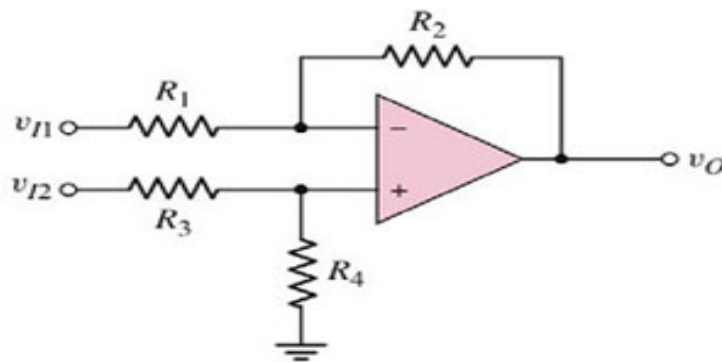
[6 marks]

Figure 6a

(c) Consider the two inverting op-amp circuit connected in cascade as shown in **Figure 6b**. Let $R_1 = 20$ kΩ, $R_2 = 160$ kΩ, $R_3 = 10$ kΩ, and $R_4 = 80$ kΩ. Find v_O/v_I for the circuit.
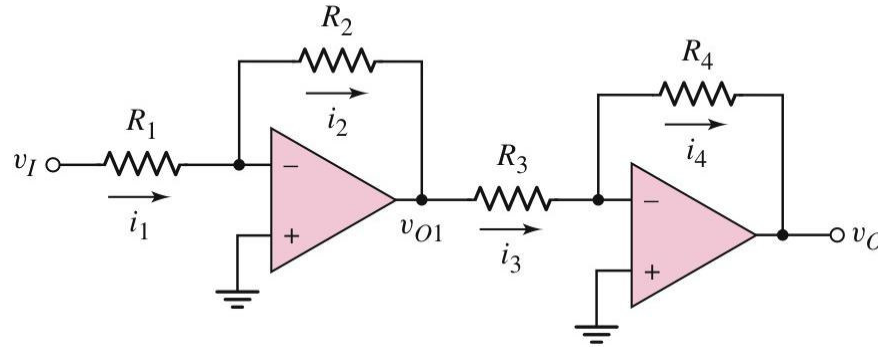
[6 marks]

Figure 6b

-END OF QUESTION PAPER-