COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER II 2010 / 2011

SUBJECT CODE : **EEEB273**

SUBJECT : **ELECTRONIC ANALYSIS AND DESIGN II**

DATE : March 2011

-- MODEL ANSWERS --

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **Four** (4) questions in **Seven** (7) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided.
4. Write answer to each question on **a new page**.
5. For all calculations, assume that V_T **= 26 mV**.

THIS QUESTION PAPER CONSISTS OF 7 PRINTED PAGES INCLUDING THIS COVER PAGE.

Question 1 [15 marks]

(a) For a BJT two-transistor current source, the transistor parameters are:

$V_{BE(on)}$**=0.7 V,** β**=120,** and V_{AN}**=100 V**. The bias voltage is V^+=5V and V^-= -5V.

(i) **Design** the circuit such that I_o **= 0.50mA** when V_{CE2}=0.7 V.

(ii) What is the **change in** I_o as V_{CE2} varies between 0.7 V and 7 V?

[8 marks]

Answers:

(i) $I_{REF} = I_o\left[1+\frac{2}{\beta}\right]\left[\frac{1+\frac{V_{CE2}}{V_A}}{1+\frac{V_{CE2}}{V_A}}\right] = 0.51\ mA$ [2]

$R_1 = \frac{V^+ - V_{BE(on)} - V^-}{I_{REF}} = 18.24k\Omega$ [2]

(ii) $\frac{\Delta I_O}{\Delta V_{CE2}} = \frac{1}{r_o}$ [1]

$r_o = \frac{V_A}{I_{CQ}} = \frac{V_A}{I_o} = 200k$ [2]

$\Delta I_o = \frac{6.3}{200k}$=31.5μA [1]

(b) Refer to **Figure 1**. All the transistors are identical. The transistor parameters are: **β=200, V_A=∞, $V_{BE(on)}$= 0.7 V**. **Calculate V_{CE4}.**

Hint: The current source equation is $I_{REF} = I_O\,(1+[2/\beta(1+\beta_3)])$.

[7 marks]

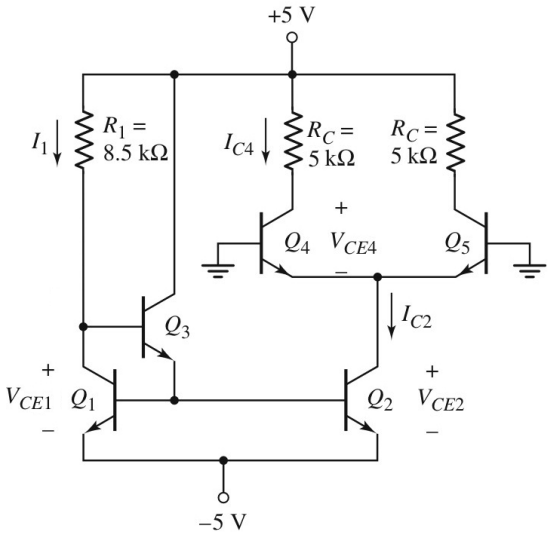


Figure 1

Answer:

$I_1 = [V^+ - V^- - 2V_{BE(on)}]/R1 = [5-(-5)-2(0.7)]/8.5k = 1.0118$ mA [2]

$I_{C2} = 1.0118$ mA [1]

$V_{E4} = 0 - V_{BE4} = -0.7$V [1]

$I_{C4} = ½\ I_{C2} = 0.5050$ mA [1]

$V_{CE4} = V^+ - I_{C4}R_C - V_{E4} = 5-(0.506)(5)-(-0.7) = 3.17$ V [2]

Question 2 [15 marks]

(a) **Describe how** class-A, class-B, and class-AB output stages are different?

[3 marks]

Answers:

(i) Class-A, class-B, and class-AB output stages are different according to the percent (%) of time the output transistors are conducting (**turned on**), as follows:

- **Class A:** Output transistor is ***biased*** *at a quiescent current* $\boldsymbol{I_Q}$ and conducts for the ***entire cycle*** *of the input signal.* [1]
- **Class B**: Output transistor conducts for only ***one-half*** *of each sine-wave input cycle.* [1]
- **Class AB:** Output transistor **biased** *at a small quiescent current* $\boldsymbol{I_Q}$, and conducts for ***slightly more than half*** *a cycle.* [1]

(b) **A class-A emitter follower** biased with a constant-current source is shown in **Figure 2**. Study **Figure 2** carefully. The transistor parameters are: $\boldsymbol{\beta = 200}$, $\boldsymbol{V_{BE} = 0.7\ V}$, and $\boldsymbol{V_{CE}}$(sat) **= 0.2V**. Neglecting base currents:

(i) **Find** the value of $\boldsymbol{I_Q}$. [3 marks]

(ii) **Determine** the value of $\boldsymbol{R}$ that will produce the maximum possible output signal swing. [4 marks]

(iii) **Calculate** the power conversion efficiency ($\boldsymbol{\eta}$). [5 marks]

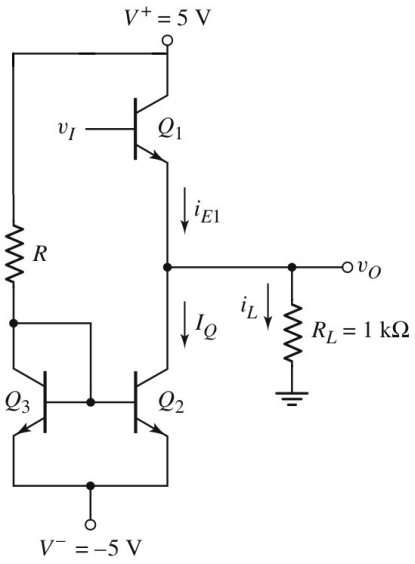


Figure 2

Answers:

(i) The value of I_Q is equivalent to the amplitude of the largest negative load current, $i_L = v_{o(min)}/R_L$

$v_{o(min)} = V^- + V_{CE(sat)} = (-5) + (0.2) = -4.8V$ [1.5]

$I_Q = i_{L(max)} = (4.8)/1k = 4.8mA$ [1.5]

(ii) $R = (V^+ - V^- - V_{BE})/I_{REF}$ [1]

$I_{REF} = (1+ 2/\beta)\ I_Q = (1+2/200)(4.8m) = 4.848mA$ [2]

$R = (5-(-5)-0.7)/(4.848m) = 1.9183k\Omega$ [1]

(iii) $\eta = P_L / P_S$ [1]

$P_L = ½ (V_p)^2 / R_L = (½)(4.8)^2/ (1k) = 11.52mW$ [1.5]

$P_S = 2V_{CC}I_Q = 2(5)(4.8m) = 48mW$ [1.5]

$\eta = (11.52 / 48)$ x 100% = 24% [1]

Question 3 [25 marks]

Figure 3 shows a differential amplifier circuit with active loads and current source. The active load transistors are matched with parameters K_p **= 0.1 mA/V^2,** V_{TP} **= -2 V** and λ_p **= 0.02 V^{-1}**. Transistors M_1 and M_2 are driven into saturation with V_{DS}(sat) **= 1.12 V**. Transistors M_5, M_6 and M_7 are identical. All the NMOS transistors have the same K_n **= 0.2 mA/V^2**, V_{TN} **= 2 V**, and λ_n **= 0.015 V^{-1}**.

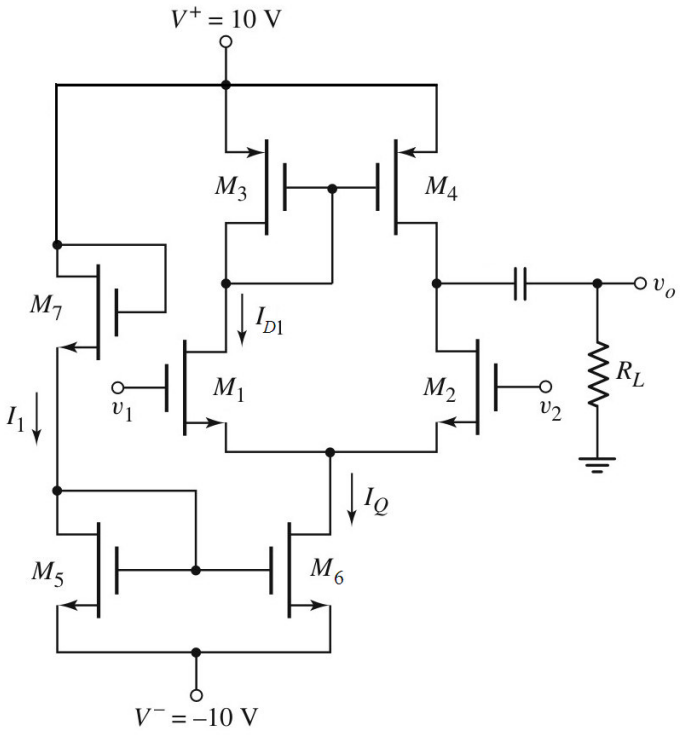


Figure 3

(i) Determine I_1, I_Q, and I_{D1} when $v_1 = v_2 = 0$. [8 marks]

(ii) Determine the **one-sided differential mode voltage gain** for this differential amplifier if R_L **= 100 kΩ**. [10 marks]

(iii) It is required that the **CMRR** of this circuit to be **55dB**. What is the common mode voltage gain? [3 marks]

(iv) Suggest ways to improve the CMRR for the circuit in **Figure 3**.[4 marks]

Answers:

(i) $I_1=K_n(V_{GS5}-V_{TN})^2 = K_n(V_{GS7}-V_{TN})^2$ [2]

$V_{GS5} = V_{GS7}$ [1]

$V_{GS5} + V_{GS7} = 2\ V_{GS5} = V^+-V^- = 10-(-10) = 20V$ [1.5]

$V_{GS5} = 10V = V_{GS7}$ [0.5]

$I_1 = (0.2m)(10-2)^2 = 12.8mA$ [1]

$I_Q = I_1 = 12.8mA$ [1]

$I_{D1} = ½I_Q = 6.4mA$ [1]

(ii) $v_o = (g_m/2)v_dR_o$ therefore $A_d = (g_m/2)R_o$ [1.5]

$R_{o(diff\ amp)} = r_{o2}//r_{o4}//R_L$ [1]

$r_{o2} = 1/(\lambda_n I_{D1}) = 1/(0.02)(6.4m) = 7.812k\Omega$ [1.5]

$r_{o4} = 1/(\lambda_p I_{D1}) = 1/(0.015)(6.4m) = 10.417k\Omega$ [1.5]

$R_{o(diff\ amp)} = (7.812k)//(10.417k)//(100k) = 4.273\ k\Omega$ [1.5]

$g_m = 2\sqrt{(K_nI_{D1})}$ [1]

$A_d = (1/2) \times [2\sqrt{(K_nI_{D1})}] \times R_{o(diff\ amp)}$ [1]

$= [(0.2m)(6.4m)]^{½}\ (4.273k) = 4.834$ [1]

(iii) $CMRR = 20 \log [A_d/A_{cm}] = 55dB$ [1]

$A_{cm} = A_d / [\log^{-1}(55/20)] = 8.6\times10^{-3}$ [2]

(iv) Select two answers:

Increase the current source output resistance. [2]

Increase the diff amp output resistance by using cascode active loads. [2]

Reduce the loading effect by increasing load resistance, R_L. [2]

Question 4 [20 marks]

A simple bipolar op-amp is designed as shown in **Figure 3a**. *Note that biasing for amplifiers in the circuit is provided by two-transistor current mirrors*. Study the figure carefully. Neglect base currents. Assume parameters for all transistors are: V_{BE}**(on) =** 0.7V, β **= 100,** and $V_A = \infty$.

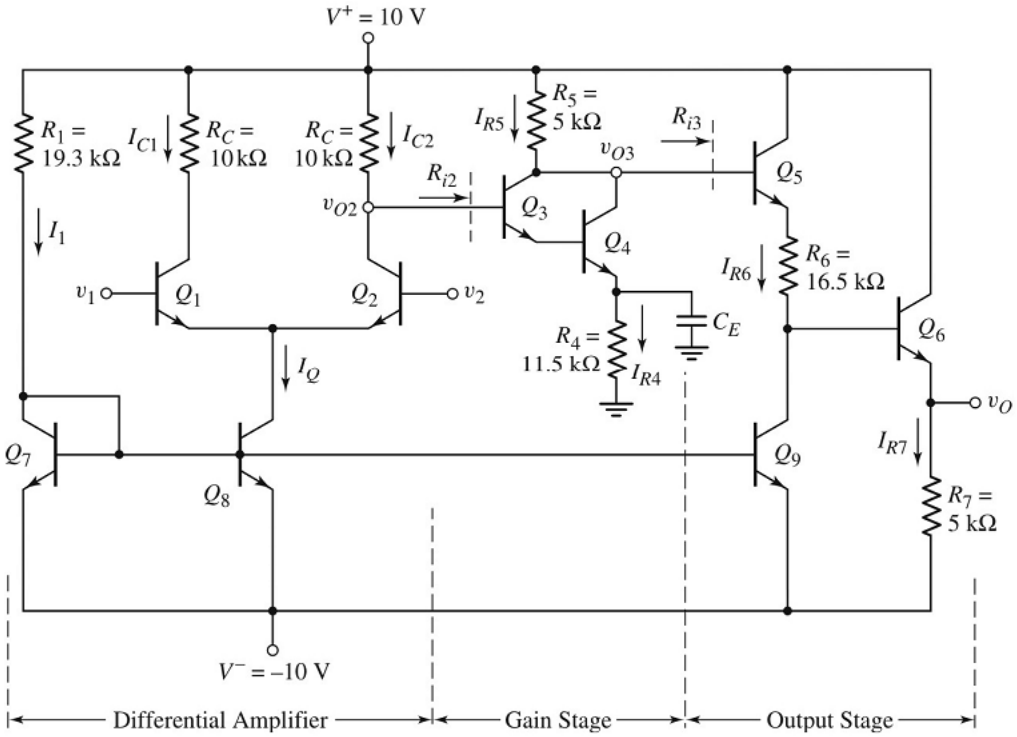


Figure 3a

(i) Referring to **Figure 3a** find I_1, I_Q, I_{C2}, v_{O2}, and v_{O3}. [10 marks]

(ii) With small-signal analysis values for A_{d1}, $r_{\pi 3}$, R_{i2}, and A_2 can be found using the following formula:

$$A_{d1} = \left(\frac{V_{o2}}{v_d}\right) = \frac{g_m}{2}\left(R_C \| R_{i2}\right)$$

$$r_{\pi 3} \cong \beta r_{\pi 4}$$

$$R_{i2} = r_{\pi 3} + (1+\beta) r_{\pi 4}$$

$$A_2 \cong \frac{I_{R4}}{2V_T}\left(R_5\right)$$

Calculate A_{d1}, A_2, and the total overall small-signal voltage gain, A_d**.**

[10 marks]

Answers:

(i)

I_1	$= (V^+ - V_{BE7} - V^-) / (R_1)$		[1]
	$= (10\text{-}0.7\text{-}(-10)) / (19.3\text{k})$	$= 1$ mA	[1]
I_Q	$= I_1 / (1 + 2/\beta)$	$= 0.9084$ mA	[2]
I_{C2}	$= I_Q / 2$	$= 0.4902$ mA	[2]
v_{O2}	$= V^+ - I_{C2} R_C = 10 - (0.4902\text{m})(10\text{k}) = 5.098$ V		[2]
I_{R4}	$= (v_{O2} - 2 V_{BE}(\text{on})) / (R_4)$		
	$= (5.098 - 1.4) / (11.5\text{k})$	$= 0.322$ mA	[1/2]
I_{R5}	$\approx I_{R4}$ (neglecting base currents)	$= 0.322$ mA	[1/2]
v_{O3}	$= V^+ - I_{R5} R_5 = 10 - (0.322\text{m})(5\text{k}) = 8.39$ V		[1]

OR	I_Q	$\approx I_1$ [Since $\beta >> 1$]	$= 1$ mA	[2]
	I_{C2}	$= I_Q / 2$	$= 0.5$ mA	[2]
	v_{O2}	$= V^+ - I_{C2} R_C = 10 - (0.5\text{m})(10\text{k}) = 5$ V		[2]
	I_{R4}	$= (v_{O2} - 2 V_{BE}(\text{on})) / (R_4)$		
		$= (5 - 1.4) / (11.5\text{k})$	$= 0.313$ mA	[1/2]
	I_{R5}	$\approx I_{R4}$ (neglecting base currents)	$= 0.313$ mA	[1/2]
	v_{O3}	$= V^+ - I_{R5} R_5 = 10 - (0.313\text{m})(5\text{k}) = 8.44$ V		[1]

(ii)

Using	$I_{C2} = 0.4902$ mA, $I_{R4} = 0.322$ mA:	
A_{d1}	$= (g_m / 2)(R_C \parallel R_{i2})$	
g_m	$= I_{C2} / V_T = (0.4902\text{mA})/(26\text{mV}) = 18.85$ mA/V	[1]
$r_{\pi 4}$	$= \beta V_T / I_{R4} = (100\text{x}26\text{m})/(0.322\text{m}) = 8.085$ kΩ	[1]
$r_{\pi 3}$	$\approx \beta\, r_{\pi 4} = 808.5$ kΩ	[1]
R_{i2}	$= r_{\pi 3} + (1 + \beta)\, r_{\pi 4}$	
	$= 808.5\text{k} + (101)(8.085\text{k}) = 1621.1$ kΩ	[1]
A_{d1}	$= (18.85\text{m}/2)(10\text{k} \parallel 1621.1\text{k}) = 93.67$	[2]
A_2	$\approx (I_{R4} / 2V_T)\, R_5 = (0.322\text{m}/(2\text{x}26\text{m}))(5\text{k}) = 30.96$	[2]
A_3	≈ 1	[1]
A_d	$= A_{d1} A_2 A_3 = 93.67 \text{ x } 30.96 \text{ x } 1 = 2900$	[1]

OR	Using	$I_{C2} = 0.5$ mA, $I_{R4} = 0.313$ mA:	
	A_{d1}	$= (g_m / 2)(R_C \parallel R_{i2})$	
	g_m	$= I_{C2} / V_T = (0.5\text{mA})/(26\text{mV}) = 19.23$ mA/V	[1]
	$r_{\pi 4}$	$= \beta V_T / I_{R4} = (100\text{x}26\text{m})/(0.313\text{m}) = 8.306$ kΩ	[1]
	$r_{\pi 3}$	$\approx \beta\, r_{\pi 4} = 830.6$ kΩ	[1]
	R_{i2}	$= r_{\pi 3} + (1 + \beta)\, r_{\pi 4}$	
		$= 830.6\text{k} + (101)(8.306\text{k}) = 1669.5$ kΩ	[1]
	A_{d1}	$= (19.23\text{m}/2)(10\text{k} \parallel 1669.5\text{k}) = 95.58$	[2]
	A_2	$\approx (I_{R4} / 2V_T)\, R_5 = (0.313\text{m}/(2\text{x}26\text{m}))(5\text{k}) = 30$	[2]
	A_3	≈ 1	[1]
	A_d	$= A_{d1} A_2 A_3 = 95.58 \text{ x } 30 \text{ x } 1 = 2867$	[1]

Question 5 [25 marks]

(a) The summing amplifier as in **Figure 5a** can be used as a digital-to-analog converter (DAC). The analogue output is calculated by using the equation:

$$v_o = -R_F\left[\frac{a_3}{R_3} + \frac{a_2}{R_2} + \frac{a_1}{R_1} + \frac{a_0}{R_0}\right](V_R)$$

Suppose that we want to convert a 4-bit binary signal ($a_3a_2a_1a_0$) to its equivalent weight in decimal value. **Design** the circuit such that when switch S_3 only is closed (i.e. resistor R_3 is connected to -5V supply), then $a_3 = 1$, thus an input $a_3a_2a_1a_0 = 1000$ will give $v_O = 8V$. Similarly, when all switches (i.e. S_0, S_1, S_2, and S_3) are closed, the binary signal $a_3a_2a_1a_0$ combination gives $v_O = 15V$. Referring to the **Table 1**, verify your design by showing that $a_3a_2a_1a_0$ combination provides the same output as shown.

[12 marks]

Table 1

$a_3a_2a_1a_0$	1000	0100	0010	0001	0110
v_O [Volts]	8	4	2	1	6

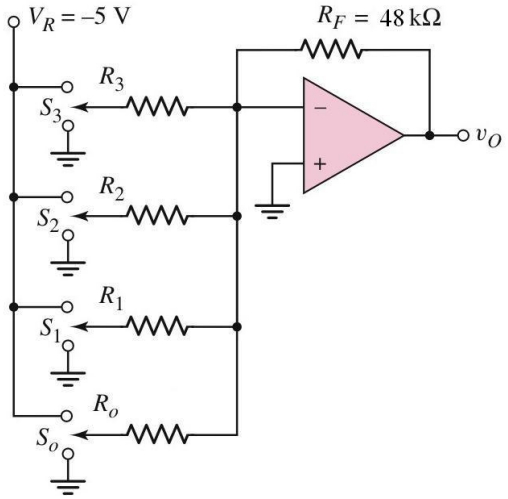


Figure 5a

Answer:

When S_3 is closed:

$v_O = -R_F[(1/R_3) +(0/R_2) +(0/R_1) +(0/R_0)](V_R)$ [2]

$v_O = -48k\ (1/R_3)(-5) =8$ [1]

$R_3 = (48k)(5)/8 =30k\Omega$ [1]

When S_2 is closed:

$v_O = -R_F(1/R_2)(V_R)$ [0.5]

$v_O = -48k\ (1/R_2)(-5) =4$ [0.5]

$R_2 = (48k)(5)/4 =60k\Omega$ [1]

When S_1 is closed:

$v_O = -R_F(1/R_1)(V_R)$ [0.5]

$v_O = -48k\ (1/R_1)(-5) =2$ [0.5]

$R_1 = (48k)(5)/2 =120k\Omega$ [1]

When S_0 is closed:

$v_O = -R_F(1/R_0)(V_R)$ [1]

$v_O = -48k\ (1/R_0)(-5) =1$

$R_0 = (48k)(5) =240k\Omega$ [1]

Verify: 0110 = 6V [2]

$v_O = -R_F[(0/R_3) +(1/R_2) +(1/R_1) +(0/R_0)](V_R)$

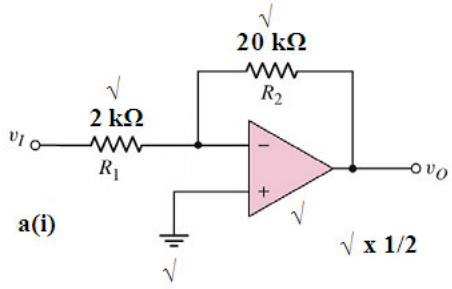
$v_O = -48k[(1/60k) +(1/120k)](-5) = (240/60) +(240/120) =6V$

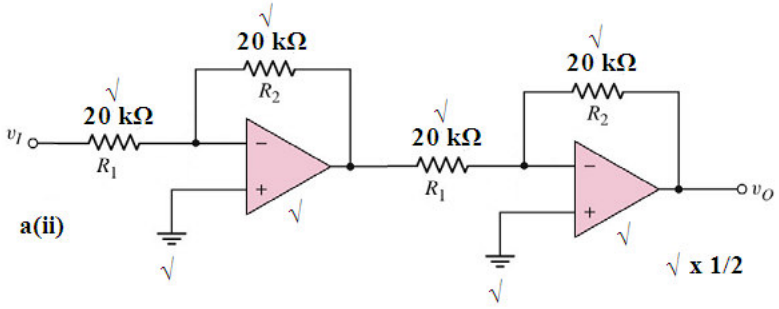
(b) With **feedback resistor** of **20 kΩ**, **sketch** the following circuits using **inverting op-amp** configuration.

(i) An inverting amplifier with a closed-loop gain of **-10**. [2 marks]

(ii) A voltage follower. [4 marks]

Answer:





(c) **Find** the voltage gain, A_v, for the op-amp in **Figure 5b**. Assume the op-amp is ideal. [7 marks]

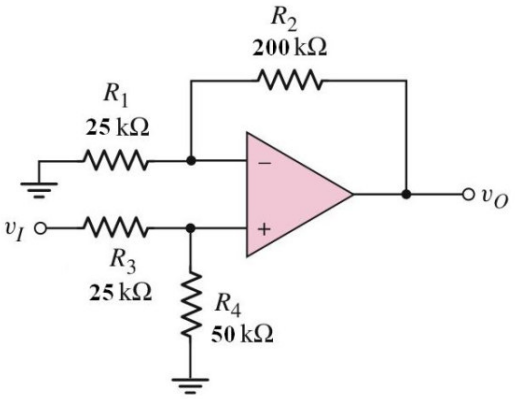


Figure 5b

Answer:

$v_O = (1+R_2/R_1)v_2$ [2]

$v_2 = [R_4/(R_3+R_4)]v_I$ [1]

$v_O = (1+R_2/R_1)\,[R_4/(R_3+R_4)]v_I$ [1]

$A_v = v_O/v_I = (1+R_2/R_1)\,[R_4/(R_3+R_4)]$ [1]

$= [1+(200k/25k)][50k/(50k+25k)] = (9)(2/3) = 6$ [2]