COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 2 2010 / 2011

PROGRAMME	**: Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	**: EEEB273**
SUBJECT	**: ELECTRONIC ANALYSIS AND DESIGN II**
DATE	**: March 2011**
TIME	**: 9.00 am – 12.00 pm (3 hours)**

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **Five** (5) questions in **Seven** (7) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided.
4. Write answer to each question on **a new page**.
5. For all calculations, assume that V_T **= 26 mV**.

THIS QUESTION PAPER CONSISTS OF SEVEN (7) PRINTED PAGES INCLUDING THIS COVER PAGE.

Question 1 [15 marks]

(a) For a **BJT two-transistor current source**, the transistor parameters are: $V_{BE}(\text{on}) = 0.7$ V, $\beta = 120$, and $V_{AN} = 100$ V. The bias voltage is $V^+ = 5$ V and $V^- = -5$V.

(i) **Design** the circuit such that $I_o = 0.50$mA when $V_{CE2} = 0.7$ V. [4 marks]

(ii) What is the **change in** I_o as V_{CE2} varies between 0.7 V and 7 V? [4 marks]

(b) Refer to **Figure 1**. All the transistors are identical. The transistor parameters are: $\beta = 200$, $V_A = \infty$, $V_{BE}(\text{on}) = 0.7$ V. **Calculate** V_{CE4}. [7 marks]

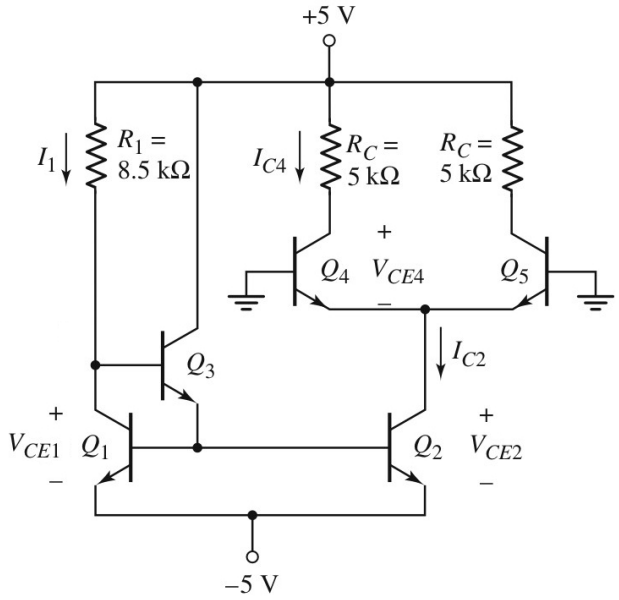

Figure 1

Hint: The current source equation is $I_{REF} = I_O\,(1+[2/\beta(1+\beta_3)])$.

Question 2 [15 marks]

(a) **Describe how** class-A, class-B, and class-AB output stages are different?

[3 marks]

(b) **A class-A emitter follower** biased with a constant-current source is shown in **Figure 2**. Study **Figure 2** carefully. The transistor parameters are: $\boldsymbol{\beta = 200}$, $\boldsymbol{V_{BE} = 0.7\ V}$, and $\boldsymbol{V_{CE}}$(sat) **= 0.2V**. Neglecting base currents:

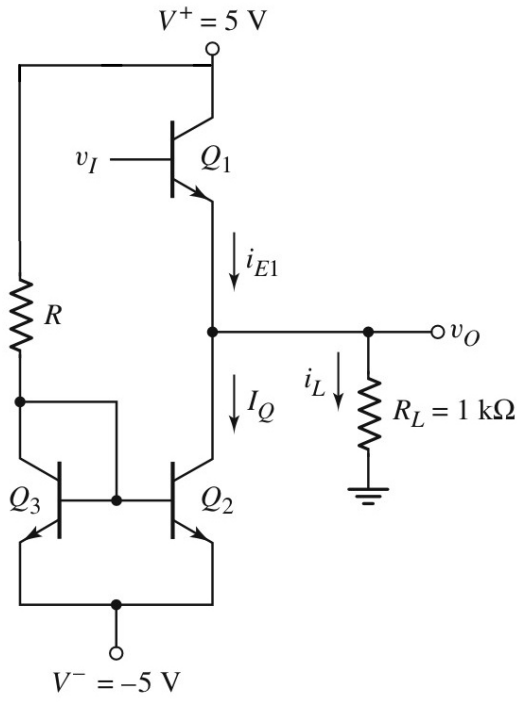

Figure 2

(i) **Find** the value of $\boldsymbol{I_Q}$. [3 marks]

(ii) **Determine** the value of $\boldsymbol{R}$ that will produce the maximum possible output signal swing. [4 marks]

(iii) **Calculate** the power conversion efficiency ($\boldsymbol{\eta}$). [5 marks]

Question 3 [25 marks]

Figure 3 shows a differential amplifier circuit with active loads and current source. The active load transistors are matched with parameters K_p **= 0.1 mA/V^2,** V_{TP} **= -2 V** and λ_p **= 0.02 V^{-1}**. Transistors M_1 and M_2 are driven into saturation with V_{DS}(sat) **= 1.12 V**. Transistors M_5, M_6 and M_7 are identical. All the NMOS transistors have the same K_n **= 0.2 mA/V^2**, V_{TN} **= 2 V**, and λ_n **= 0.015 V^{-1}**.

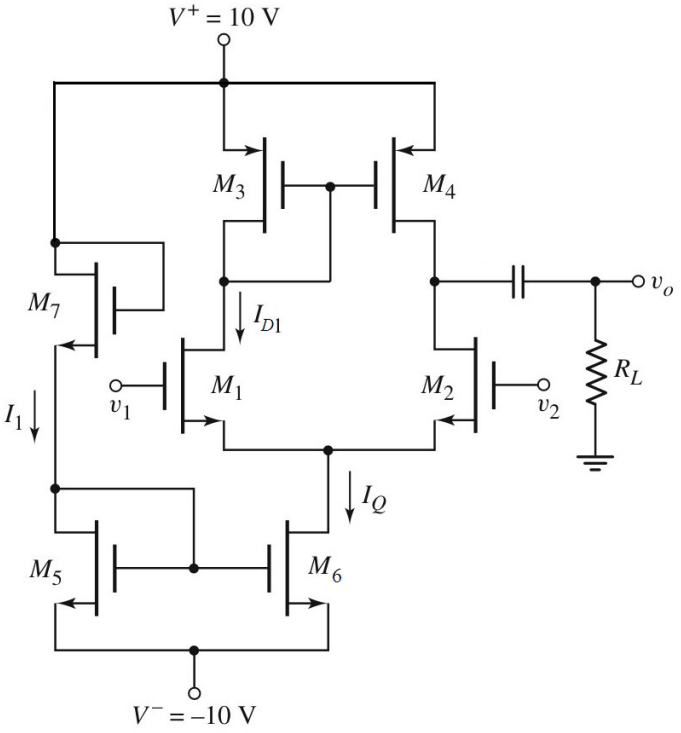

Figure 3

(i) Determine I_1, I_Q, and I_{D1} when $v_1 = v_2 = 0$. [8 marks]

(ii) Determine the **one-sided differential mode voltage gain** for this differential amplifier if R_L **= 100 kΩ**. [10 marks]

(iii) It is required that the **CMRR** of this circuit to be **55dB**. **Find** the common mode voltage gain. [3 marks]

(iv) Suggest ways to improve the CMRR for the circuit in **Figure 3**. [4 marks]

Question 4 [20 marks]

A simple bipolar op-amp is designed as shown in **Figure 4**. *Note that biasing for amplifiers in the circuit is provided by* ***two-transistor current mirrors***. Study the figure carefully. Neglect base currents. Assume parameters for all transistors are: V_{BE}**(on) = 0.7 V**, β **= 100,** and $V_A = \infty$.

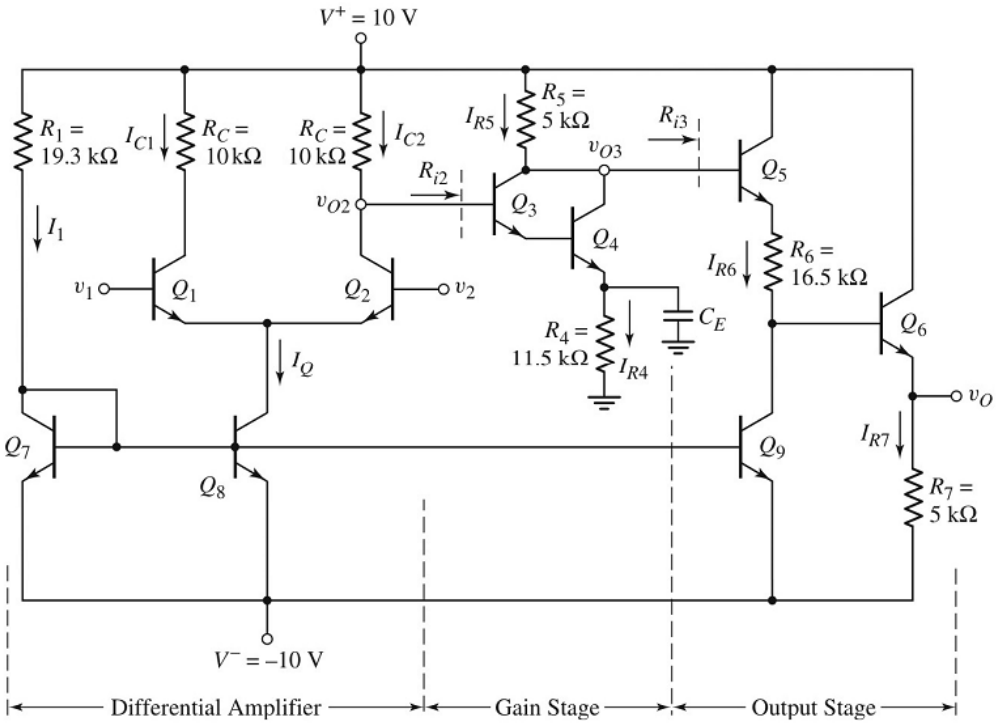

Figure 4

(i) Referring to **Figure 4** find I_1, I_Q, I_{C2}, v_{O2}, and v_{O3}. [10 marks]

(ii) With small-signal analysis values for A_{d1}, $r_{\pi 3}$, R_{i2}, and A_2 can be found using the following formula:

$$A_{d1} = \left(\frac{V_{o2}}{v_d}\right) = \frac{g_m}{2}\left(R_C \| R_{i2}\right)$$

$$r_{\pi 3} \cong \beta r_{\pi 4}$$

$$R_{i2} = r_{\pi 3} + (1+\beta) r_{\pi 4}$$

$$A_2 \cong \frac{I_{R4}}{2V_T}\left(R_5\right)$$

Calculate A_{d1}, A_2, and the total overall small-signal voltage gain, A_d.

[10 marks]

Question 5 [25 marks]

(a) The summing amplifier as in **Figure 5a** can be used as a digital-to-analog converter (DAC). The analogue output is calculated by using the equation:

$$v_o = -R_F\left[\frac{a_3}{R_3}+\frac{a_2}{R_2}+\frac{a_1}{R_1}+\frac{a_o}{R_o}\right](V_R)$$

Suppose we want to convert a 4-bit binary signal ($a_3a_2a_1a_0$) to its equivalent weight in decimal. **Design** the circuit such that when switch S_3 only is closed (i.e. resistor R_3 is connected to **-5 V** supply), then a_3 **= 1**, thus an input $a_3a_2a_1a_0$ **= 1000** will give v_O **= 8V**. Similarly, when all switches (i.e. S_0, S_1, S_2, and S_3) are closed, the binary signal $a_3a_2a_1a_0$ combination gives v_O **= 15V**. Referring to the **Table 1**, verify your design by showing that $a_3a_2a_1a_0$ combinations provide the same output as shown.

[12 marks]

Table 1

$a_3a_2a_1a_0$	**1000**	**0100**	**0010**	**0001**	**0110**
v_O [Volts]	8	4	2	1	6

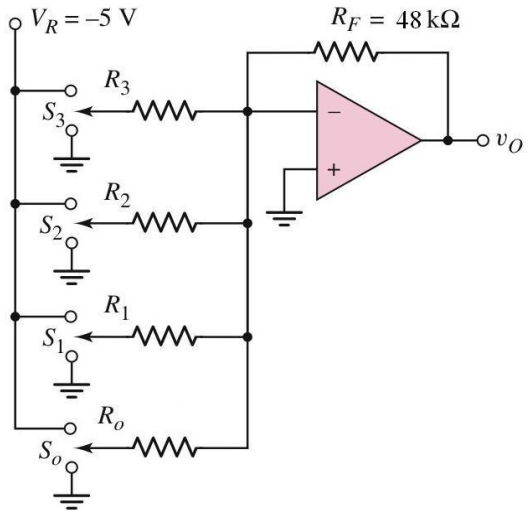

Figure 5a

(b) With **feedback resistor** of **20 kΩ**, **sketch** the following circuits using **inverting op-amp** configuration:

(i) An inverting amplifier with a closed-loop gain of **-10.** [2 marks]

(ii) A voltage follower. [4 marks]

(c) **Find** the voltage gain, $\mathbf{A_v}$, for the op-amp in **Figure 5b**. Assume the op-amp is ideal. [7 marks]

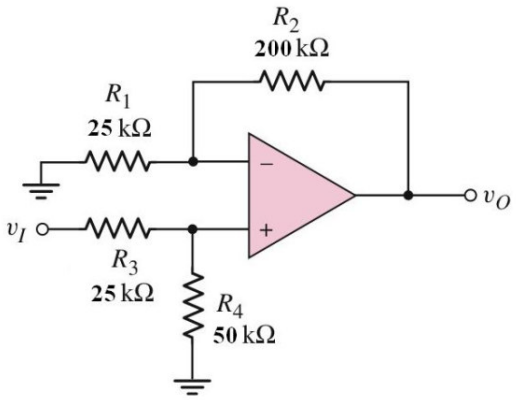

Figure 5b

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