COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 1 2011 / 2012

PROGRAMME	**: Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	**: EEEB273**
SUBJECT	**: ELECTRONIC ANALYSIS AND DESIGN II**
DATE	**: August 2011**
TIME	**: 3 hours**

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **Six** (6) questions in **Ten** (10) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided.
4. Write answer to each question on **a new page**.
5. For all calculations, assume that V_T **= 26 mV**.

THIS QUESTION PAPER CONSISTS OF TEN (10) PRINTED PAGES INCLUDING THIS COVER PAGE.

Question 1 [16 marks]

(a) **Referring** to the circuits in **Figure 1a**, the transistors in the circuit are identical.

(i) For the circuit in **Figure 1a (i)**, **show** that $I_{REF} \approx (1+4/\beta)\, I_O$. Label the currents which you use in your equations correctly. (Hints: You may start with I_{E3} and I_{E4} relationship given in the circuit. Note that $I_{B3} \neq I_{B4}$. Assume $\beta^2 >> 1$).

[4 marks]

(ii) For the circuit in **Figure 1a (ii)**, **simplify the circuit and draw** the simplified circuit. Using the simplified circuit, **derive** the ratio of V_x / I_x. Assume that $r_{\pi 4} << r_{O2}$.

[4 marks]

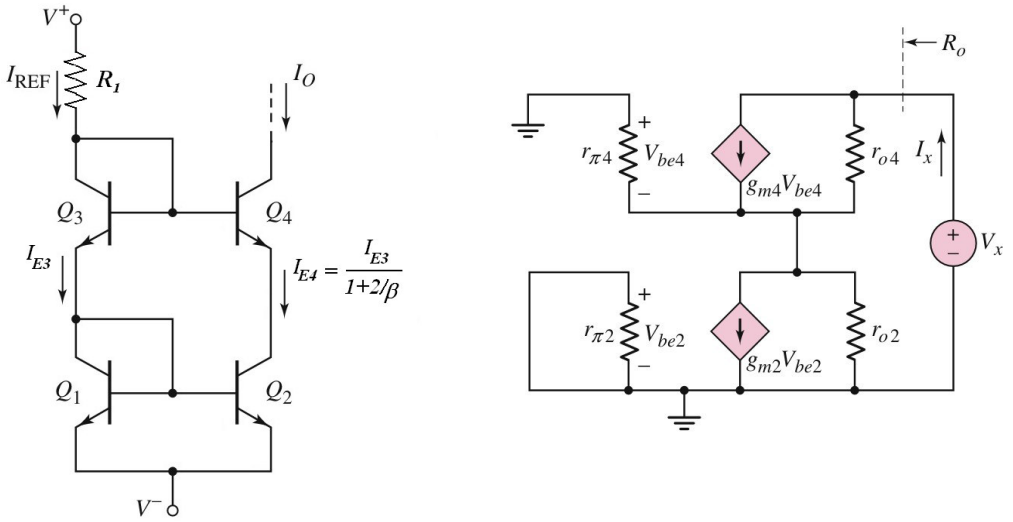

Figure 1a (i) BJT Cascode Current Source, and **(ii)** The Small Signal Equivalent Circuit.

(b) The MOSFET current source circuit in **Figure 1b** has transistor parameters k'_n **= 80 µA/V^2** and V_{TN} **= 0.5 V**. **Design** the current source so that I_O **= 50µA** when I_{REF} **=150µA** and V_{D2} at **-1.2V**. [8 marks]

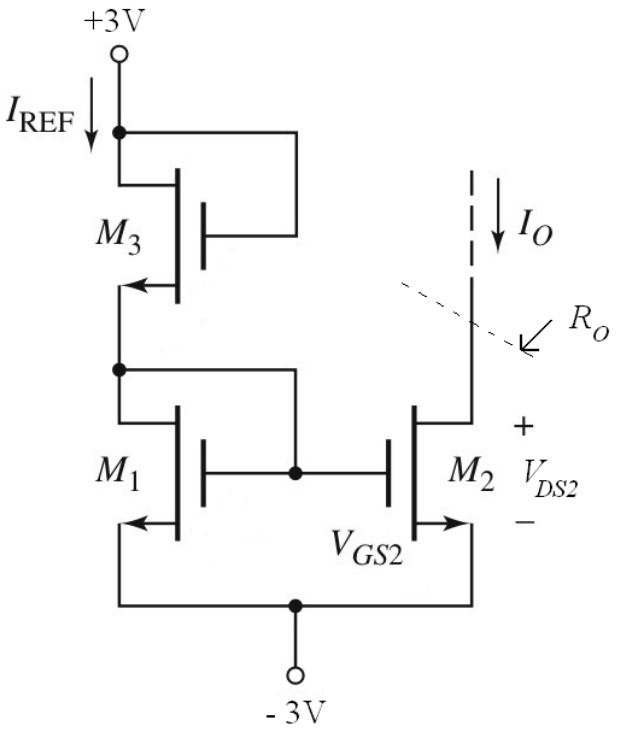

Figure 1b

Question 2 [16 marks]

Consider the circuit shown in **Figure 2**. The bias voltages are **+3 V** and **-3 V**. The transistor parameters are $K_{n1} = K_{n2} = 150\ \mu A/V^2$, $K_{n3} = K_{n4} = 100\ \mu A/V^2$, and $V_{TN} = 0.3$ V for all transistors.

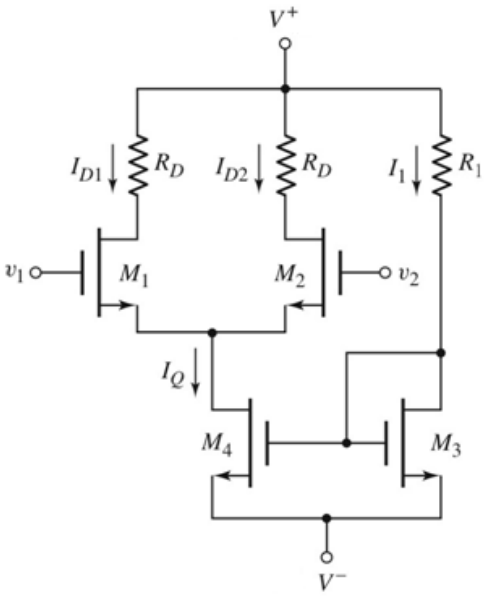

Figure 2

(a) **Calculate** R_1 and R_D for the diff-amp circuit such that $V_{DS1} = V_{DS2} = 3$ V and $I_{D1} = I_{D2} = 60$ **µA** when $v_1 = v_2 = -1.5$ V. [8 marks]

(b) Input v_1 and v_2 are changed from $v_1 = v_2 = -1.5$ V to $v_1 = v_2 = +1.05$ V. **Calculate** change in V_{DS4} (i.e. ΔV_{DS4}). [4 marks]

(c) Given that $\lambda_1 = \lambda_2 = 0$ and $\lambda_3 = \lambda_4 = 0.01\ V^{-1}$. **Calculate** the change in I_Q (i.e. ΔI_Q) using result from **part (b)**. [4 marks]

Question 3 [16 marks]

(a) The differential amplifier shown in **Figure 3a** has a three-transistor current mirror connected as an active load. The circuit is connected to power supply voltages of $V^+ = +5$ **V** and $V^- = -5$ **V**.

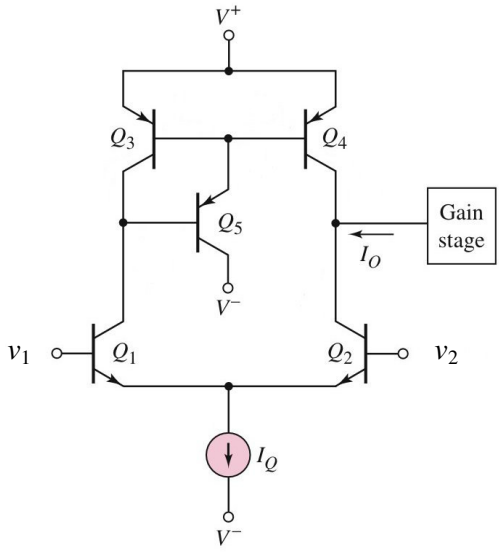

Figure 3a

(i) The dc currents in the BJT differential amplifier must be balanced such that $I_{B5} = I_O$. **Explain** why this is important in a BJT circuit. [2 marks]

(ii) **Determine** the relationship between I_O and I_Q such that the amplifier dc currents are balanced. **Calculate** the value of I_O given that $I_Q = 0.2$ **mA** and $\beta = 100$.

[5 marks]

(b) The circuit in **Figure 3b** shows a simple multistage BJT op-amp, **consisting of four different stages**. It is given that for all transistors, β**=100**.

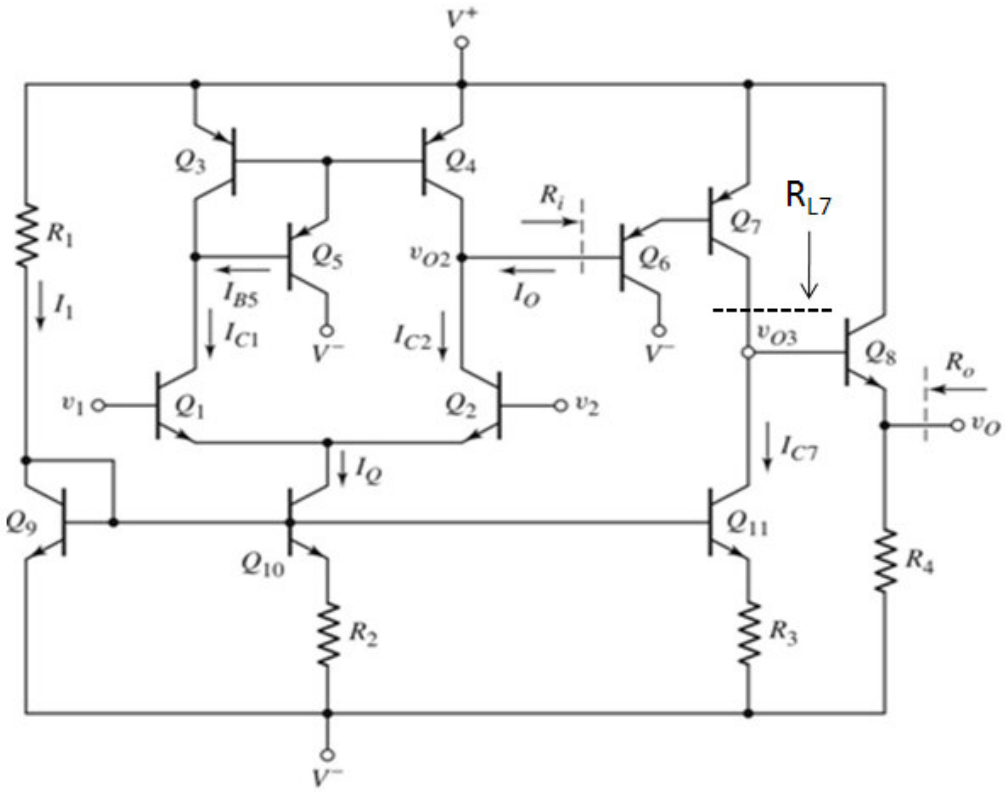

Figure 3b

(i) **Name** the four stages in the circuit, and **indicate** which transistors and resistors belonging to each stage. [4 marks]

(ii) Assuming that for all transistors: r_o **= 500 kΩ,** g_m **= 5 mA/V,** r_π **= 3 kΩ,** R_3 **= 250 Ω,** and R_4 **=10 kΩ**. For Q_7, the **Early voltage** V_A is assumed to be infinite. **Calculate the small signal input impedance** at the collector of Q_7, i.e. R_{L7} as indicated in the **Figure 3b**. [5 marks]

Question 4 [16 marks]

The folded cascode CMOS op-amp in **Figure 4** is biased such that I_{REF} **= 50 µA**. The circuit is connected to supply voltages of V^+ **= +5 V** and V^- **= -5 V**. It is given that the transistor parameters are k'_n **= 40 µA/V²**, k'_p **= 20 µA/V²**, λ_n **= 0.005 V⁻¹**, λ_p **= 0.01 V⁻¹**, and $|V_T|$ **= 1 V**. The transistor aspect ratios are $(W/L)_{1,2,5,6}$ **= 10,** $(W/L)_{3,4,11,12,13}$ **= 5,** and $(W/L)_{7,8,9,10}$ **= 20**.

(a) **Determine** the dc currents in each transistor in the circuit. [3 marks]

(b) **Determine** the differential-mode voltage gain of the op-amp. [8 marks]

(c) **Redesign** the **folded cascode differential amplifier, M_1 and M_2**, such that the differential-mode voltage gain of the op-amp is **twice** of that calculated in **part (b)**. [5 marks]

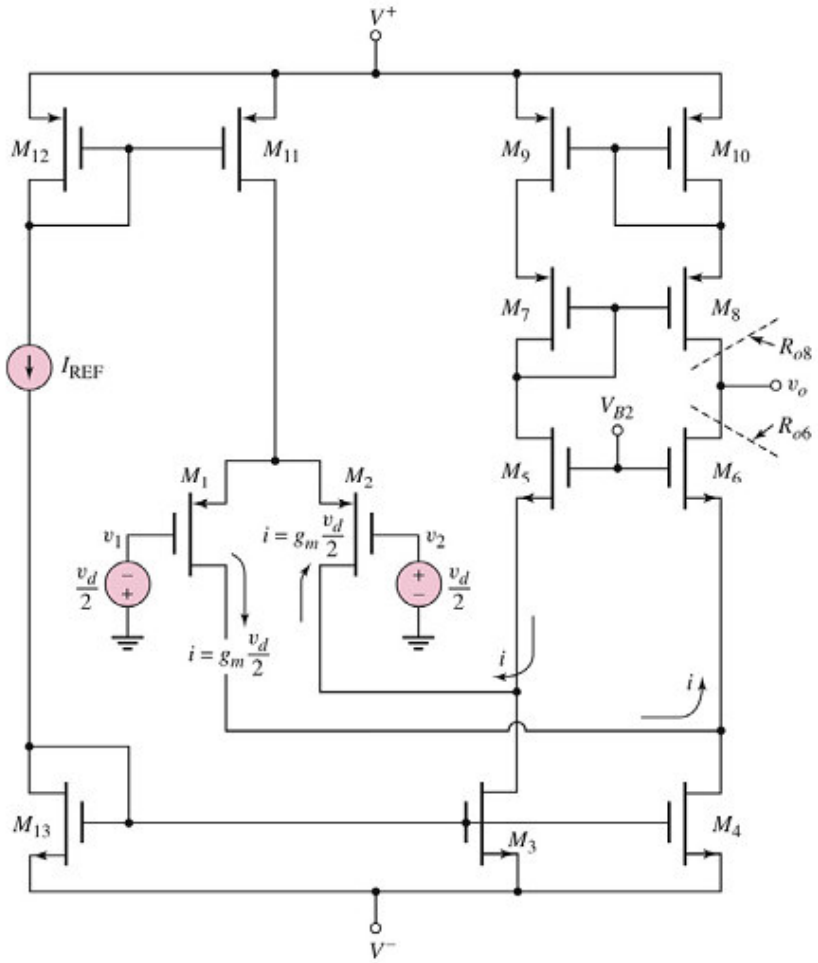

Figure 4

Question 5 [16 marks]

Figure 5 shows the output stage for 741 op-amp. Study the **Figure 5** carefully.

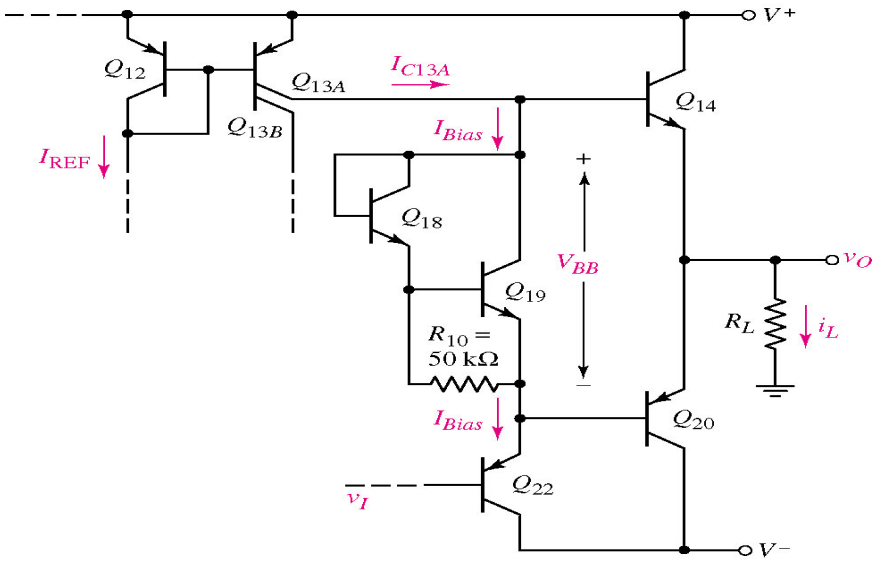

Figure 5

(a) **Describe** the operation of an **approximate (i.e. non-ideal) class-B output stage**. Assume V_{BEN}**(on) =** V_{EBP}**(on) = 0.6 V**. You may use appropriate diagrams to help your explanation. [4 marks]

(b) **What** is the class of the output stage (which consists of transistors Q_{14} and Q_{20}) used in the **Figure 5**? [2 marks]

(c) **Describe** how **quiescent bias current** for the output transistors Q_{14} and Q_{20} in **Figure 5** is established. [2 marks]

(d) **What** is the advantage of the output stage given in the **Figure 5** compared to an **approximate (i.e. non-ideal) class-B output stage**? [2 marks]

(e) For the output stage in the **Figure 5**, assume that reverse saturation currents $I_{S18} = I_{S19} = 10^{-14}$ **A**. Using $\beta_n = 200$, we can assume that $I_C \approx I_E$ for Q_{18} and Q_{19}. Given that $I_{Bias} = 0.18$ **mA**. By initially assuming that $V_{BE19} = 0.6$ **V**, **calculate** V_{BB} shown in the circuit. [6 marks]

Question 6 [20 marks]

(a) **List two** (2) ideal op-amp characteristics. [2 marks]

(b) For a **summing amplifier** using op-amps shown in **Figure 6b**, use appropriate ideal op-amp characteristics and **superposition theorem** to show that

$$v_O = v_{I1} + v_{I2}$$

when $R_1 = R_2 = R_F = 100\ \text{k}\Omega$. [7 marks]

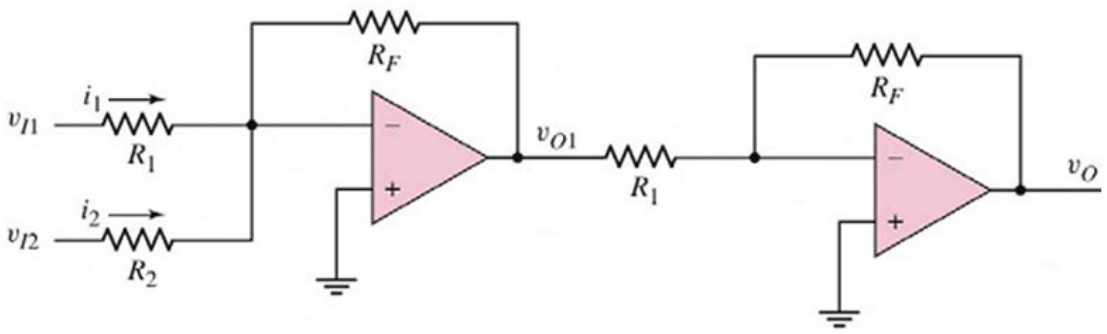

Figure 6b

(c) **Figure 6c** shows a design for an **instrumentation amplifier** using op-amps. In the design, R_{1POT} is a **100 kΩ potentiometer** (or a variable resistor) used to provide variable resistance so that differential voltage gain (A_v) of the instrumentation amplifier can be adjustable. With analysis, it can be shown that

$$v_O = \frac{R_4}{R_3}\left(1 + \frac{2R_2}{R_1 + R_{1POT}}\right)(v_{I2} - v_{I1})$$

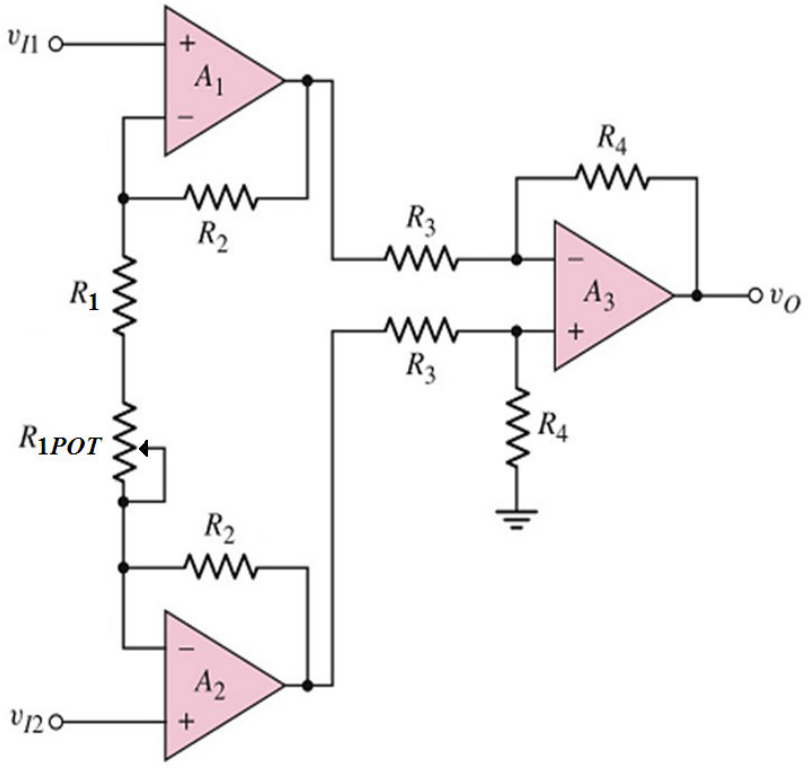

Figure 6c

(i) **What** is the name of an amplifier represented by op-amp A_3 in the **Figure 6c**?

[1 mark]

(ii) With $R_3 = R_4 = 100$ kΩ, **design an instrumentation amplifier** using the circuit as shown in the **Figure 6c** to realize a differential voltage gain (A_v) adjustable from **10 to 100.** (Hints: A_v is smallest when R_{1POT} is at maximum value, and vice versa. You are required to determine the value of R_1 and R_2 in the circuit). [7 marks]

(iii) With $v_{I1} = 1.00$ V, $v_{I2} = 1.15$ V, $R_4 = 2\,R_3$, R_{1POT} is set at **40** kΩ, and using the values of R_1 and R_2 found in step (ii) above, **calculate** A_v and v_O.

[3 marks]

-END OF QUESTION PAPER-