Name:

Student ID Number:

Section: **01/02/03/04/05 A/B**

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UNIVERSITI TENAGA NASIONAL

College of Engineering

Department of Electronics and Communication Engineering

Midterm Test – Model Answer

SEMESTER 1, ACADEMIC YEAR 2011/2012

Subject Code	:	**EEEB273**
Course Title	:	**Electronics Analysis & Design II**
Date	:	**17 June 2011**
Time Allowed	:	**2 hours**

<u>Instructions to the candidates:</u>

1. Write your Name and Student ID number. Circle your section number.
2. Write all your answers using pen. **DO NOT USE PENCIL** except for the diagram.
3. **ANSWER ALL QUESTIONS.**
4. **WRITE YOUR ANSWER ON THIS QUESTION PAPER.** Use both sides of the question paper to write your answers.
5. For all calculations, assume that V_T **= 26 mV**.

NOTE: DO NOT OPEN THE QUESTION PAPER UNTIL INSTRUCTED TO DO SO.

☺ **GOOD LUCK!** ☺

Question 1 **[40 marks]**

(a) List the advantage(s) of:

(i) A basic three-transistor current source as compared to a two-transistor BJT current source. [2 marks]

(ii) A Wilson current source as compared to a basic three-transistor BJT current source. [2 marks]

(iii) A cascode current source as compared to a Wilson BJT current source. [2 marks]

(iv) A Widlar current source as compared to a two-transistor BJT current source. [4 marks]

Answers for Question 1(a)

(i) Better approximation of I_O to I_{REF} for circuit using same transistors **[2]**

(ii) Higher output resistance by a factor of $\beta/2$ **[2]**

(iii) Higher output resistance by a factor of **2** **[2]**

(iv) Higher output resistance by a factor of $(1 + g_m R'_E)$ **[2]**
Using smaller resistors in the circuit **[2]**
Can have different values for I_O and I_{REF} where I_O is smaller than I_{REF} **[2]**
{Can use any two answers above}

(b) Consider a **modified three-transistor BJT current source** as in **Figure 1(b)**. Transistor parameters are V_{BE}**(on) = 0.7 V**, $V_A = \infty$, and β **= 80**. *Hint: Please take note of the current directions given in the* ***Figure 1(b)***.

(i) Show that

$$I_{REF} - \frac{V_{BE}}{(1+\beta)R_2} = I_O\left(1+\frac{2}{\beta(1+\beta)}\right) \quad [10 \text{ marks}]$$

(ii) For R_2 **= 10 kΩ**, V^+ **= 10 V**, and I_O **= 0.70 mA**, find I_{REF} and R_1. [10 marks]

<u>Answers for Question 1(b)</u>

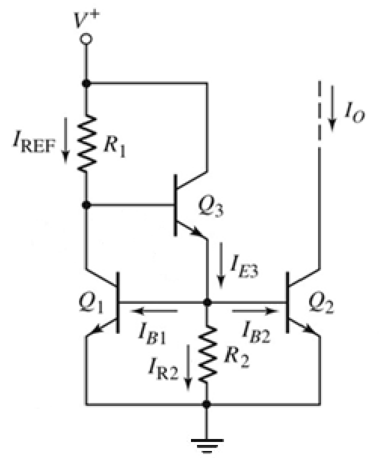


Figure 1(b)

(i)

$I_{B1} = I_{B2}$ [1]

$I_O = \beta I_{B2} \Rightarrow I_{B2} = I_O / \beta$ [1]

$I_{C1} = \beta I_{B2} \Rightarrow I_{C1} = I_O$ [1]

$I_{E3} = 2 I_{B2} + V_{BE} / R_2$ [1]

$I_{B3} = I_{E3} / (1 + \beta)$ [1]

$= (2 I_{B2})/(1 + \beta) + (V_{BE})/(1 + \beta)(R_2)$

$= (2 I_O)/(\beta(1 + \beta)) + (V_{BE})/((1 + \beta)R_2)$ [1]

$I_{REF} = I_{C1} + I_{B3}$ [1]

$= I_O + (2 I_O)/(\beta(1 + \beta)) + (V_{BE})/((1 + \beta)R_2)$ [1]

$I_{REF} - (V_{BE})/((1 + \beta)R_2) = I_O + (2 I_O)/(\beta(1 + \beta))$ [1]

$= I_O [1 + 2/(\beta(1 + \beta))]$

$$I_{REF} - \frac{V_{BE}}{(1+\beta)R_2} = I_0\left(1+\frac{2}{\beta(1+\beta)}\right)$$ [1]

(ii)

$I_{REF} = I_O (1 + 2/(\beta(1 + \beta))) + (V_{BE})/((1 + \beta)R_2)$ [2]

$= (0.70\text{m})(1+2/(80\text{x}81)) + (0.7)/(81\text{x}10\text{k})$ [2]

$= 0.700216\text{m} + 0.000864\text{m}$

$= 0.7011$ mA [1]

$R_1 = (V^+ - 2V_{BE}(\text{on}) - 0) / I_{REF}$ [2]

$= (10 - 2(0.7)) / (0.7011\text{m})$ [2]

$= 12.27$ kΩ [1]

(c) For a MOSFET current source circuit in **Figure 1(c)** the transistor parameters are V_{TN} **= 0.5 V**, k'_n **= 80 µA/V²**, and $\lambda = 0$. **Design the circuit** such that V_{DS2}**(sat) = 0.25 V**, I_{REF} **= 50 µA**, and the load current is I_O **= 100 µA**.

[10 marks]

Answers for Question 1(c)

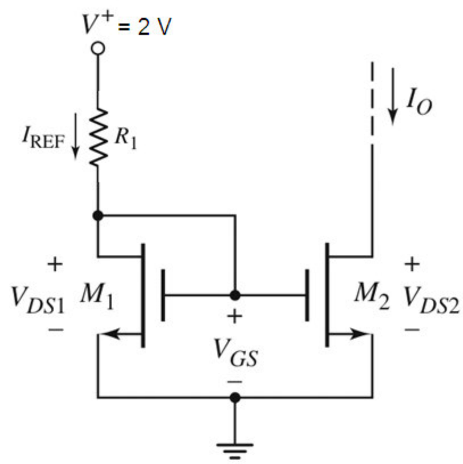


Figure 1(c)

$V_{DS2}(\text{sat}) = V_{GS} - V_{TN}$ **[1]**

$V_{GS} = V_{DS2}(\text{sat}) + V_{TN}$
$= 0.25 + 0.5 = 0.75\ \text{V}$ **[1]**

$I_{REF} = (V^+ - V_{GS} - 0) / R_1$ **[1]**

$R_1 = (V^+ - V_{GS} - 0) / I_{REF}$
$= (2 - 0.75) / (50\mu) = 25\ \text{k}\Omega$ **[1]**

$I_{REF} = (k'_n / 2)\, (W/L)_1 [V_{GS} - V_{TN}]^2$ **[1]**

$(W/L)_1 = I_{REF} / \{(k'_n / 2)\, [V_{GS} - V_{TN}]^2\}$ **[1]**
$= (50\mu) / \{(80\mu/2)\, [0.75 - 0.5]^2\}$
$= 20$ **[1]**

$I_O = (k'_n / 2)\, (W/L)_2 [V_{GS} - V_{TN}]^2$ **[1]**

$(W/L)_2 = I_O / \{(k'_n / 2)\, [V_{GS} - V_{TN}]^2\}$ **[1]**
$= (100\mu) / \{(80\mu/2)\, [0.75 - 0.5]^2\}$
$= 40$ **[1]**

Question 2 **[30 marks]**

(a) The basic differential pair is shown in **Figure 2(a)**. The circuit parameter values are: $\boldsymbol{V^+ = 10}$ **V**, $\boldsymbol{V^- = -10}$ **V** and $\boldsymbol{I_Q = 1}$ **mA**. The transistor parameters are $\boldsymbol{\beta = 100}$, $\boldsymbol{V_{BE}}$**(on) = 0.7 V** and $\boldsymbol{V_{CE}}$**(sat) = 0.2 V**. Assume that $\boldsymbol{v_{B1} = v_{B2} = 0}$**V**.

(i) Design the circuit by calculating the value of the maximum possible load, $\boldsymbol{R_C}$, before the transistors leave the active mode. [8 marks]

(ii) Using the answer in part (i), find the maximum possible single-ended differential voltage gain ($\boldsymbol{A_d}$). [3 marks]

Answers for Question 2(a)

(i)

$R_C = (V^+ - v_{C1}(\text{min})) / i_{C1}$

$v_{C1}(\text{min}) = v_E + V_{CE}(\text{sat})$

$v_E = v_{B1} - V_{BE1}(\text{on})$ [1]

$= 0 – 0.7 = -0.7$ V [1]

$v_{C1}(\text{min}) = v_E + V_{CE}(\text{sat})$ [1]

$= (-0.7) + 0.2 = -0.5$ V [1]

$i_{C1} \approx i_{E1} = I_Q / 2$ [1]

$= (1\text{m})/2 = 0.5$ mA [1]

$R_C = (V^+ - v_{C1}(\text{min})) / i_{C1}$ [1]

$= (10 – (-0.5)) / (0.5\text{m})$

$= 21$ kΩ [1]

(ii)

$A_d = (g_m R_c) / 2$ [1]

$g_m = (I_{CQ}) / V_T = (i_{C1}) / V_T$ [0.5]

$= (0.5\text{m}) / (26\text{m})$

$= 19.23$ mA/V [0.5]

$A_d = (g_m R_c) / 2$

$= (19.23\text{m} \times 21\text{k}) / 2$ [0.5]

$= 201.9$ V/V [0.5]

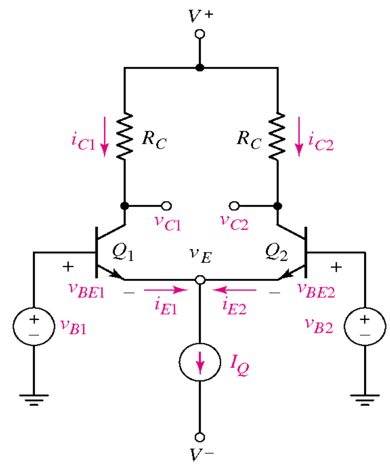


Figure 2(a)

(b) The constant current source of **Figure 2(a)** that is providing the current $\boldsymbol{I_Q}$ is implemented using the cascode current source.

(i) Sketch the differential pair circuit to include the constant current source circuit [2 marks]

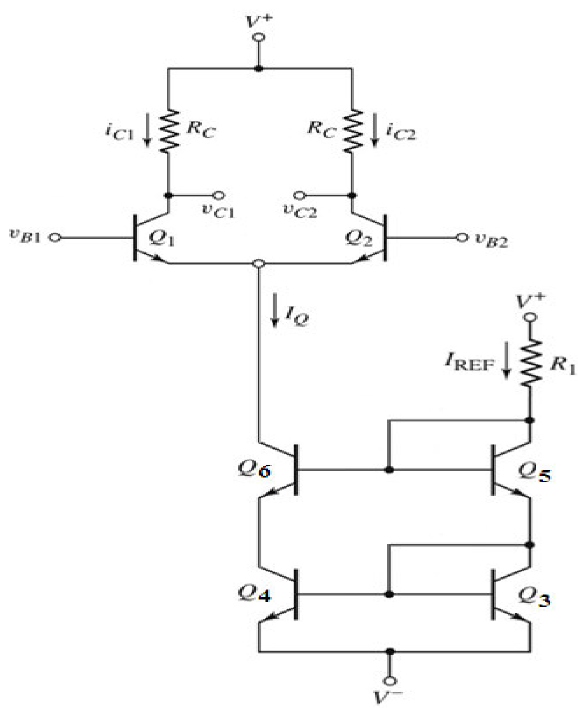
(ii) Assume that the **Early** voltage, $\boldsymbol{V_A}$, for all transistors in the circuit is **120 V**. What is the value of the output resistance, $\boldsymbol{R_O}$, looking into the constant-current source? [2 marks]

(iii) The common-mode voltage gain, $\boldsymbol{A_{cm}}$, of the differential-amplifier in **Figure 2(a)** is given as $A_{cm} = \dfrac{-g_m R_C}{1 + \dfrac{2(1+\beta)R_O}{r_\pi + R_B}}$. Find the value of $\boldsymbol{A_{cm}}$ for $\boldsymbol{R_B = 0}$. Use the results obtained previously in part (a) and (b). [2 marks]

(iv) It is given that the input voltages for the differential amplifier are $\boldsymbol{v_{B1} = 210 \times 10^{-6} \sin \omega t}$ **V** and $\boldsymbol{v_{B2} = 190 \times 10^{-6} \sin \omega t}$ **V**. Calculate the output voltage of the differential amplifier. Use values from previous calculations in part (a) and (b). [3 marks]

Answers for Question 2(b)

(i)



Correct sketch of cascode current source [1]
Correct connection between output of cascode to differential pair [1]

(ii)

β = 100, I_Q = 1 mA

For cascode current source

R_O	$= (\beta r_{O6})$	[0.5]
r_{O6}	$= V_A / I_Q$	[0.5]
	$= (120)/(1m) = 120\ k\Omega$	[0.5]
R_O	$= (\beta r_{O6}) = 100x120k$	
	$= 12\ M\Omega$	[0.5]

(iii)

g_m = 19.23 mA/V, R_C = 21 kΩ, R_B = 0, R_O = 6 MΩ

r_π	$= (\beta V_T) / i_{C1}$	[0.5]
	$= (100 \times 26m)/(0.5m)$	
	$= 5.2\ k\Omega$	[0.5]

Put all values above in the given formula

A_{cm}	$= -[(19.2m)(21k)] / [\{(1 + 2(1+100)(12M)\}/(5.2k+0)]$	
	$= -0.865m$ V/V	[1]

(iv)

A_d = 201.9, A_{cm} = -0.865m V/V

V_O	$= A_d V_d + A_{cm} V_{cm}$	[1]
V_d	$= v_{B1} - v_{B2}$	
	$= 210x10^{-6} \sin \omega t - 190x10^{-6} \sin \omega t$	
	$= 20x10^{-6} \sin \omega t$	[0.5]
V_{cm}	$= (v_{B1} + v_{B2}) / 2$	
	$= 200x10^{-6} \sin \omega t$	[0.5]
V_O	$= (201.9)(20x10^{-6} \sin \omega t) + (-0.865m)(200x10^{-6} \sin \omega t)$	
	$= 4.038x10^{-3} \sin \omega t + (-1.73x10^{-7} \sin \omega t)$	
	$= 4.038x10^{-3} \sin \omega t$ V	[1]

(c) It is given that the dc transfer characteristic of the differential pair is plotted in **Figure 2(c)**.

(i) Referring to the basic differential amplifier circuit in **Figure 2(a)**, prove the following I-V relationship which is plotted in **Figure 2(c)**. [6 marks]

$$i_{C1} = \frac{I_Q}{1+e^{-v_d/V_T}}$$

$$i_{C2} = \frac{I_Q}{1+e^{+v_d/V_T}}$$

(ii) What can you conclude by observing the dc transfer characteristic above? [4 marks]

Answers for Question 2(c)

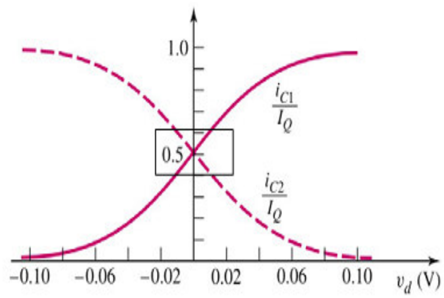


Figure 2(c)

(i)

- **Q1 and Q2 matched:**

$$i_{C1} = I_S e^{v_{BEI}/V_T} \quad \text{\{eqn 1\}} \quad [0.5]$$

and $$i_{C2} = I_S e^{v_{BE2}/V_T} \quad \text{\{eqn 2\}} \quad [0.5]$$

- **Neglect base currents:** $$I_Q = i_{C1} + i_{C2} \quad \text{\{eqn 3\}} \quad [1]$$

- **Replace eqn 1 & 2 into eqn 3:**

$$I_Q = I_S e^{v_{BEI}/V_T} + I_S e^{v_{BE2}/V_T} \quad \text{\{eqn 4\}} \quad [1]$$

- **Taking ratios of collector currents to IQ, i.e eqn1/eqn 4 and eqn2/eqn4:**

$$\frac{i_{C1}}{I_Q} = \frac{I_S e^{v_{BE1}/V_T}}{I_S[e^{v_{BE1}/V_T} + e^{v_{BE2}/V_T}]}$$ **{eqn 5}** **[0.5]**

$$\frac{i_{C2}}{I_Q} = \frac{I_S e^{v_{BE2}/V_T}}{I_S[e^{v_{BE1}/V_T} + e^{v_{BE2}/V_T}]}$$ **{eqn 6}** **[0.5]**

- **Defining** $v_d = v_{BE1} - v_{BE2}$ **{eqn7}** **[1]**
- **Simplifying eqn5 & 6 by dividing by** $e^{VBE1/VT}$ **and** $e^{VBE2/VT}$ **respectively** **[0.5]**
- **Substituting with {eqn7} to get final result:**

$$i_{C1} = \frac{I_Q}{1 + e^{-v_d/V_T}} \qquad i_{C2} = \frac{I_Q}{1 + e^{+v_d/V_T}}$$ **[0.5]**

(ii)

Any of the following points, 1 mark for each point:

- **if v_d =0, (or $v_{CM}=v_{B1}=v_{B2}$) I_Q splits evenly between Q_1 & Q_2**
- **if v_d is applied, a difference in collector current exist, causing difference in collector potential**
- **Gain is proportional to the slopes about the point v_d=0.**
- **v_d increases beyond the maximum limit: all I_Q goes to one transistor and hence the other transistor turns off.**
- **To obtain a linear amplifier: excursion of v_d about zero must be small.**

Question 3 **[30 marks]**

(a) Consider the circuit shown in **Figure 3(a)**. The circuit parameters are $\beta = 100$, $V_A = \infty$ for Q_1 and Q_2, $V_A = 50$ V for Q_3 and Q_4, $I_S = 10^{-14}$ A, $I_3 = 400$ μA, $v_{O2} = 10$ V, and $A_{cm} = -0.113$. Determine:

(i) The differential-mode input resistance. [7 marks]

(ii) The ***CMRR***. [3 marks]

(iii) Draw the ac equivalent circuit of the **differential amplifier part**. Label all the components clearly. [5 marks]

Answers for Question 3(a)

(i)

$R_{id} = 2(r_\pi + R_B)$ [1]

$R_B = 10\ \text{k}\Omega$ [1]

$r_\pi = (\beta V_T)/I_{CQ}$ [1]

$= (\beta V_T)/(I_Q/2)$

$= (2\beta V_T)/I_Q$ [1]

$= (2\beta V_T)/I_3$ [1]

$= (2\text{x}100\text{x}26\text{m})/(400\mu) = 13\ \text{k}\Omega$ [1]

$R_{id} = 2(13\text{k} + 10\text{k})$

$= 46\ \text{k}\Omega$ [1]

(ii)

$CMRR = |A_d / A_{cm}|$

$A_d = (\beta R_c)/(2(r_\pi + R_B))$

$R_c = (V^+ - v_{O2}) / I_{C2}$

$= (V^+ - v_{O2}) / (I_3/2)$ [0.5]

$= (15 - 10) / (400\mu/2)$

$= 25\ \text{k}\Omega$ [0.5]

$A_d = (\beta R_c)/(2(r_\pi + R_B))$ [0.5]

$= (100\text{x}25\text{k})/(2(13\text{k} + 10\text{k}))$

$= 54.34$ [0.5]

$CMRR = |A_d / A_{cm}|$ [0.5]

$= |54.34/(-0.113)|$

$= 480.88$ [0.5]

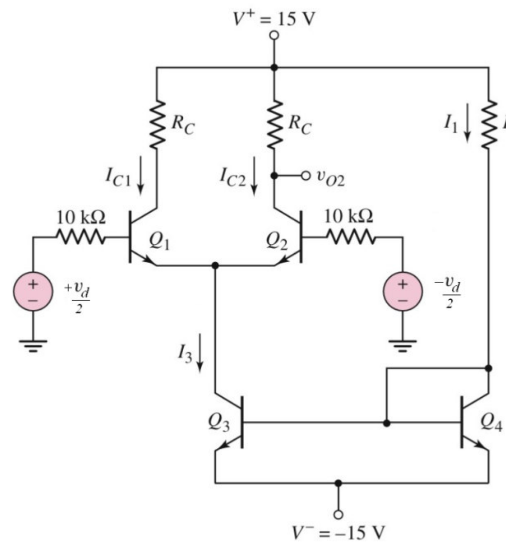
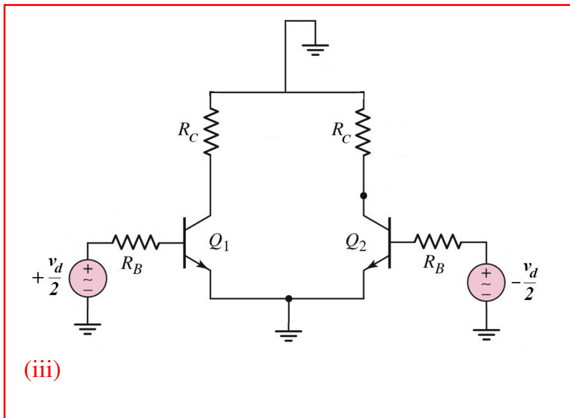


Figure 3(a)



Grounds [2], R_C [1], R_B [1], Q [1]

(b) The circuit parameters for the diff-amp shown in **Figure 3(b)** are V^+ **= 3.3 V**, V^- **= -3.3 V**, and I_Q **= 0.4 mA**. The transistor parameters are β **= 120**, V_A **= 120 V** for Q_1 and Q_2, V_A **= 80 V** for Q_3 and Q_4, and $V_A = \infty$ for Q_5.

(i) Determine the output resistance of the diff-amp. [7 marks]

(ii) Determine the open-circuit differential-mode voltage gain. [5 marks]

(iii) What is the effect of R_L on the differential-mode voltage gain of the diff-amp? Provide support for your answer. [3 marks]

Answers for Question 3(b)

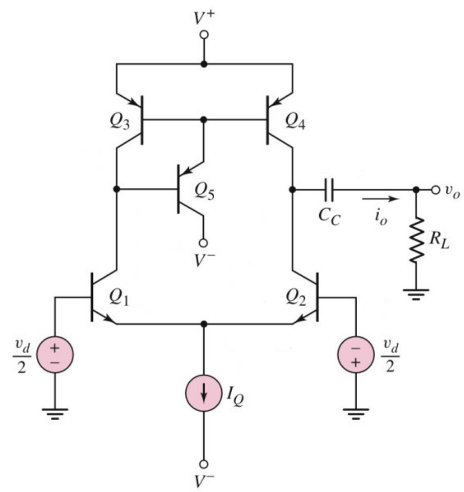


Figure 3(b)

	$I_{CQ} = I_Q / 2 = (0.4m)/2$	$= 0.2$ mA	[1]
	$r_{O2} = V_{A2}/I_{CQ} = 120/(0.2m)$	$= 600$ kΩ	[2]
	$r_{O4} = V_{A4}/I_{CQ} = 80/(0.2m)$	$= 400$ kΩ	[2]
(i)	$R_O = r_{O2} \| r_{O4} = 600k \| 400k$	$= 240$kΩ	[2]
	$g_m = I_{CQ}/V_T = (0.2m)/(26m)$	$= 7.692$ mA/V	[2]
(ii)	$A_v = g_m(r_{O2} \| r_{O4}) = (7.692m)(600k \| 400k) = 1846$		[3]

(iii) New $R_O = r_{O2} \| r_{O4} \| R_L$: $A_v = g_m R_O$ **will become smaller.**
Therefore large value for R_L is required so as not to change the differential-mode voltage gain so much. **[3]**