COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 2 2011 / 2012

PROGRAMME	**: Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	**: EEEB273**
SUBJECT	**: ELECTRONIC ANALYSIS AND DESIGN II**
DATE	**: January 2012**
TIME	**: 3 hours (9.00 am – 12.00 pm)**

INSTRUCTIONS TO CANDIDATES:

1. This question paper contains **SIX (6)** questions in **TWELVE (12)** pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided.
4. Write answer to each question on **a new page**.
5. For all calculations, assume that V_T **= 26 mV**.

THIS QUESTION PAPER CONSISTS OF TWELVE (12) PRINTED PAGES INCLUDING THIS COVER PAGE AND APPENDIX.

Question 1 [16 marks]

(a) A basic **two-transistor BJT current source** consists of two **npn-type BJT transistors** and a resistor, $\boldsymbol{R_1}$, to establish its **reference current,** $\boldsymbol{I_{REF}}$. The reference current is established when the circuit is connected to positive and negative power source, $\boldsymbol{V^+}$ and $\boldsymbol{V^-}$.

(i) Let the second transistor, $\boldsymbol{Q_2}$, be the output transistor. **Draw and label** the circuit and its components **clearly**.

[3 marks]

(ii) Assume the transistors are matched and the transistors parameters are $\boldsymbol{\beta = 88}$, $\boldsymbol{I_{S1} = 4.5\text{x}10^{-15}}$ **A**, and $\boldsymbol{I_{S2} = 3\text{x}10^{-15}}$ **A**. If $\boldsymbol{I_{REF} = 210}$ **μA**, calculate $\boldsymbol{V_{BE1}}$, $\boldsymbol{V_{BE2}}$, and the bias current, $\boldsymbol{I_O}$.

[5 marks]

(b) A **cascode N-MOSFET** current source circuit is described by the following: The output current is **1 mA**; The circuit parameters are $\boldsymbol{V^+ = 15}$ **V** and $\boldsymbol{V^- = -15}$ **V**; All transistors are identical; The transistor parameters are $\boldsymbol{V_{DS}}$**(sat) = 0.8 V**, $\boldsymbol{V_{TN} = 1.5}$ **V**, $\boldsymbol{k'_n = 120}$ **μA/V²** and $\boldsymbol{\lambda = 0}$.

(i) **Find** the **aspect ratio** for **all transistors** of the cascode current source.

[4 marks]

(ii) What is the required resistance value, $\boldsymbol{R}$, to establish the **reference current**?

[2 marks]

(iii) **How much** will the output current change if the output voltage changes by **5 V**?

[2 marks]

Question 2 [16 marks]

Consider the circuit shown in **Figure 2**, where a MOSFET differential amplifier (consists of M_1 **and** M_2) is biased by a cascode current source (consists of M_3, M_4, M_5, **and** M_6). The bias voltages are **+3 V** and **-3 V**. The transistor parameters are $K_{n1} = K_{n2} = 150\ \mu A/V^2$, $K_{n3} = K_{n4} = K_{n5} = K_{n6} = 100\ \mu A/V^2$, and $V_{TN} = 0.3$ **V** for all transistors.

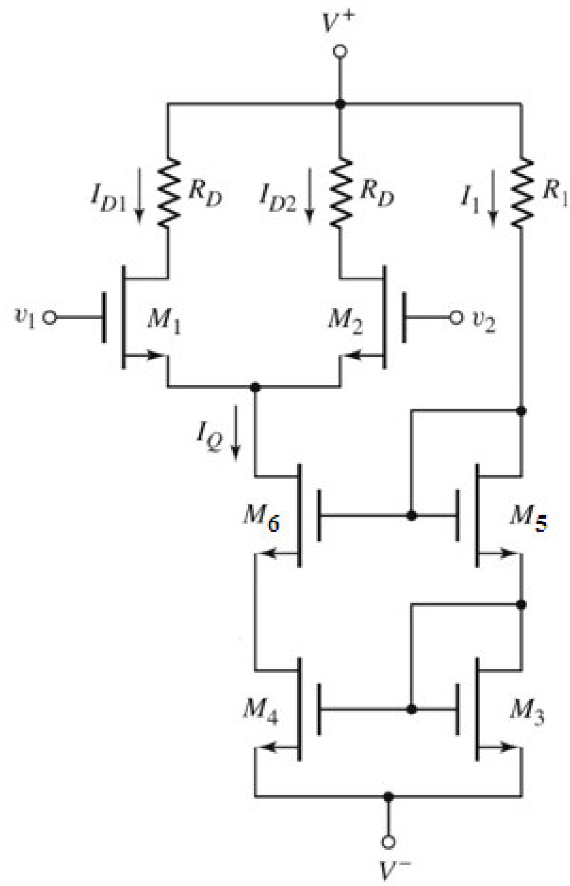

Figure 2

(a) **Calculate** R_1 and R_D in the circuit such that $V_{DS1} = V_{DS2} = 3$ **V,** $V_{DS3} = V_{DS5}$, and $I_{D1} = I_{D2} = 60\ \mu A$ when $v_1 = v_2 = -0.5$ **V**. *Hints*: $V_G = V_S + V_{GS}$, $V_D = V_S + V_{DS}$.

[8 marks]

(b) **One-sided output (V_O)** taken at V_{D2} **can be derived** using small-signal equivalent circuit to produce

$$V_o = \frac{g_m R_D}{2} V_d - \frac{g_m R_D}{1 + 2 g_m R_o} V_{cm}$$

If λ **= 0.01 V^{-1}** for M_3, M_4, M_5, and M_6**:**

(i) **Determine** the **output resistance** (R_o) of the MOSFET cascode current source.

[2 marks]

(ii) **Calculate** the differential-mode voltage gain (A_d), common-mode voltage gain (A_{cm}), and ***CMRR*** for the differential amplifier **using result from part (a)**.

[6 marks]

Question 3 [16 marks]

(a) The differential amplifier in **Figure 3a** has 4 identical PMOS transistors as an **active load**. The circuit is connected to power supply voltages of V^+ **= +3 V** and V^- **= -3 V**. The current source is I_Q **= 200 µA** and its output resistance, $R_{OCS} = \infty$. The NMOS transistors parameters are V_{TN} **= 0.4 V**, k'_n **= 100 µA/V²**, $(W/L)_n$ **= 10**, and λ_n **= 0.02 V⁻¹**. The PMOS transistors parameters are V_{TP} **= –0.4 V**, k'_p **= 50 µA/V²**, $(W/L)_p$ **= 12,** and λ_p **= 0.03 V⁻¹**. **Determine** the output voltage, v_O, if the differential input voltage applied is v_d **= (20 sin ωt) µV**.

[8 marks]

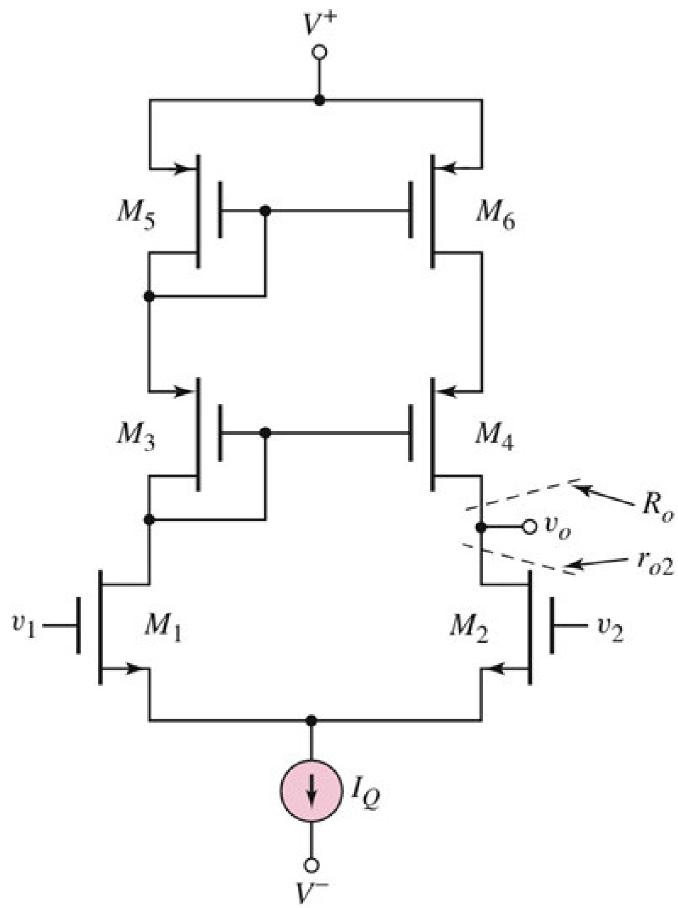

Figure 3a

(b) The circuit in **Figure 3b** shows a simple multistage BJT op-amp.

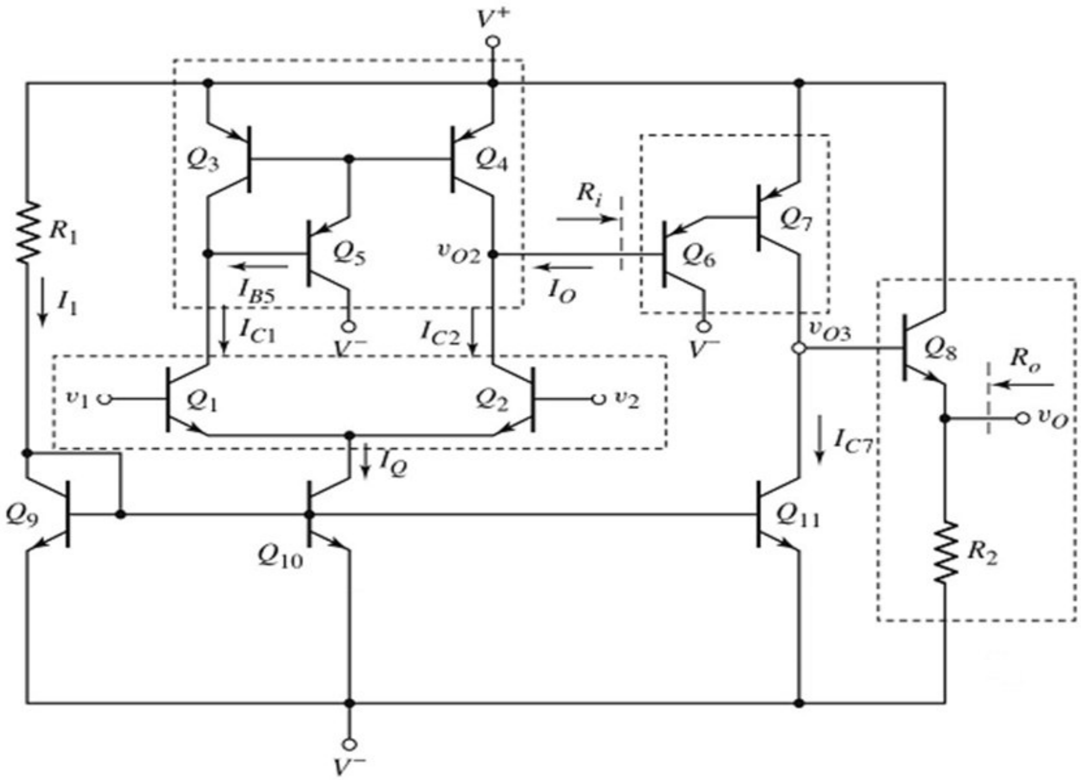

Figure 3b

(i) **Name** the circuits **indicated** by the boxes.

[2 marks]

(ii) Assuming that for all transistors: $\boldsymbol{r_o}$ **= 500 kΩ,** $\boldsymbol{g_m}$ **= 5 mA/V,** and $\boldsymbol{r_\pi}$ **= 3 kΩ,** and $\boldsymbol{R_2}$ **= 10 kΩ**. **Calculate the small signal impedances** $\boldsymbol{R_i}$ and $\boldsymbol{R_O}$ as indicated in the **Figure 3b**.

[6 marks]

Question 4 [16 marks]

(a) Consider input stage and bias circuit of the 741 operational amplifier in **Figure 4a**, with $V^+ =$ **+15 V**, $V^- =$ **-15 V**, $V_{BE6} = V_{BE7} =$ **0.6 V**, $\beta = 200$ and $I_{C9} =$ **10 µA**. The reverse saturation current $I_S = 10^{-14}$ **A** for each transistor and the current flow through resistance R_5 is **1mA**. Ignore the base currents and assume the dc currents in the input stage are exactly balanced.

(i) Determine the resistance R_5 and R_4.

[4 marks]

(ii) Find the current I_{C1} and $r_{\pi 6}$.

[2 marks]

(iii) Determine the dc voltage at the collector of Q_5 (i.e. V_{C5}).

[2 marks]

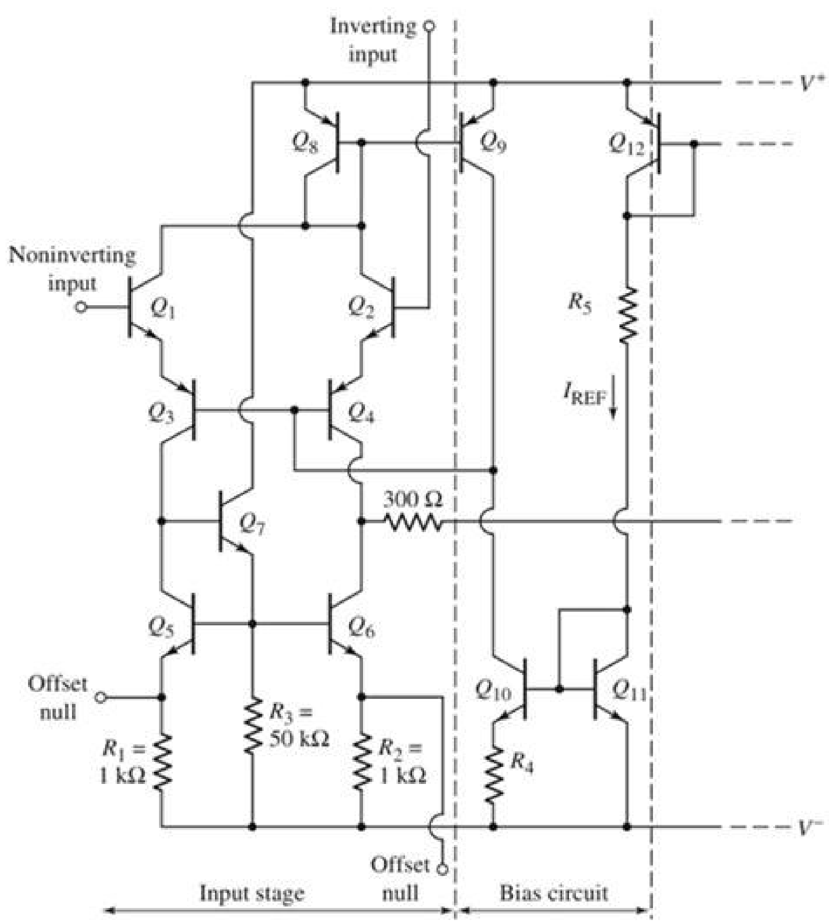

Figure 4a

(b) Consider the **MC14573** op-amp in **Figure 4b.** Assume transistors parameters of V_{TN} **= 0.5 V**, V_{TP} **= -0.5 V**, K_n **= 125 µA/V²**, K_p **= 100 µA/V²**, V_{SG5} **= 1.5 V**, λ_n **= 0.01 V⁻¹**, λ_p **= 0.02 V⁻¹** and the circuit parameters of V^+ **= +10 V** and V^- **= -10 V**.

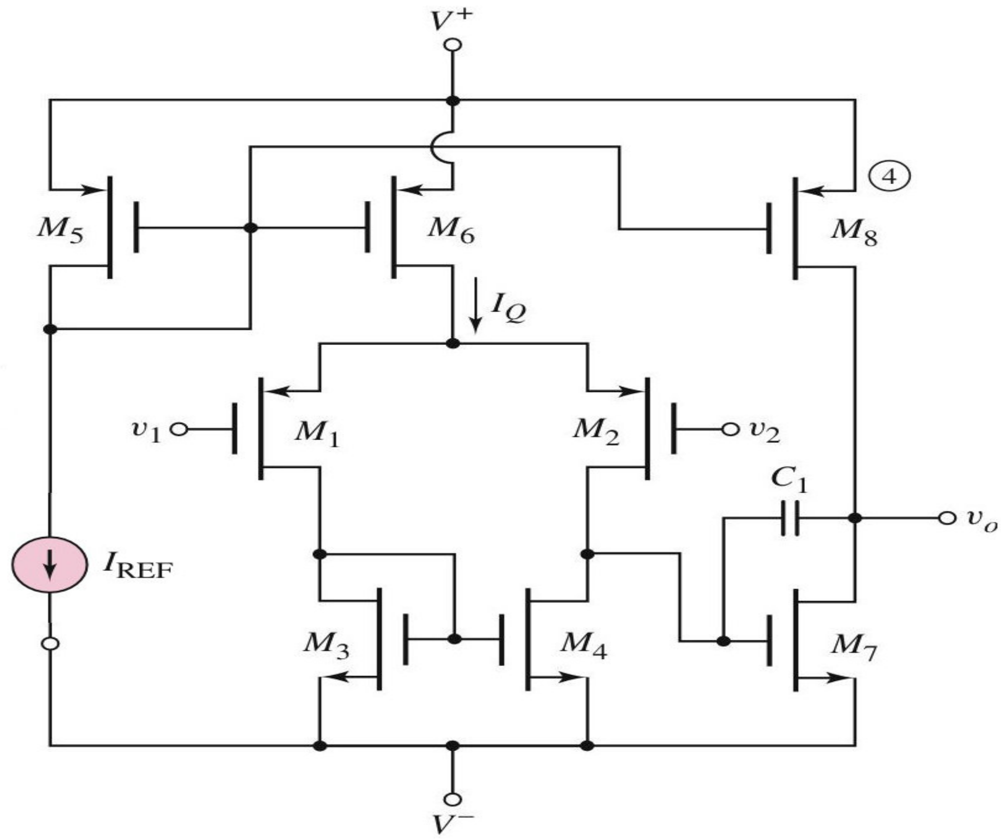

Figure 4b

(i) **Find** the dc bias currents I_Q.

[3 marks]

(ii) **Determine** the overall voltage gain of the op-amp.

[5 marks]

Question 5 [16 marks]

(a) **Differentiate** among **class-A, class-B, class-AB, and class-C** output stage amplifiers.

[6 marks]

(b) Study **Figure 5** carefully. The transistor parameters are: $\boldsymbol{\beta}$ **= 180,** $\boldsymbol{V_{BE}}$**(on) = 0.7 V**, and $\boldsymbol{V_{CE}}$**(sat) = 0.4 V**. **Design** the output stage amplifier for maximum output swing and then calculate its **power conversion efficiency**, $\boldsymbol{\eta}$.

[10 marks]

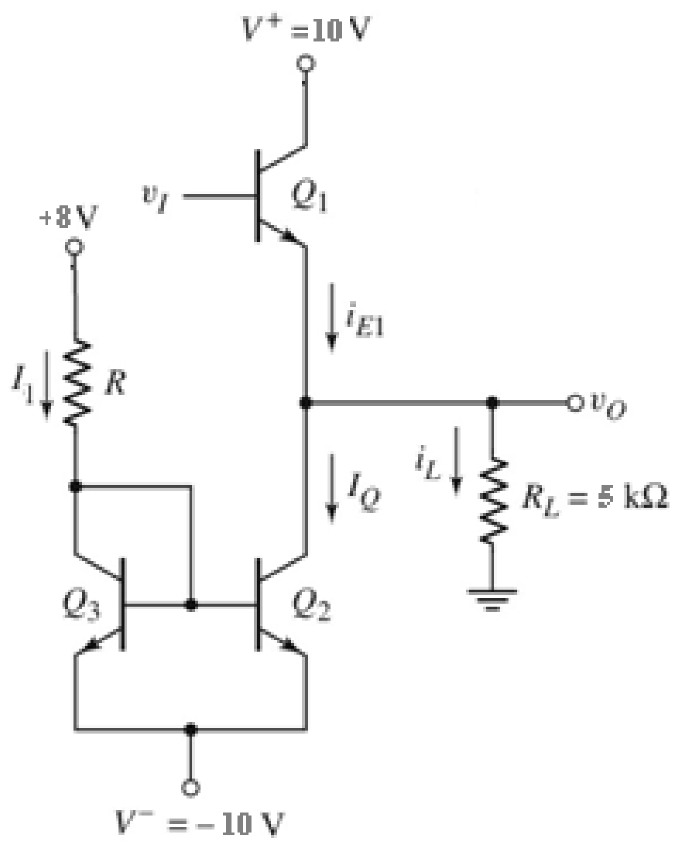

Figure 5

Question 6 [20 marks]

(a) Using **feedback resistor** of **18 kΩ**, **draw** the following circuits using **inverting op-amp** configuration:

(i) An **inverting amplifier** with a closed-loop gain of **-10**.

[4 marks]

(ii) A **voltage follower**.

[4 marks]

(b) Consider the **non-inverting op-amplifier** shown in **Figure 6a**. Assume the op-amp is ideal. Determine the resistor values of $\boldsymbol{R_1}$ and $\boldsymbol{R_2}$ to produce a closed-loop gain of **15**, with the minimum resistance in the circuit is to be **20 kΩ**.

[4 marks]

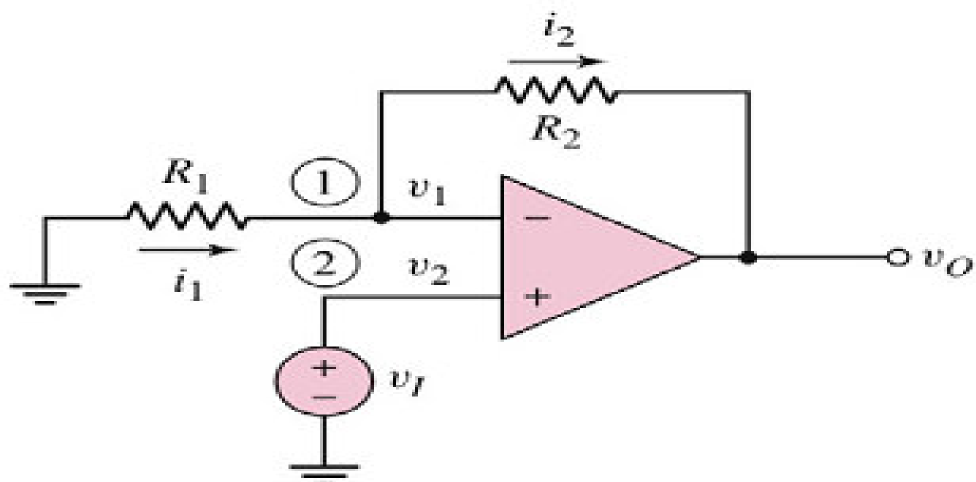

Figure 6a

(c) For a **generalized summing op-amp** as shown in **Figure 6b** the total output voltage is the sum of the individual terms, or

$$v_O = -\frac{R_F}{R_1}v_{I1} - \frac{R_F}{R_2}v_{I2} + \left(1+\frac{R_F}{R_N}\right)\left(\frac{R_P}{R_A}v_{I3} + \frac{R_P}{R_B}v_{I4}\right)$$

where $R_N = R_1 \| R_2$

$R_P = R_A \| R_B \| R_C$

Design a summing op-amp similar to **Figure 6b** to produce the output

$$v_O = -5v_{I1} - 10v_{I2} + 5v_{I3} + 2v_{I4}$$

The smallest resistor value allowable in the design is **15 kΩ**.

[8 marks]

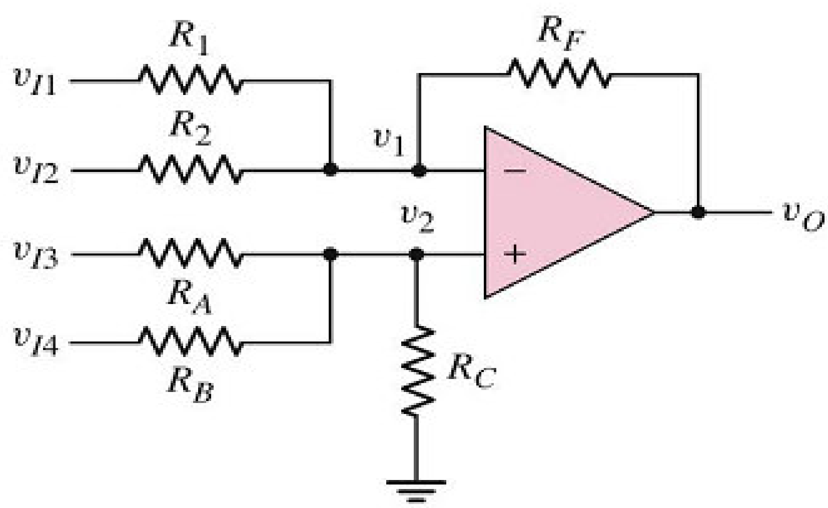

Figure 6b

-END OF QUESTION PAPER-

APPENDIX

BASIC FORMULA FOR TRANSISTORS

BJT

$$i_C = I_S e^{v_{BE}/V_T}$$

$$i_C = \alpha i_E = \beta i_B$$

$$i_E = i_B + i_C$$

$$\alpha = \frac{\beta}{\beta + 1}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$\beta = g_m r_\pi$$

$$r_o = \frac{V_A}{I_{CQ}}$$

MOSFET

$$v_{DS}(sat) = v_{GS} - V_{TN}$$

$$i_D = K_n [v_{GS} - V_{TN}]^2$$

$$K_n = \frac{k_n^{'}}{2} \cdot \frac{W}{L}$$

$$v_{SD}(sat) = v_{SG} + V_{TP}$$

$$i_D = K_p [v_{SG} + V_{TP}]^2$$

$$K_p = \frac{k_p^{'}}{2} \cdot \frac{W}{L}$$

$$g_m = 2\sqrt{K_n I_{DQ}}$$

$$r_o \cong \frac{1}{\lambda I_{DQ}}$$