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UNIVERSITI TENAGA NASIONAL

College of Engineering

Department of Electronics and Communication Engineering

Midterm Test

SEMESTER 2, ACADEMIC YEAR 2011/2012

Subject Code	:	**EEEB273**
Course Title	:	**Electronics Analysis & Design II**
Date	:	**14 November 2011**
Time Allowed	:	**2 hours (8 – 10 PM)**

Instructions to the candidates:

1. Write your Name and Student ID number. Circle your section number.
2. Write all your answers using pen. **DO NOT USE PENCIL** except for the diagram.
3. **ANSWER ALL QUESTIONS.**
4. **WRITE YOUR ANSWER ON THIS QUESTION PAPER.**

NOTE: DO NOT OPEN THE QUESTION PAPER UNTIL INSTRUCTED TO DO SO.

☺ **GOOD LUCK!** ☺

Question No.									
Marks									

Question 1 [40 marks]

(a) For all **BJT current sources** given in **Table 1**, all transistors are matched and have same parameters. The transistor parameters are: β **= 50**, V_{BE}**(on) = 0.6 V**, and V_A **= 120 V**. The circuit parameters are: V^+ **= 10 V**, V^- **= -10 V,** and R_1 **= 18 kΩ**.

(i) **Calculate** reference current (I_{REF}), output current (I_O), and output resistance (R_O) for every BJT current source given in the **Table 1** and fill in the **Table 1** with your answers. **Show all calculations** in the area provided after the **Table 1** and **do not forget** to put proper **Units** for I_{REF}, I_O, and R_O in the **Table 1**.

Table 1

BJT current source	Reference current, I_{REF}	Output current, I_O	Output resistance, R_O
Three-transistor current source	**1.044 mA**	**1.044 mA**	**114.98 kΩ**
Wilson current source	**1.044 mA**	**1.044 mA**	**2.847 MΩ**
Cascode current source	**1.044 mA**	**0.967 mA**	**6.204 MΩ**

[0.5 mark each] [4.5 marks]

(ii) Based on the value of R_O, **which current source** has the most stable I_O?

[2 marks]

Cascode [2]

Show all your calculations for I_{REF}, I_O, and R_O for every BJT current source given in the **Table 1** in the following space:

[13.5 marks]

Three-transistor current source	Wilson current source	Cascode current source
$I_{REF} = (V^+ - 2\,V_{BE} - V^-)/R_1$ = (10 – 2x0.6 – (-10))/(18k) = 1.044 mA **-- same for all CS**		
$I_O = I_{REF}/(1 + 2/(\beta(1+\beta)))$ = (1.044m)/(1+2/(50x51)) = 1.044 mA	$I_O = I_{REF}/(1 + 2/(\beta(2+\beta)))$ = (1.044m)/(1+2/(50x52)) = 1.044 mA	$I_O = I_{REF}/(1 + 4/\beta)$ = (1.044m)/(1+4/(50)) = 0.967 mA
$r_{O2} = V_A / I_O$ = 120/(1.044m) = 114.98 kΩ $R_O = r_{O2}$ = 114.98 kΩ	$r_{O3} = V_A / I_O$ = 120/(1.044m) = 114.98 kΩ $R_O = (\beta\, r_{O3})/2$ = (50x114.98k)/2 = 2.847 MΩ	$r_{O4} = V_A / I_O$ = 120/(1.278m) = 124.08 kΩ $R_O = \beta\, r_{O4}$ = 50x117.391k = 6.204 MΩ

[1.5 mark each]

(b) Consider the **MOSFET current source** circuit shown in **Figure 1** for the following questions. The circuit parameters are V^+ **= 10 V**, V^- **= -10 V,** I_O **= 0.25 mA,** and the transistor parameters are: V_{TN} **= 1.5V**, V_{DS2}**(sat) = 2.5 V**, $k'_{n1} = k'_{n2}$ **= 40 μA/V²**, k'_{n3} **= 20 μA/V²** and $\lambda = 0$.

(i) **Determine** the voltages V_{GS1} and V_{GS3}, and the current I_{REF}.

[8 marks]

$V_{DS2}(sat) = V_{GS2} - V_{TN}$

$V_{GS2} = V_{DS2}(sat) + V_{TN} = 2.5 + 1.5 = 4$ V

$V_{GS1} = V_{GS2} = 4$ V [2]

$V_{GS3} = V^+ - V_{GS1} - V^- = 10 - 4 + 10 = 16$ V [2]

Since $k'_{n1} = k'_{n2}$ and $V_{GS1} = V_{GS2}$

Assume $(W/L)_1 = (W/L)_2$

Then $I_{REF} = I_O = 0.25$ mA [4]

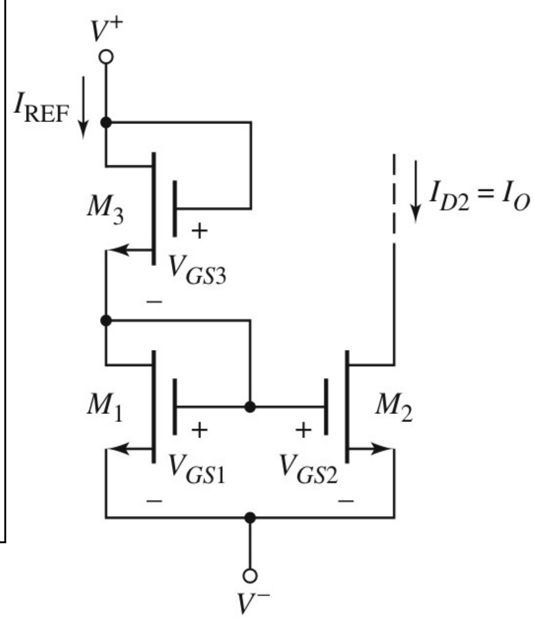


Figure 1

(ii) **Calculate** the width-to-length ratio of M_3, i.e. $\left(W/L\right)_3$.

[4 marks]

$I_{REF} = (k'_{n3}/2)(W/L)_3[V_{GS3} - V_{TN}]^2$

$(W/L)_3 = I_{REF} / \{(k'_{n3}/2)[V_{GS3} - V_{TN}]^2\}$ [3]

$= (0.25m)/\{(20\mu/2)(16-1.5)^2\} = 0.1189$ [1]

(iii) If λ **= 0.01 V**$^{-1}$, what is the change in output current (I_O) as the output voltage at V_{D2} has changed by **9 V**?

[4 marks]

$R_O = r_{O2} = 1/(\lambda I_O) = 1/(0.01 \times 0.25m) = 400\ k\Omega$ **[2]**

$R_O = \Delta V_{D2} / \Delta I_O$

$\Delta I_O = \Delta V_{D2} / R_O = 9/400k = 0.0225\ mA = 22.5\ \mu A$ **[2]**

(iv) **Suggest** a suitable **circuit** to stabilize the output current against variations in the output voltage of the MOSFET current source.

[4 marks]

Use other MOSFET current source circuits with higher R_O, such as cascode CS and modified Wilson CS.

Answer in drawing of cascode CS and modified Wilson CS also can be accepted.

[4] for any answer above.

Question 2 [30 marks]

The **BJT differential amplifier** as shown in **Figure 2** has these following parameters: $V^+ = 10$ **V**, $V^- = -10$ **V**, $R_1 = 30$ **kΩ**, $\beta = 100$, $V_{CE1} = V_{CE2} = 6$ **V**, $A_{cm} = 0.5$, and $V_T = 26$ **mV**. The **Early** voltages are $V_A = 100$ **V** for Q_1 and Q_2, and $V_A = 80$ **V** for Q_3 and Q_4. Use $V_{BE}(\text{on}) = 0.6$ **V.**

(a) **Determine** the currents I_1 and I_{C2} of the transistors for $v_1 = v_2 = 0$ V.

[8 marks]

$I_1 = (V^+ - V_{BE}(\text{on}) - V^-) / R_1$
$= (10 - 0.6 - (-10))/(30k) = 0.647$ mA **[4]**

$I_{C2} = I_{C4}/2 = [I_1 / (1+2/\beta)] / 2$
$= [0.647m / (1+2/100)] / 2 = 0.3171$ mA **[4]**

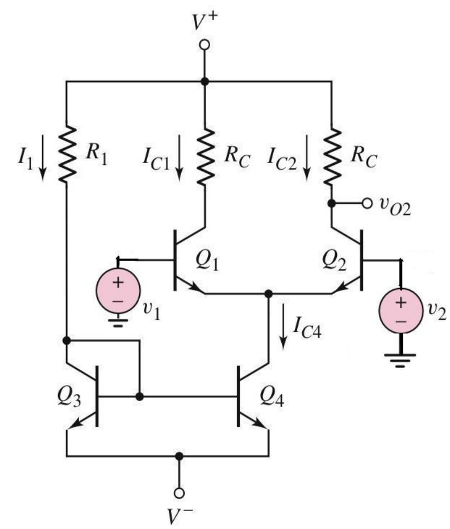


Figure 2

(b) **Determine** the values of R_C, r_{o4}, r_{o2}.

[9 marks]

R_C	$= (V^+ - V_{C2}) / I_{C2}$	$= (10 - 5.4) / 0.3171m = 13.876$ kΩ	**[3]**
V_{C2}	$= (V_{CE2} + V_{E2}) = 6 + (-0.6)$	$= 5.4$ V	
V_{E2}	$= (V_{B2} - V_{BE2}) = (v_2 - V_{BE2})$	$= 0 - 0.6 = -0.6$ V	

$r_{o4} = V_{A4} / I_{C4} = 80 / 0.647m = 123.64$ kΩ **[3]**

$r_{o2} = V_{A2} / I_{C2} = 100 / 0.3171m = 315.36$ kΩ **[3]**

(c) Determine the differential mode voltage gain (A_d) and ***CMRR*** for a **two-sided output**.

[8 marks]

A_d	$= g_{m2} R_C$	= (12.196 m)(13.876k)	= 169.23	[3]
g_{m2}	$= I_{C2} / V_T$	= 0.3171mA / 26mV	= 12.196 mA/V	[2]
CMRR	$= \lvert A_d / A_{cm} \rvert$	= 176.89 / 0.5	= 353.78	[3]

(d) **What is the impact** of including an emitter resistor R_E for Q_1 and Q_2 on the differential mode voltage gain (A_d)? **Write down** the equation of the differential mode voltage gain when emitter resistor R_E for Q_1 and Q_2 are included in the circuit.

[5 marks]

A_d **is reduced.** [2]

Original: $A_d = (\beta R_C) / 2[r_\pi]$

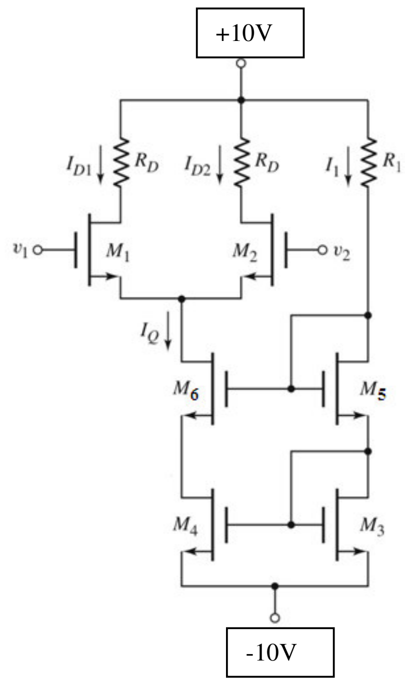
With R_E: $A_d = (\beta R_C) / 2[r_\pi + (1+\beta) R_E]$ [3]

Question 3 [30 marks]

With aid of circuit diagram, **design a MOSFET differential amplifier** with **cascode current source** to establish the desired bias current $\boldsymbol{I_Q}$ **= 0.58 mA**. The supply voltages for the overall circuit are $\boldsymbol{V^+}$ **= 10 V** and $\boldsymbol{V^-}$ **= -10 V**. The transistor parameters for the MOSFET differential amplifier pair are $\boldsymbol{k'_n}$ **= 80 μA/V²** and for the current source pair are $\boldsymbol{k'_n}$ **= 40 μA/V²**. For all transistors assume $\boldsymbol{\lambda}$ **= 0.02 V⁻¹** and $\boldsymbol{V_{TN}}$ **= 1 V**. Consider a **one-sided output** with $\boldsymbol{V_{DS2}}$**(sat) = 0.8 V** and a differential-mode voltage gain of $\boldsymbol{A_d}$ **= 10**.

(a) Draw the designed circuit. **Label the circuit clearly**.

[7 marks]



Diff-amp pair	**[1]**
R_D pair	**[1]**
NMOS for diff-amp and CS	**[1]**
I_Q	**[1]**
Output	**[1]**
Cascode CS	**[1]**
Supplies	**[1]**

(b) Determine the (**W/L**) ratio for transistors in the **differential amplifier pair**.

[8 marks]

$(W/L)_{1,2} = (2I_{D1})/[k'_n(V_{GS1}-V_{TN})^2]$ **[2]**

$= (I_Q)/[k'_n(V_{DS2}(sat))^2]$ **[3]**

$= (0.58m)/[(80\mu)(0.8)^2]$ **[2]**

$= 11.33$ **[1]**

(c) Determine the drain resistance (***R_D***) in the **differential amplifier**.

[6 marks]

$A_d = (g_{m2} R_D)/2$

$R_D = (2 A_d) / g_{m2}$ **[2]**

$g_{m2} = 2[\sqrt{(K_n I_D)}] = (I_Q)/[(V_{DS2}(sat))] = 0.725$ **mA/V** **[2]**

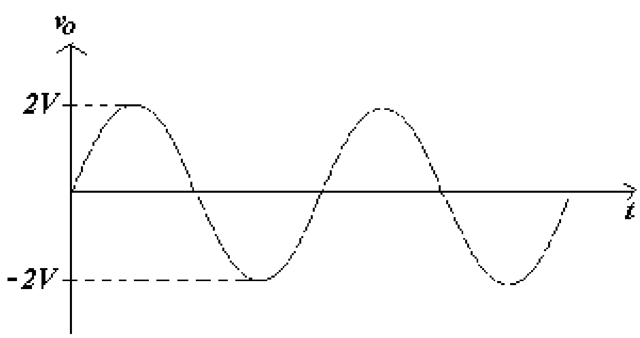
$R_D = (2 A_d) / g_{m2}$
$= (2 \times 10) / (0.725m) = 27.58$ **kΩ** **[2]**

(d) Draw the output voltage of the differential amplifier when a differential-mode input voltage of $v_d = 0.2 \sin \omega t$ **V** is applied.

[4 marks]

$v_O = A_d v_d$
$= (10)(0.2 \sin \omega t)$ **V or** $2 \sin \omega t$ **V** **[1]**

Amplitude **[1]**
Shape **[1]**
Axis **[1]**



(e) With reference to your designed circuit in **part (a)** above, and using a **P-MOSFET cascode** current source **as an active load** to replace the drain resistances (***R_D***) in the differential amplifier, **as shown in Figure 3**, **calculate** the differential-mode voltage gain (*A_d*) of the new circuit for a **one-sided output**. For all **P-MOSFET** transistors ***M_{11}*** to ***M_{14}***, assume ***λ* = 0.02 V^{-1}** and ***V_{TP}* = -1 V.** ***R_O*** in the **Figure 3** can be calculated using ***$R_O \approx g_m r_{o12} r_{o14}$***

[5 marks]

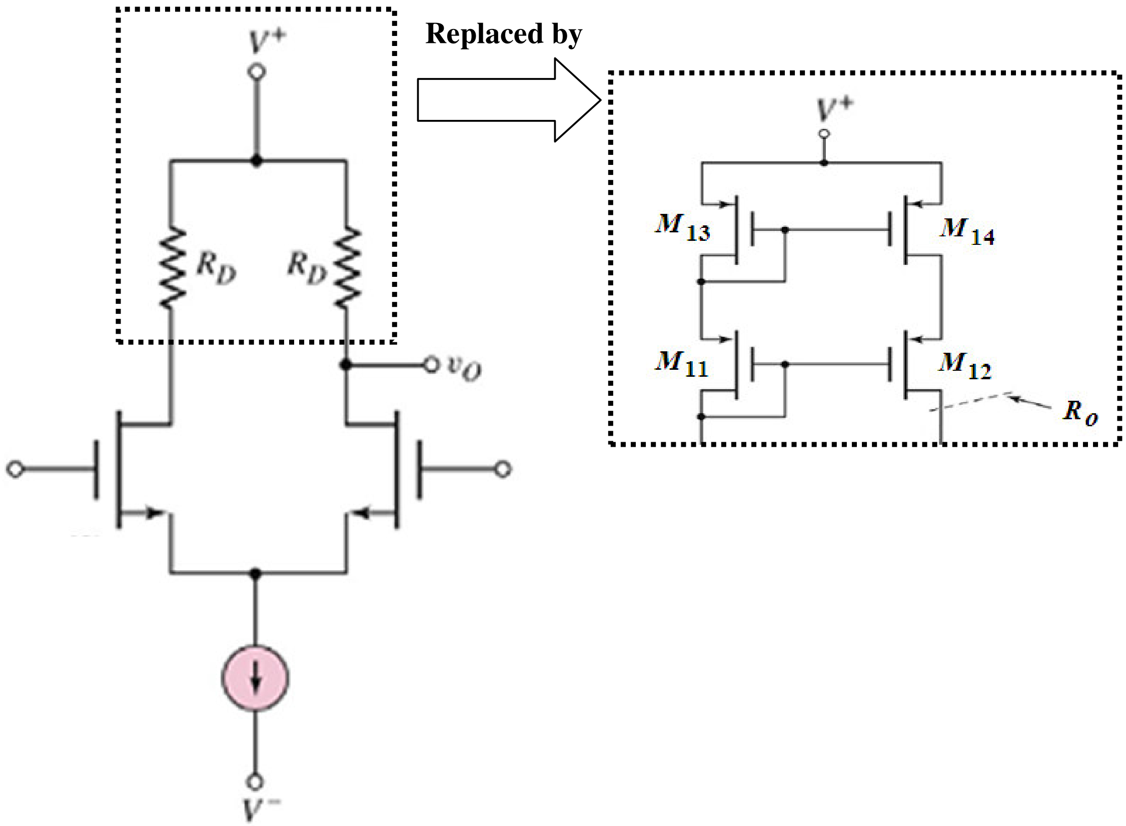


Figure 3

r_{o2}	$= 1/(\lambda I_{D2})$	$= 1/[(0.02)(0.29m)]$	$= 172.4\ k\Omega$	[1]
$r_{o12} = r_{o14} = r_{o2} = 172.4k$				[1]
g_m	$= 2[\sqrt{(K_n I_D)}]$	$= (I_Q)/[V_{DS2}(sat)]$	$= 0.725\ mA/V$	
R_o	$= (0.725m)(172.4k)(172.4k)$		$= 21.548\ M\Omega$	[1]
R_{out}	$= r_{o2} \parallel R_o$	$\approx r_{o2}$	$= 172.4\ k\Omega$	[1]
A_d	$= g_m R_{out}$	$= (0.725m)(172.4k\Omega) = 124.99$		[1]

-End of Questions-