UNIVERSITI TENAGA NASIONAL

COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 3 2011 / 2012

PROGRAMME	: **Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	: **EEEB273**
SUBJECT	: **ELECTRONIC ANALYSIS AND DESIGN II**
DATE	: **May 2012**
TIME	: **3 hours**

INSTRUCTIONS TO CANDIDATES:

1. This question paper contains **SIX (6)** questions in **THIRTEEN (13)** pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided.
4. Write answer to each question on **a new page**.
5. For all calculations, assume that V_T **= 26 mV**.
6. Use at least **4 significant numbers** in all calculations.

THIS QUESTION PAPER CONSISTS OF THIRTEEN (13) PRINTED PAGES INCLUDING THIS COVER PAGE AND APPENDIX.

Question 1 [16 marks]

(a) A basic **three-transistor current source** consists of matched **npn transistors Q_1, Q_2, and Q_3**, has output current (I_O) and reference current (I_{REF}). A resistor R_1 is used to establish I_{REF}. The circuit parameters are **$V^+ = 3$ V** and **$V^- = -3$ V**, and the transistor parameters are **$V_{BE}(on) = 0.7$ V, $\beta = 50$**, and $V_A = \infty$.

(i) Let the second transistor, Q_2, be the output transistor. **Draw and label** the circuit and its components **clearly**.

[3 marks]

(ii) If the output current is **0.25 mA**, what are the values of I_{REF} and R_1?

[4 marks]

(iii) **Discuss the advantage** of a BJT three-transistor current source over **two-transistor current source**.

[2 marks]

(b) For a MOSFET current source shown in **Figure 1**, the transistor parameters are k'_n **= 100 μA/V²**, V_{TN} **= 0.4 V** and λ **= 0.01** V^{-1}. Given that V^+ **= 2.5 V**, V^- **= -2.5 V**, I_{REF} **= 100 μA**, I_O **= 60 μA**, and V_{DS2}**(sat) = 0.4 V,** find:

(i) The width-to-length (**W/L**) ratio for all transistors in the circuit.

[5 marks]

(ii) How much the output current (I_O) would change if the output voltage at V_{D2} changes by **3V**?

[2 marks]

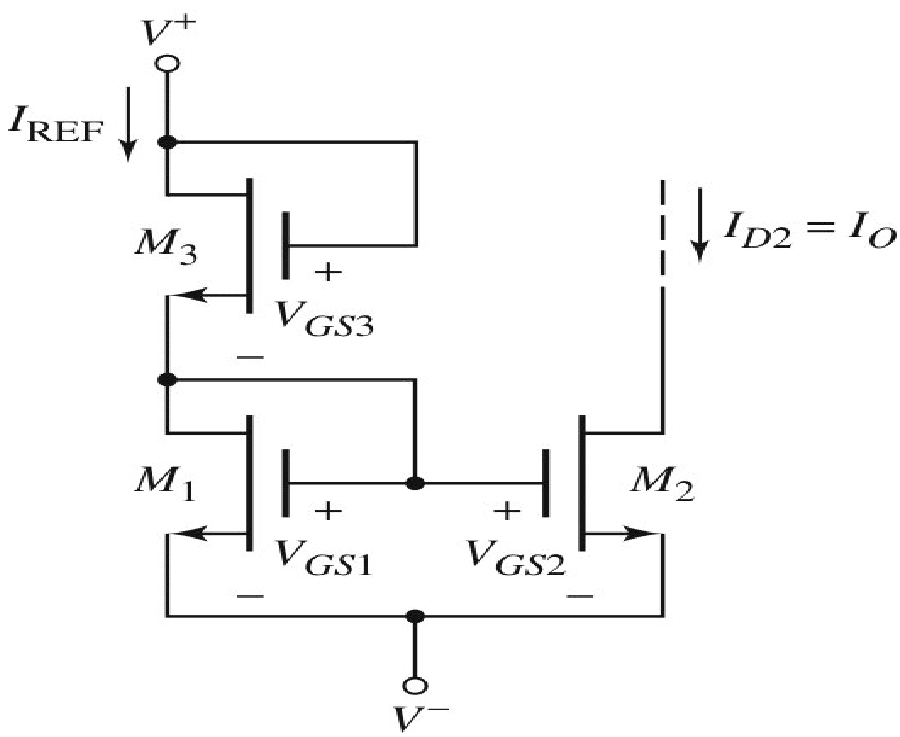

Figure 1

Question 2 [16 marks]

(a) Consider the BJT differential amplifier in **Figure 2a**. Study **Figure 2a** carefully. The circuit and transistor parameters are $\boldsymbol{I_Q}$ **= 1 mA**, $\boldsymbol{\beta}$ **= 100**, and **Early voltage** $V_A = \infty$.

(i) **Design** the circuit such that **one-sided** differential-mode **output** voltage at $\boldsymbol{v_{C2}}$ **= 7.5 V** when a differential-mode input voltage of $\boldsymbol{v_d}$ **= 0.05 V** is applied.

[4 marks]

(ii) **Determine** the differential-mode input resistance ($\boldsymbol{R_{id}}$).

[2 marks]

(iii) **Determine** the $\boldsymbol{CMRR_{dB}}$ when the common-mode voltage gain ($\boldsymbol{A_{cm}}$) is **-0.2 V/V.**

[2 marks]

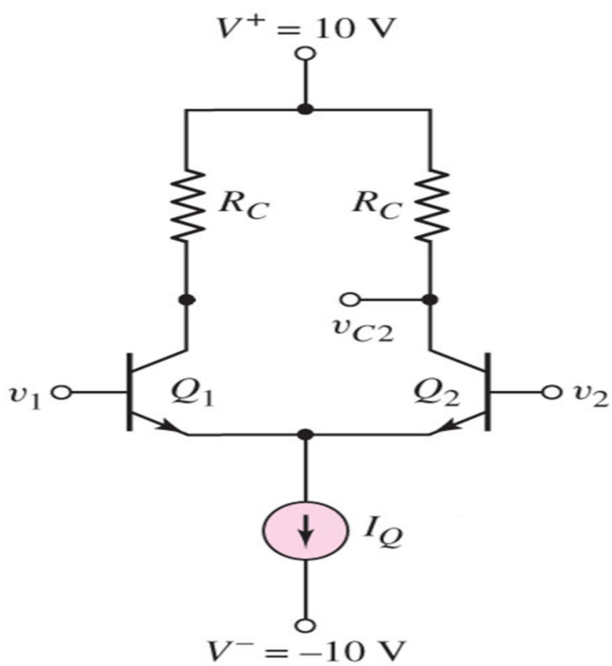

Figure 2a

(b) The BJT differential amplifier shown in **Figure 2b** is biased by a **0.18 mA** constant current source (i.e. I_Q = **0.18 mA**). It is to be redesigned to use an active load in order to increase its differential-mode voltage gain (A_d). The active load to be used is a **BJT Wilson current source** using **pnp transistors** to replace the collector resistors (R_C) in the differential amplifier, as graphically shown in **Figure 2b**.

The transistor parameters are $\beta = 150$, $V_{BE}(\text{on}) = V_{EB}(\text{on}) = 0.7$ V, $V_{AN} = 120$ V, and $V_{AP} = 100$ V. **The one-sided output** voltage taken at v_{C2} can be calculated using:

$$v_O = v_{C2} = g_{m2}\, v_d\, (r_{O2} \parallel R_{OAL})$$

where R_{OAL} is the output resistance of the **BJT Wilson current source**.

(i) **Draw the new circuit** incorporating the **active load's full circuit diagram**. Label the circuit correctly and clearly with appropriate symbols and numbering for transistors used in circuit. Leave I_Q symbol as it is in the **Figure 2b**.

[4 marks]

(ii) **Find** the output resistance of the **BJT Wilson current source** (R_{OAL}).

[2 marks]

(iii) **Determine** the differential-mode voltage gain (A_d) of **the new circuit**.

[2 marks]

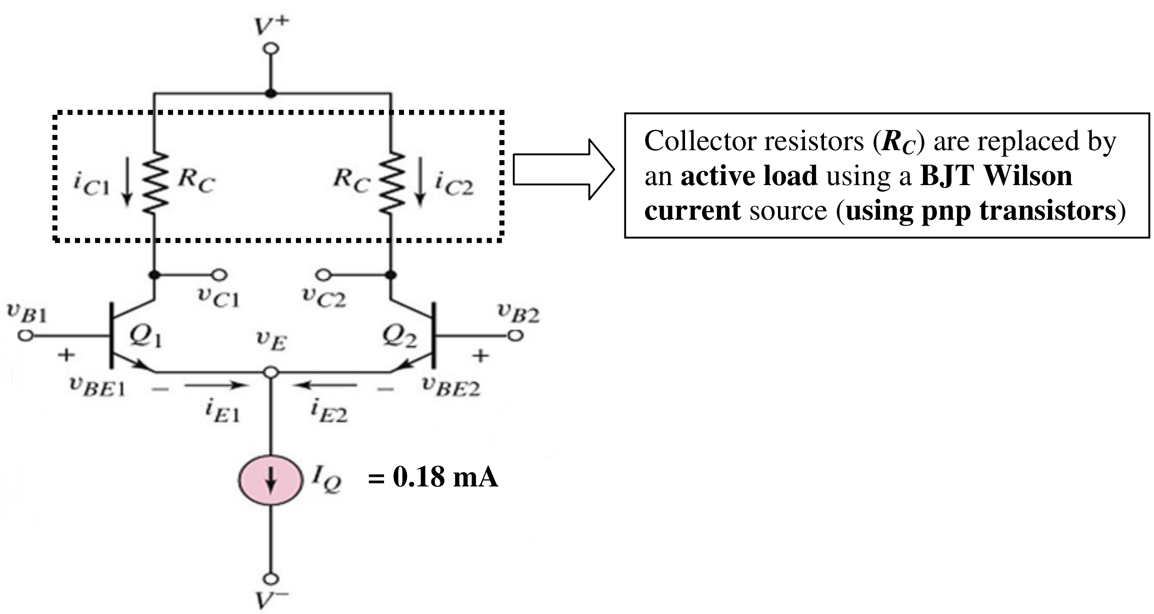

Figure 2b

Question 3 [16 marks]

(a) Consider the MOSFET differential amplifier with an active load as shown in **Figure 3a**. The transistors parameters are $\boldsymbol{V_{TN} = 1}$ **V,** $\boldsymbol{V_{TP} = -1}$ **V,** $\boldsymbol{K_n = 90}$ **μA/V²,** $\boldsymbol{K_p = 60}$ **μA/V²,** $\boldsymbol{I_Q = 0.4}$ **mA,** $\boldsymbol{\lambda_n = 0.02}$ $\mathbf{V^{-1}}$ and $\boldsymbol{\lambda_p = 0.01}$ $\mathbf{V^{-1}}$. Assume that the differential amplifier transistors $\boldsymbol{M_1}$ **and** $\boldsymbol{M_2}$ **are identical** and active load transistors $\boldsymbol{M_3}$ **and** $\boldsymbol{M_4}$ **are identical**. Determine:

(i) The **output resistance** of the amplifier.

[3 marks]

(ii) The **differential-mode** voltage gain.

[3 marks]

(iii) The **output voltage,** $\boldsymbol{v_O}$**,** if the differential input voltage applied is $\boldsymbol{v_d}$ **= (20 sin ωt) μV**.

[1 mark]

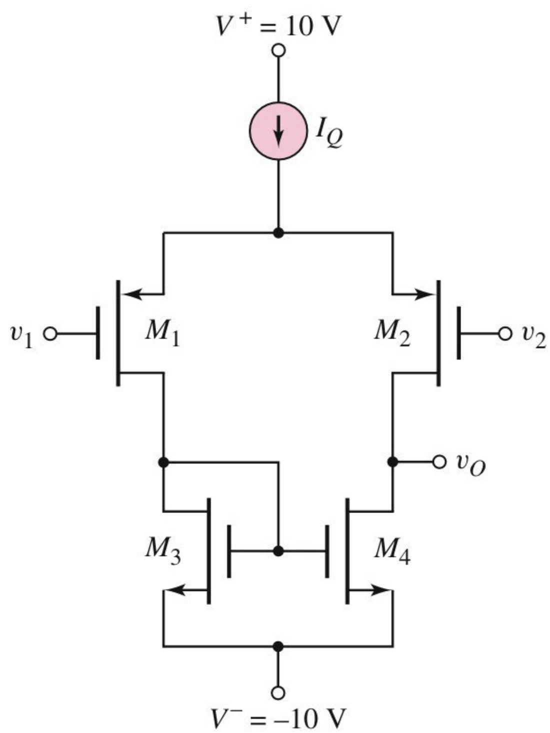

Figure 3a

(b) Consider the multistage bipolar circuit in **Figure 3b**, in which base currents are negligible. The transistors and circuits parameters are: V_{BE}**(on) = 0.7 V**, β **= 100** and $V_A = \infty$, R **= 12 kΩ**, R_C **= 4 kΩ**, R_{E1} **= 2.6 kΩ**, R_{E2} **= 2.43 kΩ**, I_Q **= 0.5 mA**, I_{CQ3} **= 0.5 mA** and I_{CQ4} **= 3 mA**. Determine:

(i) The **output voltage** v_{O2}, v_{O3}, and v_O when $v_1 = v_2 = 0$ **V**.

[3 marks]

(ii) The **overall voltage gain** (v_O/v_d) if the voltage gain of the second stage (i.e. v_{O3}/v_{O2}) = **-1.47 V/V**.

[6 marks]

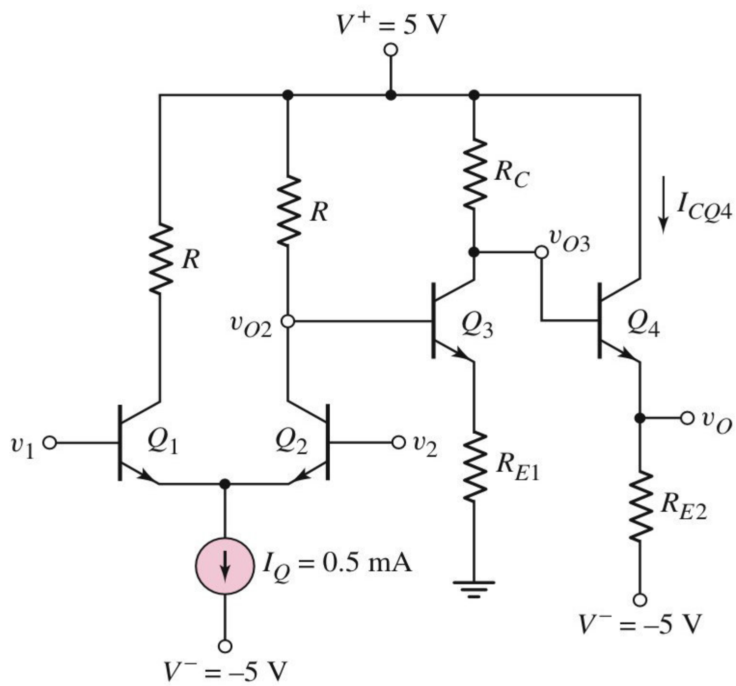

Figure 3b

Question 4 [16 marks]

(a) **Figure 4a** shows reference circuit and gain stage of **741 op-amp**. Transistors Q_{12} and Q_{13} form a current mirror, and Q_{13B} has a scale factor **0.70** times that of Q_{12}. Power supply voltages are $V^+ = +12$ **V** and $V^- = -12$ **V.** Assume $V_{BE} = V_{EB} = 0.6$ **V** and $\beta = 200$ for npn transistors. **Calculate** I_{REF} and I_{C16}.

[8 marks]

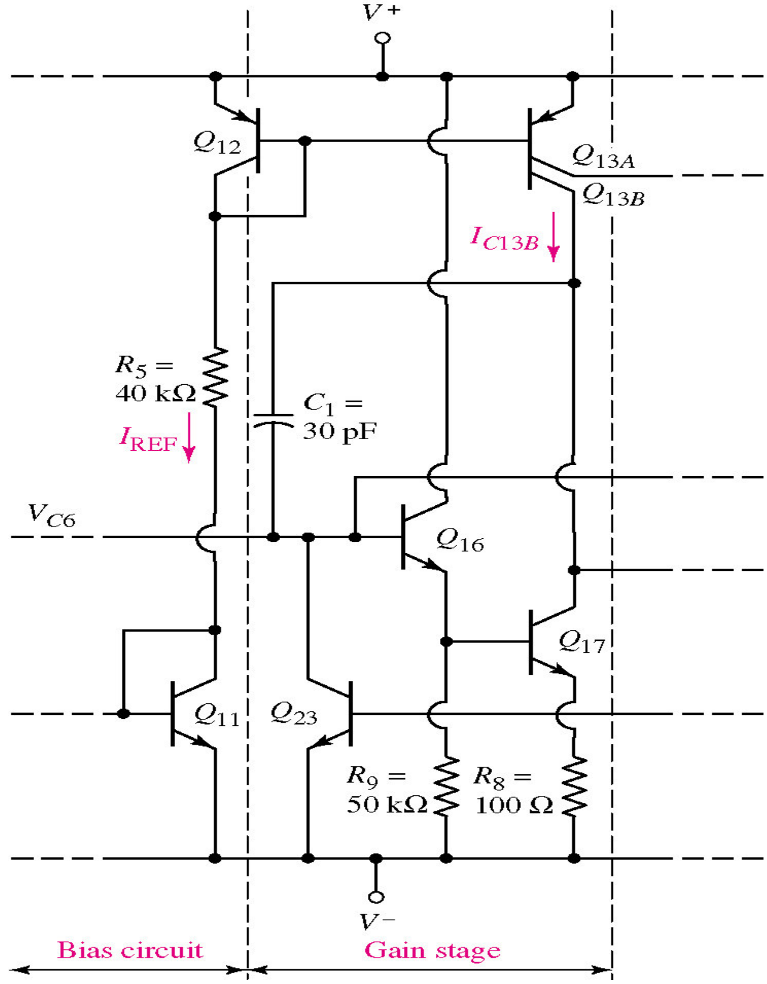

Figure 4a

(b) A MOSFET op-amp circuit as shown in **Figure 4b** is biased with $\boldsymbol{I_Q = 200\ \mu A}$. The transistor parameters are $\boldsymbol{k'_n = 100\ \mu A/V^2}$, $\boldsymbol{k'_p = 40\ \mu A/V^2}$, $\boldsymbol{V_{TN} = 0.4\ V}$, $\boldsymbol{V_{TP} = -0.4\ V}$, and $\boldsymbol{\lambda_n = \lambda_p = 0}$. The transistor aspect ratios are $\boldsymbol{(W/L)_1 = (W/L)_2 = 20}$, $\boldsymbol{(W/L)_3 = 50}$, and $\boldsymbol{(W/L)_4 = 40}$.

(i) **Design** the circuit (i.e. find the values of $\boldsymbol{R_{D1}}$, $\boldsymbol{R_{D2}}$, and $\boldsymbol{R_S}$) such that $\boldsymbol{I_{D3} = 150\ \mu A}$, $\boldsymbol{I_{D4} = 200\ \mu A}$, and $\boldsymbol{v_o = 0}$ for $\boldsymbol{v_1 = v_2 = 0}$.

[6 marks]

(ii) **Find** the differential voltage gain ($\boldsymbol{A_d}$) of the differential amplifier in the circuit.

[2 marks]

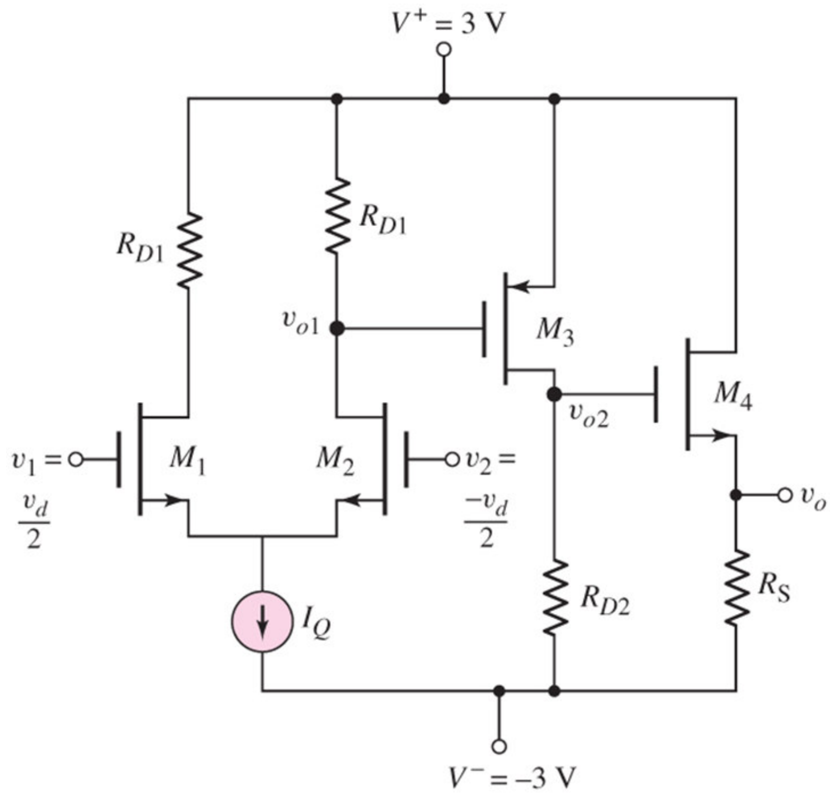

Figure 4b

Question 5 [16 marks]

Study the output stage circuit shown in **Figure 5** carefully. Let $R_L = 1\ k\Omega$, $V_{BB} = 1.40\ V$ and the reverse saturation current for the transistors, $I_S = 2 \times 10^{-15}$ **A**. **Assume** $\beta >> 1$.

(a) **Explain** the "cross-over distortion" phenomenon in **class-B output stage**.

[3 marks]

(b) What is the **advantage** of the output stage shown in **Figure 5** compared to the **class-A** and **class-B** output stages?

[2 marks]

(c) Referring to **Figure 5**, for the case of the output voltage $v_O = -4\ V$, **determine** i_L, i_{Cp}, and i_{Cn}.

[7 marks]

(d) Referring to **Figure 5**, for the case of the output voltage $v_O = -4\ V$, **calculate** the power dissipated in transistor Q_n and Q_p.

[4 marks]

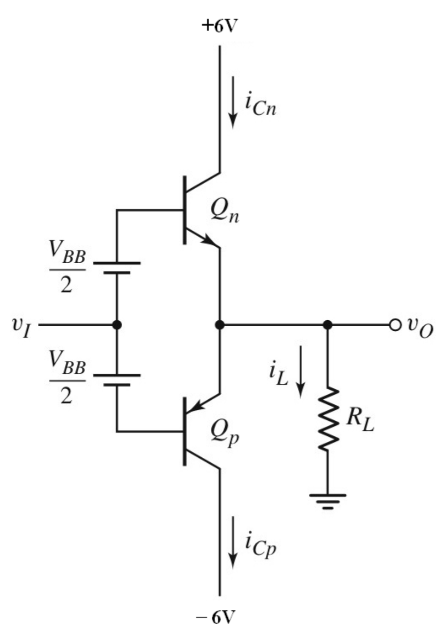

Figure 5

Question 6 [20 marks]

(a) **States** four **(4)** applications of an ideal operational amplifier.

[4 marks]

(b) Consider the two inverting op-amp circuit connected in cascade as shown in **Figure 6a**. Let $\boldsymbol{R_1 = 20\ k\Omega}$, $\boldsymbol{R_2 = 100\ k\Omega}$, $\boldsymbol{R_3 = 80\ k\Omega}$, and $\boldsymbol{R_4 = 40\ k\Omega}$. Find v_O/v_I for the circuit.

[6 marks]

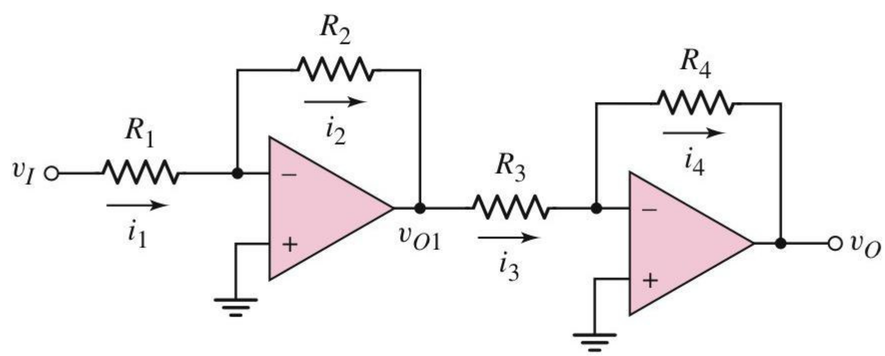

Figure 6a

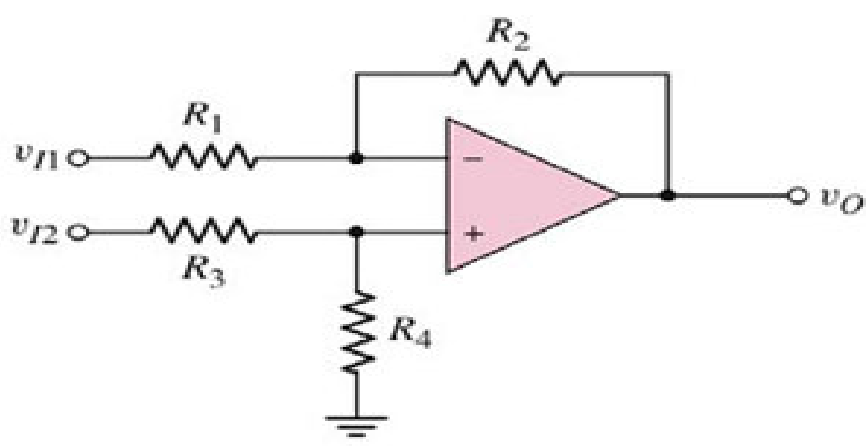

Figure 6b

(c) **A general output equation** for a difference amplifier shown in **Figure 6b** is

$$v_O = A_d v_d + A_{cm} v_{cm}$$

For the difference amplifier in **Figure 6b**, the circuit parameters are $\boldsymbol{R_1 = R_3 = 10\ k\Omega}$, $\boldsymbol{R_2 = 100\ k\Omega}$, and $\boldsymbol{R_4 = 110\ k\Omega}$ and the output voltage equation is as follows:

$$v_O = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4 / R_3}{1 + R_4 / R_3}\right) v_{I2} - \left(\frac{R_2}{R_1}\right) v_{I1}$$

where
$$v_{I1} = v_{cm} - \frac{v_d}{2}$$

and
$$v_{I2} = v_{cm} + \frac{v_d}{2}$$

Find $\boldsymbol{A_d}$, $\boldsymbol{A_{cm}}$, and then calculate the ***CMRR* in dB**.

[10 marks]

-END OF QUESTION PAPER-

APPENDIX

BASIC FORMULA

BJT

$$i_C = I_S e^{v_{BE}/V_T} \text{ ;npn}$$

$$i_C = I_S e^{v_{EB}/V_T} \text{ ;pnp}$$

$$i_C = \alpha i_E = \beta i_B$$

$$i_E = i_B + i_C$$

$$\alpha = \frac{\beta}{\beta + 1}$$

;Small signal

$$\beta = g_m r_\pi$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

MOSFET

;N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n [v_{GS} - V_{TN}]^2$$

$$K_n = \frac{k_n'}{2} \cdot \frac{W}{L}$$

;P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p [v_{SG} + V_{TP}]^2$$

$$K_p = \frac{k_p'}{2} \cdot \frac{W}{L}$$

;Small signal

$$g_m = 2\sqrt{K_{?} I_{DQ}}$$

$$r_o \cong \frac{1}{\lambda I_{DQ}}$$