COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 1   2012 / 2013

PROGRAMME	: **Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	: **EEEB273**
SUBJECT	: **ELECTRONIC ANALYSIS AND DESIGN II**
DATE	: **September 2012**
TIME	: **3 hours**

INSTRUCTIONS TO CANDIDATES:

1. This question paper contains **SIX (6)** questions in **ELEVEN (11)** pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided.
4. Write answer to each question on **a new page**.
5. For all calculations, assume that V_T **= 26 mV**.
6. Use at least **4 significant numbers** in all calculations.

THIS QUESTION PAPER CONSISTS OF ELEVEN (11) PRINTED PAGES INCLUDING THIS COVER PAGE AND APPENDIX.

Question 1 [16 marks]

(a) Consider the **Widlar current source** as in **Figure 1a**. Let I_O **= 20 µA** and R_E **= 4.2kΩ**. Neglect base currents and assume I_{S1} **= 4 x 10^{-15} A**. **Determine** I_{REF}, V_{BE1}, V_{BE2}, and R_1.

[8 marks]

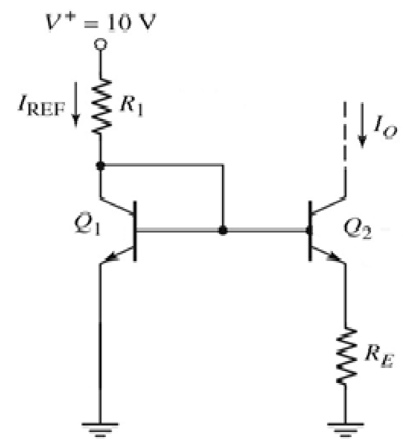

Figure 1a

(b) Refer to **Figure 1b**. Consider the **cascode current source** with parameters V^+ **= 5 V,** V^- **= -5 V,** and I_{REF} **= 200 µA** at V_{GS1} **= 1.8 V**. All transistors are matched and operating in saturation region with parameters g_m **= 0.3 mA/V^2** and λ **= 0.025V^{-1}**. **Determine** I_o at V_{D4} **= +2.5 V**.

[8 marks]

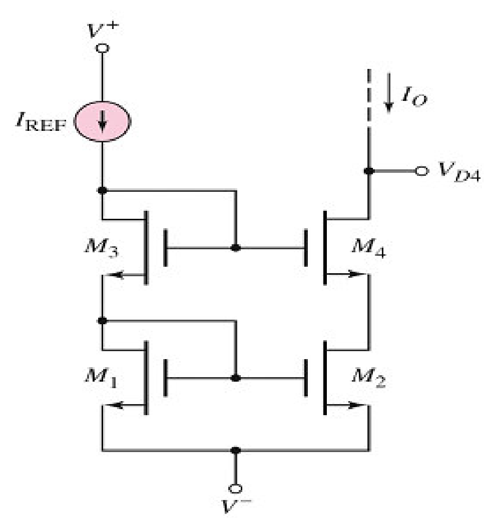

Figure 1b

Question 2 [16 marks]

(a) The basic differential pair is shown in **Figure 2a**. It is given that V^{+} **= 15 V**, V^{-} **= -15 V**, R_C **= 5 kΩ**, I_Q **= 2 mA**, and transistor parameters are β **= 100**, V_A **= 100 V**, V_{BE}**(on) = 0.7 V**, V_{CE}**(sat) = 0.3 V**.

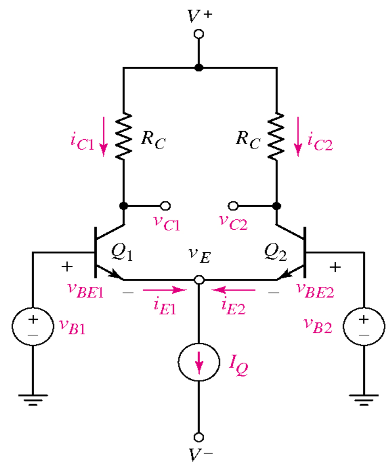

Figure 2a

(i) **Calculate** the **one-sided** small-signal differential voltage gain (A_d) of the differential amplifier. [2 marks]

(ii) The constant current source of **Figure 2a** that is providing the current I_Q is implemented using the **basic two transistor current source**. **Find** the value of A_{cm}, the **common-mode voltage gain** of the differential-amplifier, using **equation given below**. Assume $R_B = 0$. [2 marks]

$$A_{cm} = \frac{-g_m R_C}{1 + \frac{2(1+\beta)R_O}{r_\pi + R_B}}$$

(iii) The input voltages for the differential amplifier are $v_{B1} = 210 \times 10^{-6} \sin \omega t$ **V** and $v_{B2} = 190 \times 10^{-6} \sin \omega t$ **V**. **Calculate the output voltage** of the differential amplifier **applying superposition theorem**, taking into account the effect of the non-ideal current source. **Use values from previous calculations**. **What** is the output voltage if an ideal current source is used instead? **Justify** your answer. [4 marks]

(iv) **Calculate** the value of ***Vcm*****(max)** of this differential amplifier. [4 marks]

(b) The differential amplifier shown in **Figure 2b** has a **three-transistor current mirror** connected as an **active load**. The circuit is connected to power supply voltages of $\boldsymbol{V^+}$ **= +5 V** and $\boldsymbol{V^-}$ **= -5 V**.

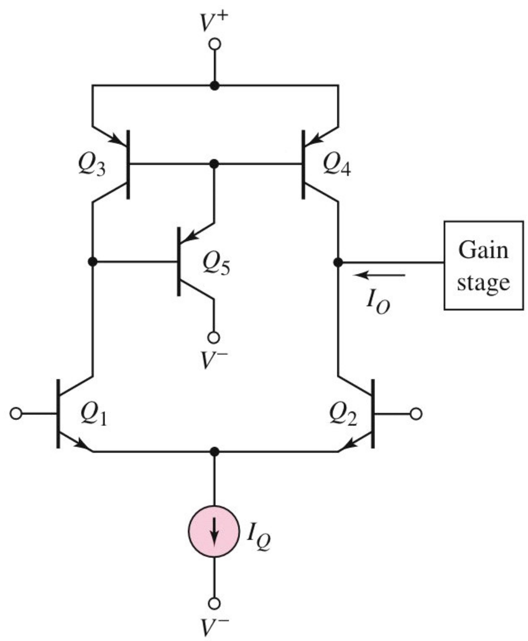

Figure 2b

(i) **Determine** the relationship between $\boldsymbol{I_O}$ and $\boldsymbol{I_Q}$ such that the amplifier **dc currents are balanced**. [3 marks]

(ii) **Calculate** the value of $\boldsymbol{I_O}$ given that $\boldsymbol{I_Q}$ **= 0.2 mA** and $\boldsymbol{\beta}$ **=100**. [1 mark]

Question 3 [16 marks]

Figure 3 shows a differential amplifier circuit with active loads and biased by a current source using **MOSFET**. Transistors M_1 and M_2 are driven into saturation with $V_{DS}(\text{sat}) = 1.12$ **V**. The active load transistors (M_3 and M_4) are matched with parameters $K_p = 0.1\ \text{mA/V}^2$, $V_{TP} = -2\ \text{V}$, and $\lambda_p = 0.02\ \text{V}^{-1}$. Transistors M_5, M_6 and M_7 are **identical**. All the **NMOS transistors** have the same $K_n = 0.2\ \text{mA/V}^2$, $V_{TN} = 2$ V, and $\lambda_n = 0.015\ \text{V}^{-1}$.

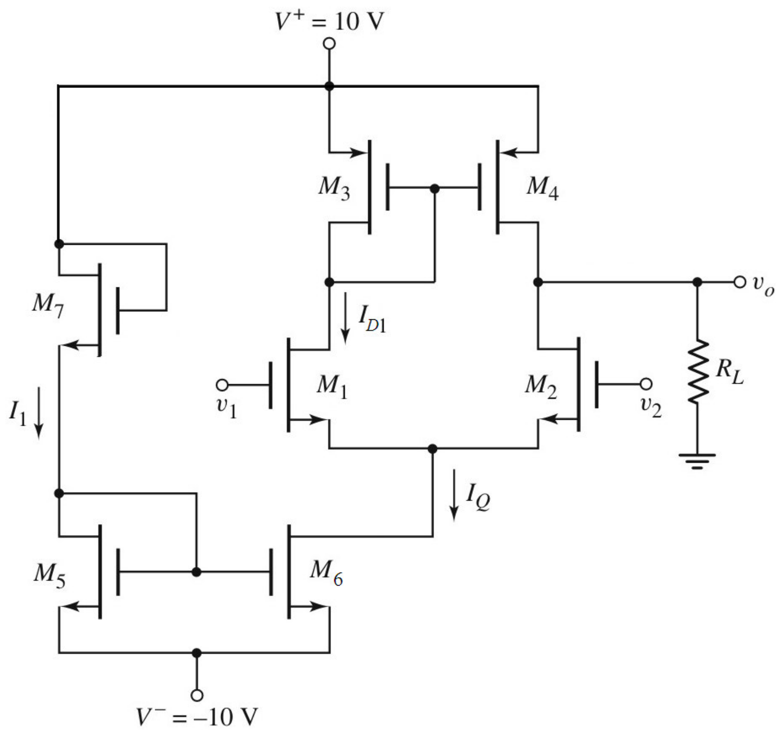

Figure 3

(a) Determine I_1, I_Q, and I_{D1} when $v_1 = v_2 = 0$. [5 marks]

(b) Determine the **one-sided differential mode voltage gain** (A_d) for the differential amplifier if $R_L = 100\ \text{k}\Omega$. [6 marks]

(c) It is required that the **CMRR** of the circuit to be **60 dB**. **What** is the **common mode voltage gain** (A_{cm})? [3 marks]

(d) **Suggest 2 ways** to improve the **CMRR** for the circuit in the **Figure 3**. [2 marks]

Question 4 [16 marks]

Consider the **input stage and bias circuit** of the **741 operational amplifier** in **Figure 4a**, with V^+ **= 5 V** and V^- **= -5 V**, V_A **= 50 V**, $V_{BE6} = V_{BE7}$ **= 0.6 V**, β **= 200** and I_{C9} **= 10 µA**. The reverse saturation current $I_S = 10^{-14}$ **A** for each transistor and the current flow through resistor R_5 is **0.4 mA**. Ignore the base currents for dc calculations and assume the **dc currents in the input stage are exactly balanced**.

(a) What is the **purpose** of Q_3 and Q_4 in the circuit? [2 marks]

(b) **Determine** the resistance R_4. [4 marks]

(c) **Calculate** the value of $r_{\pi6}$. [2 marks]

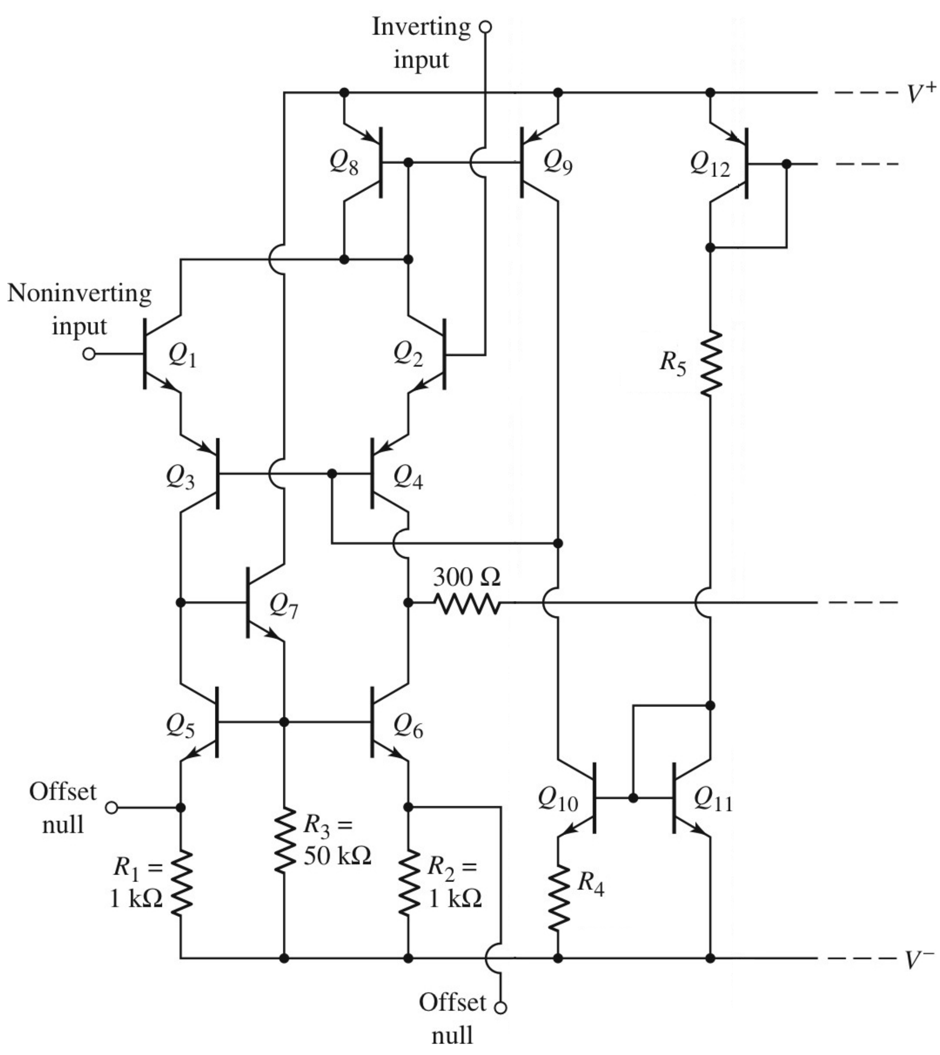

Figure 4a

(d) **Figure 4b** shows the **ac equivalent circuit** of the input stage of the **741 op-amp** shown in the **Figure 4a**. **Determine** the effective output resistance, R_O, looking at v_{o1}. **Neglect** the effective resistances in the emitters of Q_4 and Q_2.

(Hint: The output resistance (R_O) of a **Widlar current source** can be calculated using the following formula: $R_O = r_o\,[1 + g_m\,(r_\pi \parallel R_E)]$).

[8 marks]

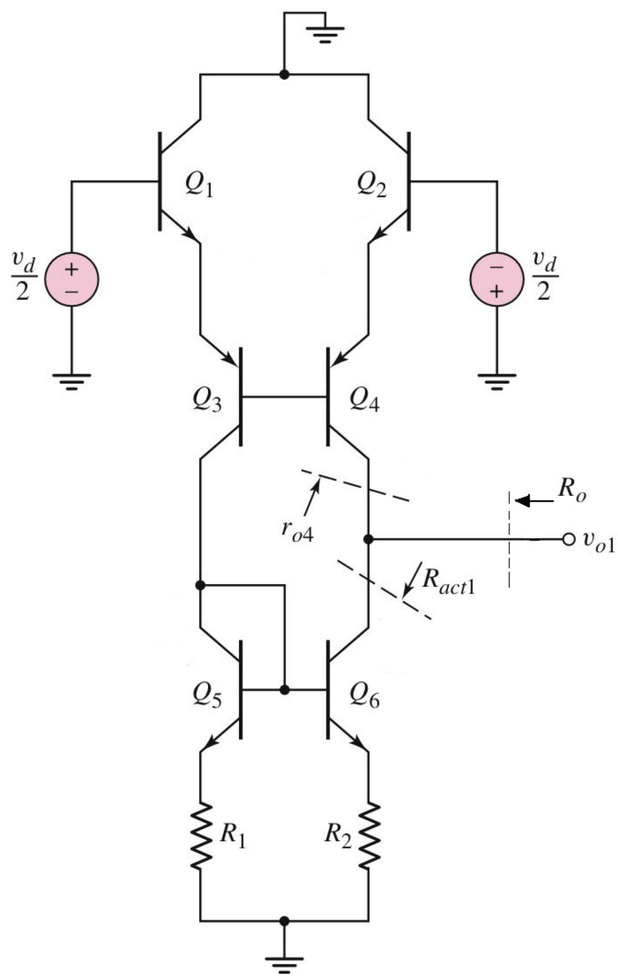

Figure 4b

<u>Question 5 [16 marks]</u>

(a) **State** the main disadvantage of both **Class A** and **Class B** output stages. **Comment** on the **power conversion efficiency** of both output stages. [2 marks]

(b) The circuit parameters for the **emitter follower** circuit in **Figure 5** is V^+ **= 10 V**, V^- **= -10 V**, and R_L **= 1 kΩ**. The transistor parameters are V_{BE}**(on) = 0.7 V**, V_{CE}**(sat) = 0.2 V,** and $V_A = \infty$. **Neglect** base currents. The **output voltage** is varying from **-8 V** to **+8 V**.

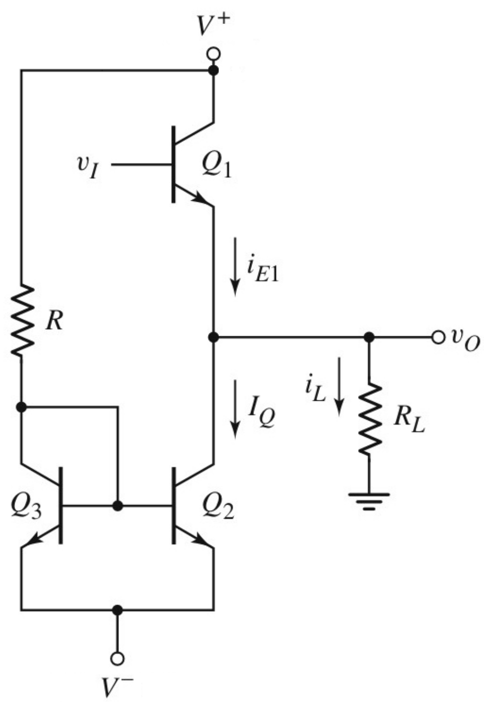

Figure 5

(i) **Find** the required I_Q and the value of R. [4 marks]

(ii) For v_O **= 0 V**, **find** the power dissipated in the transistor Q_1, and the power dissipated in the current source (Q_2, Q_3, and R). [5 marks]

(iii) **Determine** the conversion efficiency for a symmetric sine-wave output voltage with peak value of **8 V**. [5 marks]

Question 6 [20 marks]

(a) **Find** the voltage gain, $A_v = v_O/v_I$, for the circuit in **Figure 6a**. Assume that the op-amp is ideal. [5 marks]

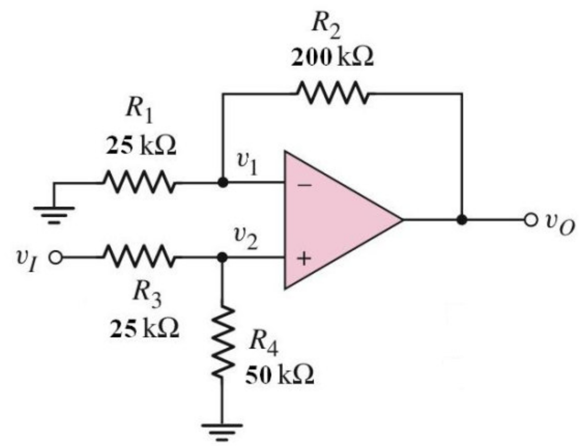

Figure 6a

(b) Consider the two inverting op-amp circuit connected in cascade as shown in **Figure 6b**. Let R_1 **= 20 kΩ**, R_2 **= 100 kΩ**, R_3 **= 150 kΩ**, and R_4 **= 60 kΩ**. Find v_O when $v_I = 0.12$ **V**. [4 marks]

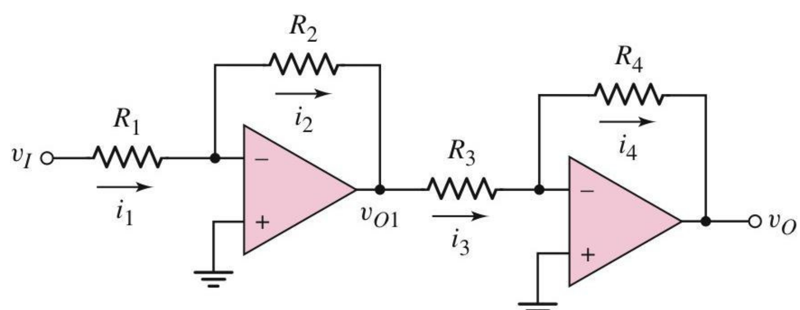

Figure 6b

(c) **Figure 6c**, in next page, shows a design for an **instrumentation amplifier** using op-amps. In the design, R_{1POT} is a **100 kΩ potentiometer** (or a variable resistor) used **to provide variable resistance** so that differential voltage gain (A_v) of the instrumentation amplifier can be adjustable. With analysis, it can be shown that

$$v_O = \frac{R_4}{R_3}\left(1 + \frac{2R_2}{R_1 + R_{1POT}}\right)(v_{I2} - v_{I1})$$

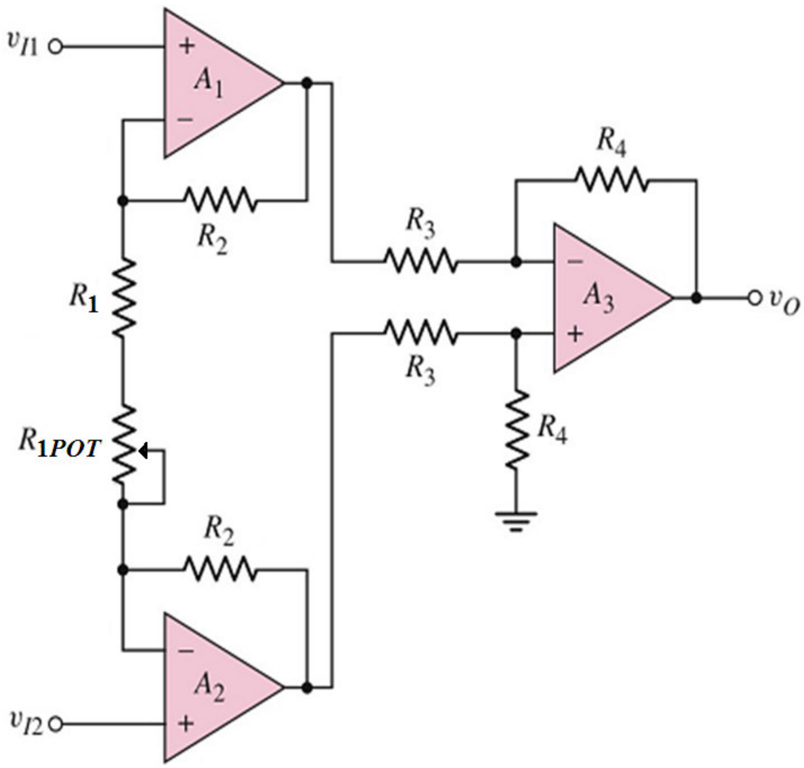

Figure 6c

(i) **What** is the name of an amplifier represented by op-amp A_3, R_3, and R_4 in the **Figure 6c**? [1 mark]

(ii) With $R_3 = R_4 = 100\ k\Omega$, **design an instrumentation amplifier** using the circuit as shown in the **Figure 6c** to realize a differential voltage gain (A_v) adjustable from **10 to 100.** (Hints: A_v is smallest when R_{1POT} is at maximum value. You are required to determine the value of R_1 and R_2 in the circuit). [7 marks]

(iii) With $v_{I1} = 1.00$ V, $v_{I2} = 1.15$ V, $R_4 = 2\ R_3$, R_{1POT} is set at **40 kΩ**, and using the values of R_1 and R_2 found in **step (ii)** above, **calculate** A_v and v_O. [3 marks]

-END OF QUESTION PAPER-

APPENDIX

BASIC FORMULA

BJT

$$i_C = I_S e^{v_{BE}/V_T} \text{; npn}$$

$$i_C = I_S e^{v_{EB}/V_T} \text{; pnp}$$

$$i_C = \alpha i_E = \beta i_B$$

$$i_E = i_B + i_C$$

$$\alpha = \frac{\beta}{\beta + 1}$$

;Small signal

$$\beta = g_m r_\pi$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

MOSFET

;N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n [v_{GS} - V_{TN}]^2$$

$$K_n = \frac{k_n'}{2} \cdot \frac{W}{L}$$

;P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p [v_{SG} + V_{TP}]^2$$

$$K_p = \frac{k_p'}{2} \cdot \frac{W}{L}$$

;Small signal

$$g_m = 2\sqrt{K_{?} I_{DQ}}$$

$$r_o \cong \frac{1}{\lambda I_{DQ}}$$