Name:

Student ID Number:

Section: **01/02/03/04/05 A/B**

Lecturer: **Dr Jamaludin / Dr Azni Wati / Dr Fazrena Azlee**

UNIVERSITI TENAGA NASIONAL

College of Engineering

Department of Electronics and Communication Engineering

Test 2

SEMESTER 1, ACADEMIC YEAR 2012/2013

Subject Code	:	**EEEB273**
Course Title	:	**Electronics Analysis & Design II**
Date	:	**3 August 2012**
Time Allowed	:	**1.5 hours**

Instructions to the candidates:

1. Write your Name and Student ID number. Circle your section number.
2. **Write all your answers using pen**. **DO NOT USE PENCIL** except for the diagram.
3. **ANSWER ALL QUESTIONS.**
4. **WRITE YOUR ANSWER ON THIS QUESTION PAPER.**
5. For BJT, use V_T **= 26 mV** where appropriate.
6. Use at least **4 significant numbers** in all calculations.

NOTE: DO NOT OPEN THE QUESTION PAPER UNTIL INSTRUCTED TO DO SO.

☺ **GOOD LUCK!** ☺

Question No.	1	2	3	Total
Marks				

Question 1 **[40 marks]**

The circuit parameters for the differential amplifier shown in **Figure 1** are $V^+ = 5$ **V**, $V^- = -5$ **V**, $A_{cm} = -0.28$, and $I_Q = 240$ **μA**. The **NMOS** transistor parameters are $V_{TN} = 0.4$ **V**, $k'_n = 100$ **μA/V²**, $(W/L)_n = 8$, and $\lambda_n = 0.018$ **V⁻¹**. The **PMOS** transistor parameters are $V_{TP} = -0.4$ **V**, $k'_p = 40$ **μA/V²**, $(W/L)_p = 10$, and $\lambda_p = 0.02$ **V⁻¹**.

a) **Determine** the maximum **common-mode voltage input,** v_{cm}**(max),** that can be applied such that the transistors are **still biased in saturation region**. [6 marks]

b) **Draw the ac equivalent circuit** for the differential-mode input ($v_1 = +v_d/2$ and $v_2 = -v_d/2$). **Indicate** the resultant ac currents in all transistors. [6 marks]

c) **Determine** the output resistance R_o of the differential amplifier. [5 marks]

d) **Calculate** the small-signal differential-mode voltage gain $A_d = v_o/v_d$. [5 marks]

e) **Suggest** one way **to increase** the differential-mode voltage gain and **show** your new circuit and **justify** the change(s). [6 marks]

f) **Find** the **one-sided output voltage** (v_o) taken at v_{D2} of the differential amplifier when $v_1 = (0.10 + 0.05 \sin \omega t)$ **mV** and $v_2 = (-0.10 + 0.05 \sin \omega t)$ **mV.** [12 marks]

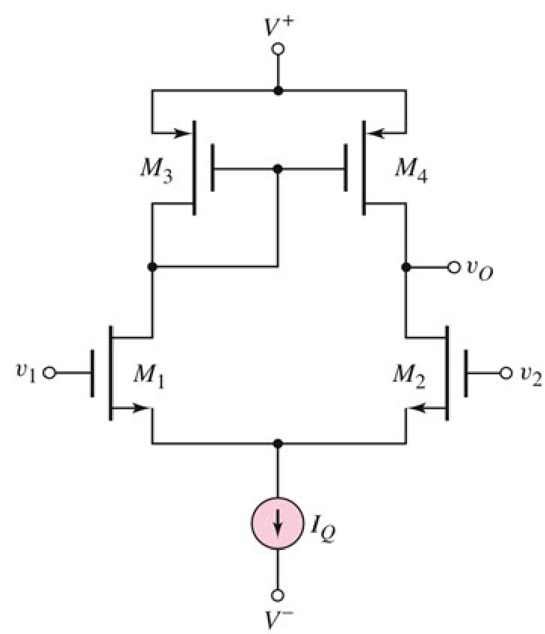


Figure 1

Answers for Question 1

(a) $V_{SG3} = [\sqrt{(I_{D3}/K_n)}] - V_{TP}$

$= [\sqrt{(I_Q/2)/[(k'_p/2)(W/L)_p]}] - V_{TP}$ (3)

$= [\sqrt{(120\mu)/[(40\mu/2)(10)]}] + 0.4$

$= 1.175$ V

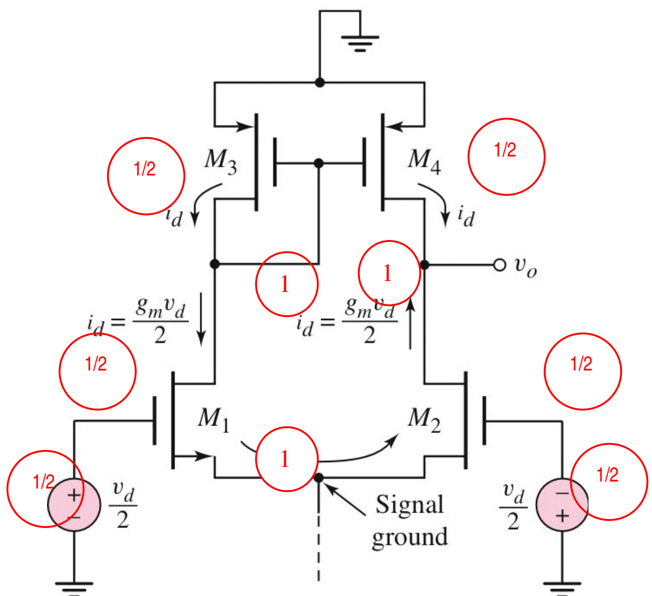
$v_{cm(\max)} = V^+ - V_{SG3} - V_{DS1(sat)} + V_{GS1}$

$= V^+ - V_{SG3} - (V_{GS1} - V_{TN}) + V_{GS1} = V^+ - V_{SG3} + V_{TN}$ (3)

$= 5 - 1.175 + 0.4$

$= 4.225$ V

(b)



Answers for Question 1 (Cont.)

(c)

r_{o2} = $1/(\lambda_n I_D) = [(0.018)(120\mu)]^{-1} = 463$ kΩ (2)

r_{o4} = $1/(\lambda_p I_D) = [(0.02)(120\mu)]^{-1} = 416.7$ kΩ (2)

R_o = $r_{o2} // r_{o4} = 219.3$ kΩ (1)

(d) R_o = $r_{o2} // r_{o4} = 219.3$ kΩ (1)

g_m = $2\sqrt{[K_n I_D]} = 2\sqrt{[(k'_n/2)(W/L)_n(I_Q/2)]}$ (2)

= $2\sqrt{[(100\mu/2)(8)(120\mu)]} = 0.4382$ mA/V^2

A_d = $g_m R_o = (0.4382\text{m})(219.3\text{k}) = 96.09$ (2)

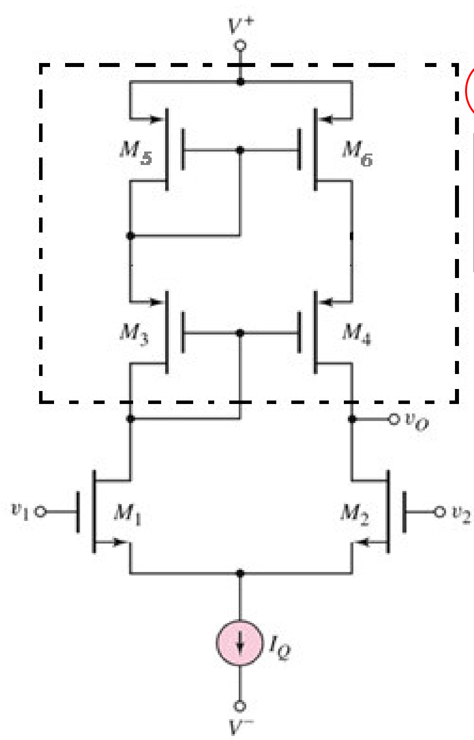
(e) **Increase voltage gain by using cascode active load.** (2)

$A_d = g_m R_o$ (1)

Previous $R_o = r_{o2} // r_{o4}$

New circuit $R_o = r_{o2} // R_o(\text{active load}) = r_{o2} // g_m r_{o4} r_{o6} \cong r_{o2}$ (1)

The new R_o **is larger than the previous one.**



(2)

-transistor type PMOS
-within cascode connections
-connection with diff-amp

Answers for Question 1 (Cont.)

(f) v_d $= v_1 - v_2$ (1)

$= (0.10 + 0.05 \sin \omega t) - (-0.10 + 0.05 \sin \omega t)$ (2)

$= 0.20$ mV (1)

v_{cm} $= (v_1 + v_2)/2$ (1)

$= [(0.10 + 0.05 \sin \omega t) + (-0.10 + 0.05 \sin \omega t)]/2$ (2)

$= 0.05 \sin \omega t$ mV (1)

v_O $= A_d v_d + A_{cm} v_{cm}$ (2)

$= (96.09)(0.2\text{mV}) + (-0.28)(0.05 \sin \omega t \text{ mV})$ (1)

$= (19.22 - 0.014 \sin \omega t)$ mV (1)

Question 2 **[30 marks]**

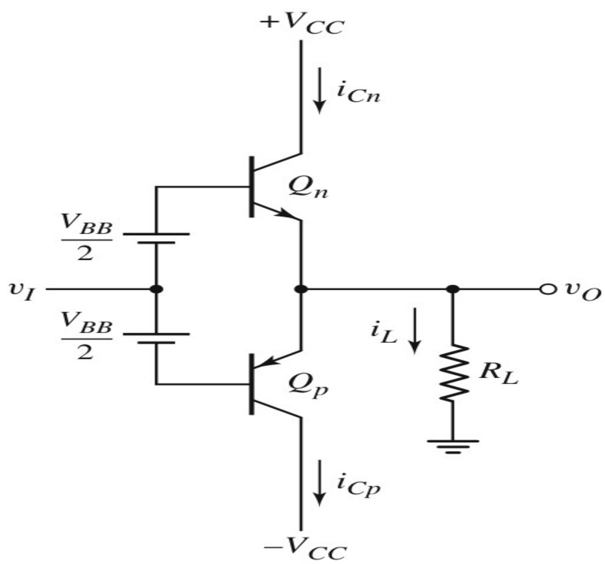


Figure 3

For a simplified class-AB output stage with BJTs in **Figure 3**, given that $\boldsymbol{V_{CC}}$ **= 5 V** and $\boldsymbol{R_L}$ **= 1 kΩ**. For each transistor, the reverse-bias saturation current is $\boldsymbol{I_S = 2 \times 10^{-15}}$ **A**.

a) **What** are two **disadvantages** of class-AB output stage compared to the class-B output stage? [4 marks]

b) **What** is the **advantage** of class-AB output stage compared to the class-B output stage? [2 marks]

c) **Determine** the value of $\boldsymbol{V_{BB}}$ that produces $\boldsymbol{i_{Cn} = i_{Cp}}$ **= 1.1 mA** when $\boldsymbol{v_I}$ **= 0 V**. **What** is the power dissipated in each transistor? [6 marks]

d) For $\boldsymbol{v_O}$ **= -3.6 V, determine** $\boldsymbol{i_L}$, $\boldsymbol{i_{Cn}}$, $\boldsymbol{i_{Cp}}$, and $\boldsymbol{v_I}$. Reiterate your calculation twice for $\boldsymbol{i_{Cn}}$ and $\boldsymbol{i_{Cp}}$. **What** is the power dissipated in $\boldsymbol{Q_n}$, $\boldsymbol{Q_p}$, and $\boldsymbol{R_L}$? [18 marks]

Answers for Question 2

a) i) Required power handling capability of ***Q***s in class-AB will be ***slightly larger*** than class-B.
ii) **Power Conversion Efficiency (*η*)** will be ***less*** than class-B.
[2 marks for each answer]

b) **Eliminating crossover distortion in the class-B.** [2 marks]

Answers for Question 2 (Cont.)

c)

i_{Cn}	$= I_S \exp(V_{BEn} / V_T)$	
V_{BEn}	$= V_T \ln(i_{Cn} / I_S)$	[1]
	$= (0.026) \ln (1.1 \text{x} 10^{-3} / 2 \text{x} 10^{-15}) = 0.70286$ V	[0.5, 0.5]
V_{BB}	$= 2\, V_{BE}$	[1]
	= 2 x 0.70286 = 1.40572 V	[0.5, 0.5]
P_Q	$= i_{Cn}\, v_{CE}$	[1]
	= (1.1m)(5V – 0V) = 5.5 mW	[0.5, 0.5]

d)

For v_O = -3.6 V,	i_L	$= v_O / R_L$	[1]
		= (-3.6V)/(1 kΩ) = -3.6 mA	[0.5, 0.5]
Approximation:	i_{Cp}	$\approx \lvert i_L \rvert$ = 3.6 mA	[1]
	v_{EBp}	$= V_T \ln(i_{Cp} / I_S)$	[0.5]
		$= (0.026) \ln(3.6 \text{x} 10^{-3} / 2 \text{x} 10^{-15}) = 0.73369$ V	[0.5]
	v_{BEn}	$= V_{BB} - v_{EBp}$	[1]
		= 1.40572 – 0.73369 = 0.67203 V	[0.5]
	i_{Cn}	$= I_S \exp(V_{BEn} / V_T)$	[1]
		$= (2 \text{x} 10^{-15}) \exp(0.67203 / 0.026) = 0.336026$ mA	[0.5]
Then, finally	i_{Cp}	$\approx i_{Cn} - i_L$	[1]
		= (0.336026m) - (-3.6m) = 3.936026 mA	[0.5]
	v_{EBp}	$= V_T \ln(i_{Cp} / I_S)$	
		$= (0.026) \ln(3.936026 \text{x} 10^{-3} / 2 \text{x} 10^{-15}) = 0.73601$ V	[0.5]
	v_{BEn}	$= V_{BB} - v_{EBp}$	
		= 1.40572 – 0.73601 = 0.66971 V	[0.5]
	i_{Cn}	$= I_S \exp(V_{BEn} / V_T)$	
		$= (2 \text{x} 10^{-15}) \exp(0.66971 / 0.026) = 0.307341$ mA	[0.5]
	i_{Cp}	$= i_{Cn} - i_L$	
		= (0.307341m) - (-3.6m) = 3.907341 mA	[0.5]
	v_I	$= v_O - v_{EBp} + V_{BB}/2$	[1]
		= (-3.6) - 0.73601 + 1.40572/2 = -3.63315 V	[0.5]
Power:			
For Q_n:	P_{Qn}	$= i_{Cn}\, v_{CEn}$	[1]
		= (0.307341m)(5-(-3.6)) = 2.643 mW	[0.5, 0.5]
For Q_p:	P_{Qp}	$= i_{Cp}\, v_{ECp}$	[1]
		= (3.907341m)(-3.6-(-5)) = 5.470 mW	[0.5, 0.5]
For R_L:	P_{RL}	$= i^2_L\, R_L$	[1]
		$= (-3.6 \text{ mA})^2 (1 \text{ k}\Omega) = 12.96$ mW	[0.5, 0.5]

Question 3 **[30 marks]**

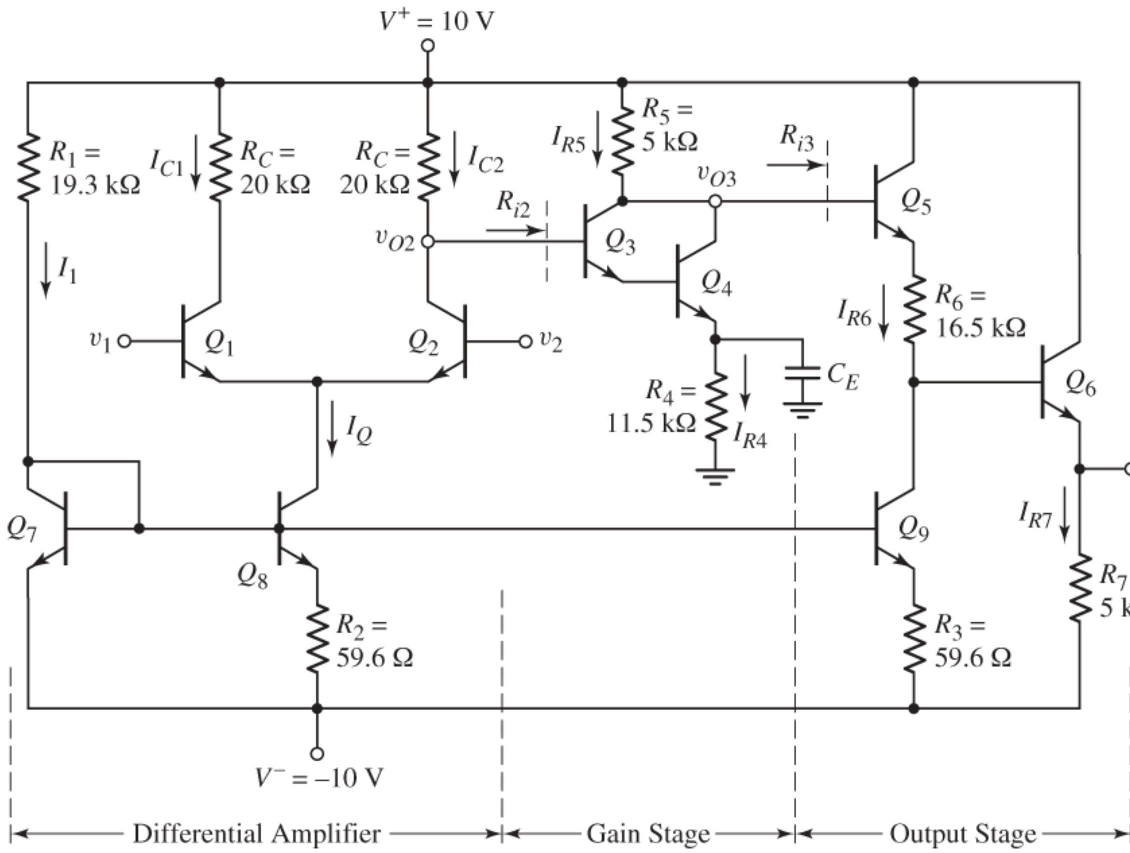


Figure 3

Refer to **Figure 3**. It is given that $I_Q = I_{R4} = I_{R6} = 0.4$ **mA**, and $I_{R7} = 2$ **mA**. **Neglect base currents** and assume V_{BE}**(on) = 0.7 V** for all transistors except Q_8 and Q_9 in the **Widlar** circuit.

a) **List** all **transistors** and **resistors** forming the **biasing stage** of the circuit in the **Figure 3**? [3 marks]

b) **Calculate** the common-mode input range. **State** your assumptions. [7 marks]

c) **Calculate** overall gain of the circuit. Assume $\beta = 100$ and $V_A = \infty$. It is given that the gain of the **Darlington Pair** can be calculated using [18 marks]

$$A_{V2} = \left(\frac{I_{R4}}{2V_T}\right)(R_5 \parallel R_{i3})$$

d) **Comment** on the **loading effect** of the output stage onto the gain stage. [2 marks]

Answers for Question 3

a)

Q_7, R_1, Q_8, R_2, Q_9 and R_3. **[0.5 mark each]**

b)

V_{cm}(max) = V_{C1}, assume V_{CE}(min) = V_{BE}(on) **[1]**
$V_{C1} = V^+ - I_{C1} R_C$ = 10 - (0.2m)(20k) = 6 V **[2]**

V_{cm}(min) = $V^- + V_{BE1} + V_{BE8}$ **[2]**
assume neglect V_{R2} **[0.5]**
V_{cm}(min) = -10 + 0.7 + 0.7 = -8.6 V **[1.5]**

c)

$$A_d = A_{d1}.A_{v2}.A_{v3} = \left(\frac{v_{o2}}{v_1 - v_2}\right).\left(\frac{v_{o3}}{v_{o2}}\right).\left(\frac{v_o}{v_{o3}}\right)$$ **[2]**

$$A_{d1} = \left(\frac{V_{o2}}{v_d}\right) = \frac{g_m}{2}\left(R_C \| R_{i2}\right)$$ **[2]**

$$R_{i2} = r_{\pi 3} + (1+\beta) r_{\pi 4}$$ **[2]**

$$r_{\pi 4} = \beta V_T / I_{R4} = (100)(0.026)/0.4\text{m} = 6.5\text{k}\Omega$$ **[0.5]**

$$r_{\pi 3} \cong \beta^2 V_T / I_{R4} = (100)^2 (0.026)/0.4\text{m} = 650\text{k}\Omega$$ **[1.5]**

$$R_{i2} = 650\text{k} + (101)(6.5\text{k}) = 1307\text{k}\Omega$$ **[0.5]**

$$g_m = I_Q /(2V_T) = 0.4\text{m}/(2 \times 0.026) = 7.70\text{mA/V}$$ **[0.5]**

$$\therefore A_{d1} = (7.70\text{m}/2)(20\text{k} \| 1307\text{k}) = 75.8$$ **[1]**

$$R_{i3} = r_{\pi 5} + (1+\beta)\left[R_6 + r_{\pi 6} + (1+\beta) R_7\right]$$ **[2]**

$$r_{\pi 5} = \beta V_T / I_{R6} = (100)(0.026)/0.4\text{m} = 6.5\text{k}\Omega$$ **[0.5]**

$$r_{\pi 6} = \beta V_T / I_{R7} = (100)(0.026)/2\text{m} = 1.3\text{k}\Omega$$ **[0.5]**

$$R_{i3} = 6.5\text{k} + (1+100)\left[16.5\text{k} + 1.3\text{k} + (1+100)5\text{k}\right] = 52.8\text{M}\Omega$$ **[1]**

$$A_{v2} = \frac{I_{R4}}{2V_T}\left(R_5 \| R_{i3}\right) = \frac{0.4\text{m}}{2(0.026)}\left(5\text{k} \| 52.8\text{M}\right) = 38.5$$ **[1]**

$$A_{v3} \approx 1$$ **[1]**

$$A_d = (75.8)(38.5)(1) = 2918$$ **[2]**

d)

Since $R_{i3} >> R_5$, the output stage does not load down the gain stage **[2]**

Appendix: BASIC FORMULA

BJT

$$i_C = I_S e^{v_{BE}/V_T} \text{ ; npn}$$

$$i_C = I_S e^{v_{EB}/V_T} \text{ ; pnp}$$

$$i_C = \alpha i_E = \beta i_B$$

$$i_E = i_B + i_C$$

$$\alpha = \frac{\beta}{\beta + 1}$$

;Small signal

$$\beta = g_m r_\pi$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

MOSFET

;N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n [v_{GS} - V_{TN}]^2$$

$$K_n = \frac{k_n'}{2} \cdot \frac{W}{L}$$

;P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p [v_{SG} + V_{TP}]^2$$

$$K_p = \frac{k_p'}{2} \cdot \frac{W}{L}$$

;Small signal

$$g_m = 2K_n \left(V_{GSQ} - V_{TN}\right) = 2\sqrt{K_n I_{DQ}}$$

$$r_o \cong \frac{1}{\lambda I_{DQ}}$$