COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 2 2012 / 2013

PROGRAMME	: **Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	: **EEEB273**
SUBJECT	: **ELECTRONIC ANALYSIS AND DESIGN II**
DATE	: **January 2013**
TIME	: **3 hours**

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **Five** (5) questions in **Ten** (10) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided.
4. Write answer to different question on **a new page**.
5. For all calculations, assume that V_T **= 26 mV**.
6. Use at least **4 significant numbers** in all calculations.

THIS QUESTION PAPER CONSISTS OF TEN (10) PRINTED PAGES INCLUDING THIS COVER PAGE.

Question 1 [15 marks]

(a) For a **BJT Cascode current source (using npn transistors)** with $\boldsymbol{R_1}$ **= 9.3 kΩ**, the transistor parameters are $\boldsymbol{V_{BE}}$**(on) = 0.7 V,** $\boldsymbol{\beta}$ **= 120,** and $\boldsymbol{V_A}$ **= 100 V**. The bias voltages are $\boldsymbol{V^+}$ **= 5 V** and $\boldsymbol{V^-}$ **= -5 V**.

(i) **Draw** the circuit for the **BJT Cascode current source specified above**. Label the circuit clearly. [2 marks]

(ii) **Show that the relationship between** $\boldsymbol{I_O}$ **and** $\boldsymbol{I_{REF}}$ can be given by the following equation. [5 marks]

$$I_O \cong \frac{I_{REF}}{1+4/\beta}$$

<u>Hints</u>: You may start by using equation $\boldsymbol{I_{E4} = I_{E3} / (1+2/\beta)}$ derived for a **BJT two-transistor current source**.

(b) **A MOSFET two-transistor (using NMOS) current source** is using **a resistor to establish its** $\boldsymbol{I_{REF}}$. The output current ($\boldsymbol{I_O}$) is **1 mA** and the circuit parameters are $\boldsymbol{V^+}$ **= 15 V** and $\boldsymbol{V^-}$ **= -15 V**. Assume all transistors are identical. The transistor parameters are $\boldsymbol{V_{DS}}$**(sat) = 0.8 V**, $\boldsymbol{V_{TN}}$ **= 1.5 V**, $\boldsymbol{k'_n}$ **= 50 μA/V²** and $\boldsymbol{\lambda = 0}$.

(i) Let the second transistor, $\boldsymbol{M_2}$, be the output transistor. **Draw and label** the circuit and its components **clearly**. **<u>Hints</u>**: You need to determine the value of $\boldsymbol{R_1}$ in order to draw and label the circuit **correctly**. [2 marks]

(ii) **Calculate the aspect ratios** for all transistors. [2 marks]

(iii) **Find** the change on the **output current** due to changes on the output voltage from **2 to 10 Volt**. [2 marks]

(iv) **Discuss how** the reference portion of the circuit can be designed with MOSFETs. [2 marks]

Question 2 [20 marks]

(a) Consider the differential amplifier in **Figure 2a** where **one-sided output** is taken at $\boldsymbol{V_{D2}}$. It is given that $\boldsymbol{R_D = 18\ k\Omega}$, $\boldsymbol{K_n = 125\ \mu A/V^2}$, $\boldsymbol{\lambda = 0}$, $\boldsymbol{A_{cm} = 0.2}$, and ***CMRR*** of the differential amplifier is **55 dB.**

(i) Find $\boldsymbol{I_Q}$. [6 marks]

(ii) Instead of increasing the value of $\boldsymbol{R_D}$, **suggest how** the circuit can be modified to get a bigger ***CMRR***. [3 marks]

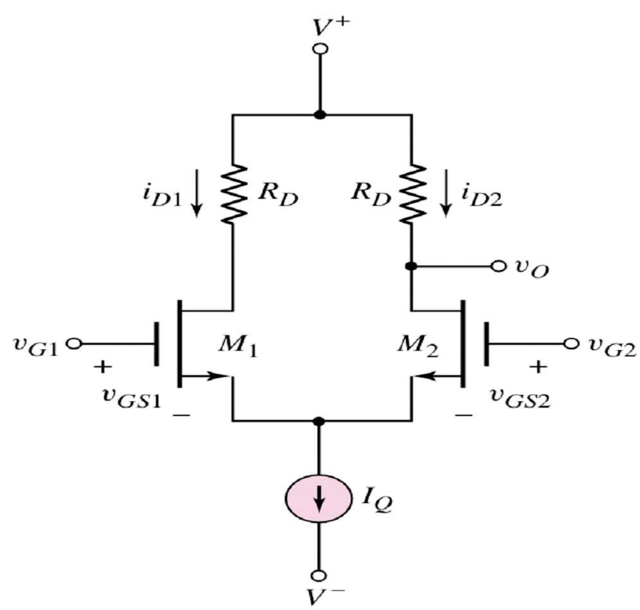

Figure 2a

(b) The differential amplifier shown in **Figure 2b** has a **three-transistor current mirror** connected as an **active load**. The circuit is connected to power supply voltages of V^+ **= +5 V** and V^- **= -5 V**.

(i) **Derive** the relationship between I_O and I_Q such that the amplifier **dc currents are balanced**. State your assumptions. [9 marks]

(ii) **Calculate** the value of I_O given that I_Q **= 0.2 mA** and β**=120**. [2 marks]

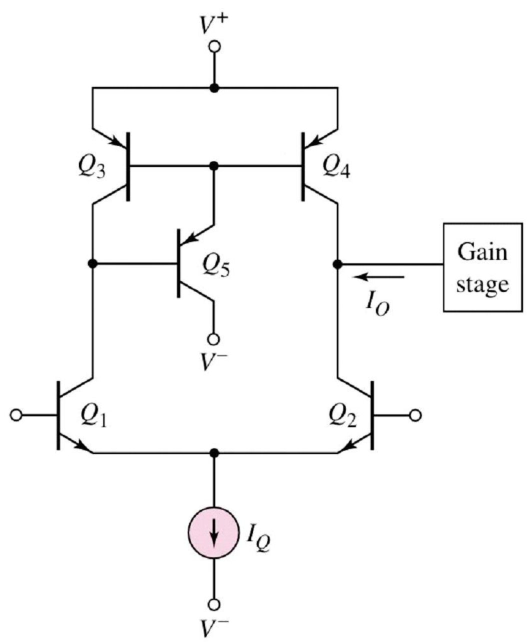

Figure 2b

Question 3 [25 marks]

(a) A simple **bipolar op-amp** is designed as shown in **Figure 3a**. ***Note** that biasing for amplifiers in the circuit is provided by **two-transistor current mirrors***. Study the figure carefully. **Neglect base currents**. Assume parameters for all transistors are: $\boldsymbol{V_{BE}}$**(on) = 0.7 V**, $\boldsymbol{\beta}$ **= 120,** and $\boldsymbol{V_A} = \infty$.

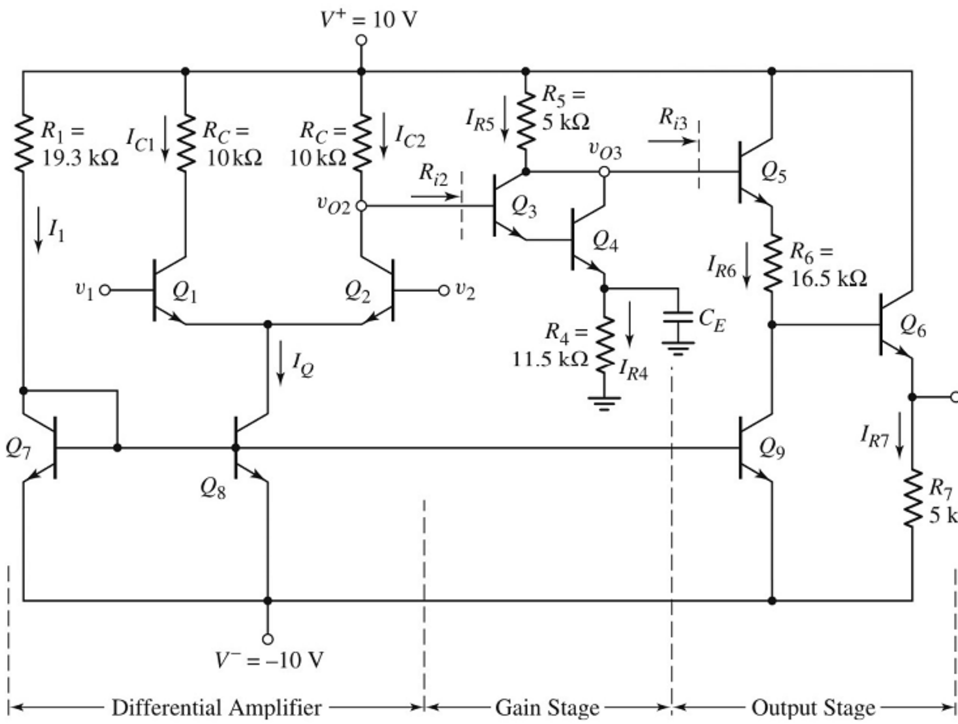

Figure 3a

(i) Referring to **Figure 3a,** find $\boldsymbol{I_1}$, $\boldsymbol{I_Q}$, $\boldsymbol{I_{C2}}$, $\boldsymbol{v_{O2}}$, and $\boldsymbol{v_{O3}}$. [5 marks]

(ii) With small-signal analysis values for $\boldsymbol{A_{d1}}$, $\boldsymbol{r_{\pi 3}}$, $\boldsymbol{R_{i2}}$, and $\boldsymbol{A_2}$ can be found using the following formula:

$$A_{d1} = \left(\frac{V_{o2}}{v_d}\right) = \frac{g_m}{2}\left(R_C \| R_{i2}\right)$$

$$r_{\pi 3} \cong \beta r_{\pi 4}$$

$$R_{i2} = r_{\pi 3} + (1+\beta) r_{\pi 4}$$

$$A_2 \cong \frac{I_{R4}}{2V_T}(R_5)$$

Calculate $\boldsymbol{A_{d1}}$, $\boldsymbol{A_2}$, and the total overall small-signal voltage gain, $\boldsymbol{A_d}$.

[10 marks]

(b) Consider the **MC14573** op-amp in **Figure 3b.** Assume transistors parameters of V_{TN} = **0.5 V**, V_{TP} = **-0.5 V**, K_n = **125 μA/V²**, K_p = **100 μA/V²**, V_{SG5} = **1.5 V**, λ_n = **0.01V⁻¹**, λ_p = **0.02 V⁻¹** and the circuit parameters of V^+ = **10 V**, V^- = **-10 V**.

(i) **Find** the dc bias currents I_Q. [3 marks]

(ii) **Determine** the **overall voltage gain** of the op-amp. [7 marks]

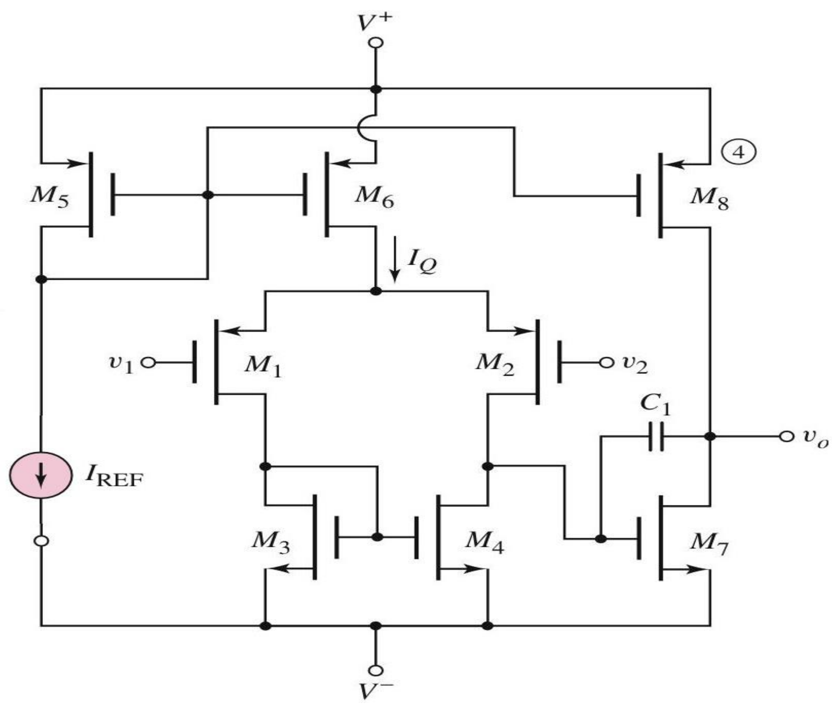

Figure 3b

<u>Question 4 [15 marks]</u>

Study the output stage circuit shown in **Figure 4** carefully. Let R_L **= 1 kΩ,** V_{BB} **= 1.40 V** and the reverse saturation current for the transistors, $I_S = 2 \times 10^{-15}$ **A**. **Assume** $\beta >> 1$.

(a) **Explain** the ñcross-over distortionò phenomenon in **class-B output stage**.

[3 marks]

(b) What is the **advantage** of the output stage shown in **Figure 4** compared to the **class-A** and **class-B** output stages? [2 marks]

(c) Referring to **Figure 4**, for the case of the output voltage $v_O = -3.5$ **V**, **determine** i_L, i_{Cp}, and i_{Cn}.

[6 marks]

(d) Referring to **Figure 4**, for the case of the output voltage $v_O = -3.5$ **V**, **calculate** the power dissipated in transistor Q_n and Q_p. [4 marks]

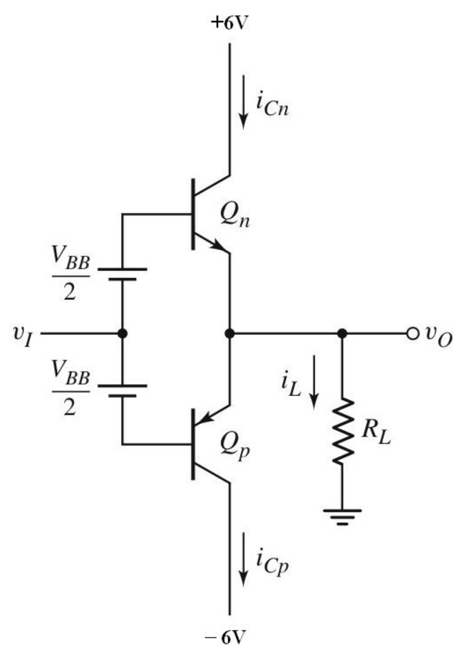

Figure 4

Question 5 [25 marks]

(a) **List** two (**2**) ideal operational amplifier characteristics. [2 marks]

(b) **State** three (**3**) applications of an ideal operational amplifier. [3 marks]

(c) For an **amplifier circuit** using op-amps shown in **Figure 5a**, use appropriate ideal op-amp characteristics and **superposition theorem** to show that

$$v_O = v_{I1} + v_{I2}$$

when $R_1 = R_2 = R_F = 100\ \text{k}\Omega$. [7 marks]

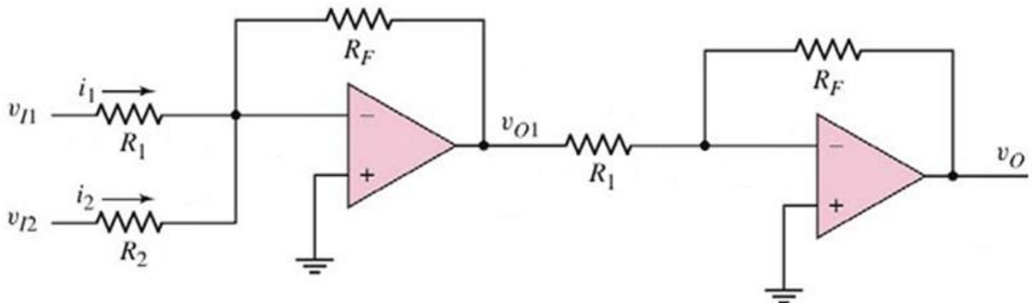

Figure 5a

(d) **Find** the voltage gain, A_v, for the op-amp circuit in **Figure 5b**. Assume the op-amp is ideal. [5 marks]

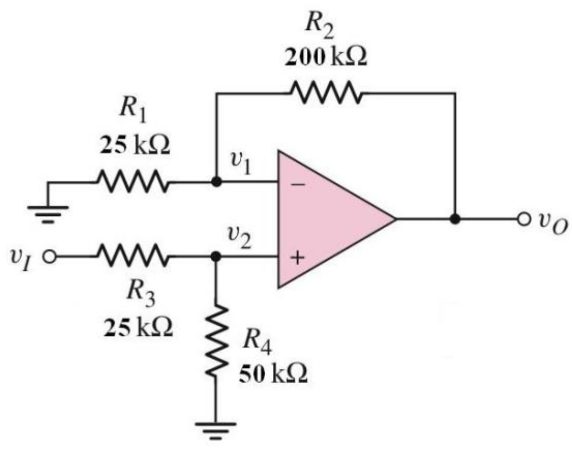

Figure 5b

(e) For a **generalized summing op-amp** as shown in **Figure 5c** the total output voltage (***v_O***) is the sum of the individual terms, or

$$v_O = -\frac{R_F}{R_1}v_{I1} - \frac{R_F}{R_2}v_{I2} + \left(1 + \frac{R_F}{R_N}\right)\left(\frac{R_P}{R_A}v_{I3} + \frac{R_P}{R_B}v_{I4}\right)$$

where $R_N = R_1 \| R_2$

$R_P = R_A \| R_B \| R_C$

Design a summing op-amp similar to **Figure 5c** to produce the output

$$v_O = -5v_{I1} - 10v_{I2} + 5v_{I3} + 2v_{I4}$$

The smallest resistor value allowable in the design is **15 kΩ**.

[8 marks]

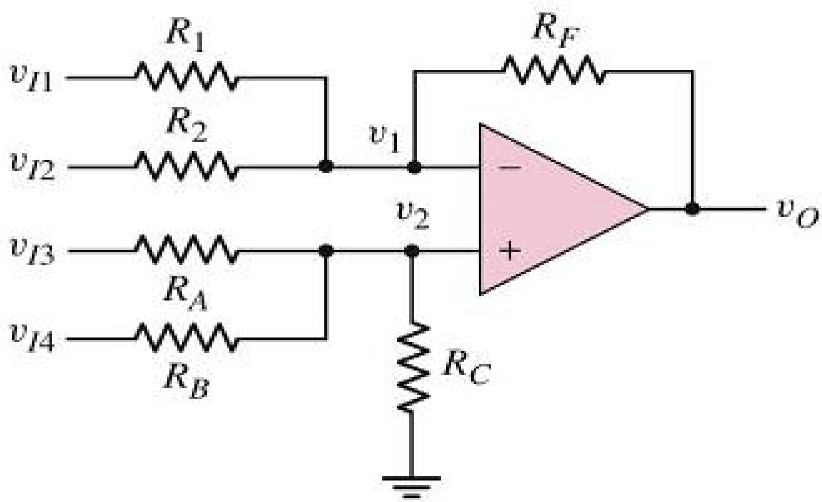

Figure 5c

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APPENDIX

BASIC FORMULA

BJT

$$i_C = I_S e^{v_{BE}/V_T} \text{ ; npn}$$

$$i_C = I_S e^{v_{EB}/V_T} \text{ ; pnp}$$

$$i_C = \alpha i_E = \beta i_B$$

$$i_E = i_B + i_C$$

$$\alpha = \frac{\beta}{\beta + 1}$$

;Small signal

$$\beta = g_m r_\pi$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

MOSFET

;N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n [v_{GS} - V_{TN}]^2$$

$$K_n = \frac{k_n'}{2} \cdot \frac{W}{L}$$

;P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p [v_{SG} + V_{TP}]^2$$

$$K_p = \frac{k_p'}{2} \cdot \frac{W}{L}$$

;Small signal

$$g_m = 2\sqrt{K_? I_{DQ}}$$

$$r_o \cong \frac{1}{\lambda I_{DQ}}$$