COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 1 2013 / 2014

PROGRAMME	**: Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	**: EEEB273**
SUBJECT	**: ELECTRONIC ANALYSIS AND DESIGN II**
DATE	**: September 2013**
TIME	**: 3 hours**

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **Six** (6) questions in **Ten** (10) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided.
4. Write answer to different question on **a new page**.
5. For all calculations, assume that V_T **= 26 mV**.
6. Use at least **4 significant numbers** in all calculations.

THIS QUESTION PAPER CONSISTS OF TEN* (10) *PRINTED PAGES INCLUDING THIS COVER PAGE.

Question 1 [20 marks]

You are required **to design** a differential amplifier with passive load using **NPN** bipolar junction transistors (**BJT**).

The differential amplifier is biased by a **1.5 mA** constant current from a **2-transistor NPN BJT** current source. Power supplies of **+10 V** and **-10 V** are used to power the overall circuit.

Output of the differential amplifier is taken as **one-sided output** at one of its transistor. The differential-mode voltage gain (A_d) is **150 V/V**.

Available components for the design are:

- Matched **NPN BJTs** with $\beta = 50$, $V_{BE}(on) = 0.7$ V, and $V_A = \infty$.
- Various resistors with precise values.

Design the differential amplifier described above, complete with its biasing circuit, and **draw and label clearly** the circuit diagram of your design. **Show clearly all calculations** related to the design, with the values as accurate as possible.

[20 marks]

Question 2 [15 marks]

As knowledge in electronic design and analysis advances, a differential amplifier circuit can be improved **to increase its gain** by **using active loads**. The BJT differential amplifier shown in **Figure 2** is biased by a **0.18 mA** constant current source (i.e. I_Q = **0.18 mA**). The differential amplifier uses a **BJT Cascode current source** made up of **PNP transistors** as the **active load**. The output voltage (v_O) of the differential amplifier is taken at v_{C2}. Information related to the transistor parameters are: β **= 150,** V_{BE}**(on) =** V_{EB}**(on) = 0.7 V,** V_{AN} **= 120 V**, and V_{AP} **= 100 V**.

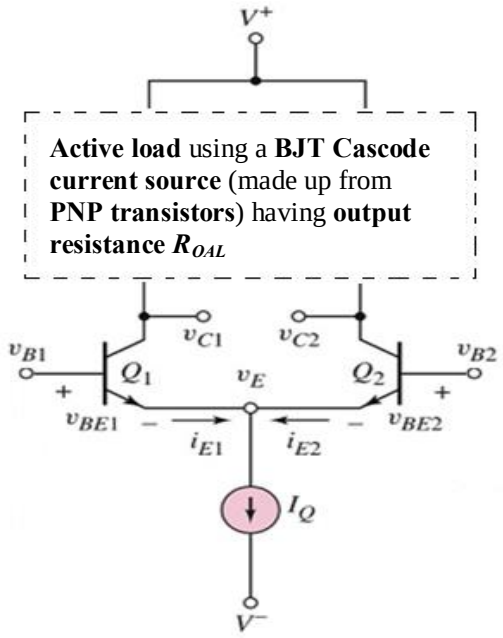

Figure 2

(a) **Calculate** the output resistance of the **BJT Cascode current source** (R_{OAL}) and then **sketch** the differential amplifier circuit incorporating the Cascode current source as the active load. [5 marks]

(b) **Determine** the differential-mode voltage gain of the circuit, $A_d = v_O/v_d$. [6 marks]

(c) **Determine** the output voltage of the circuit if a differential input v_d **= 5 sin (ωt) mV** is applied. **How** will this output different if we use a **two-transistor current source** (made up of **PNP transistors**) as the active load? [4 marks]

Question 3 [10 marks]

(a) **Briefly describe** the advantage of **Class-AB** output stage as compared to the **Class-A** and **Class-B** output stages. [3 marks]

(b) A **Class-A emitter follower** biased with a constant-current source is shown in **Figure 3**. The transistor parameters are: β **= 180,** V_{BE} **= 0.7 V**, and V_{CE}**(sat) = 0.2 V**. Neglect base currents.

(i) **Find** the value of I_Q. [3 marks]

(ii) **Determine** the value of R that will produce the maximum possible output signal swing. [2 marks]

(iii) **Calculate** the conversion efficiency, η. [2 marks]

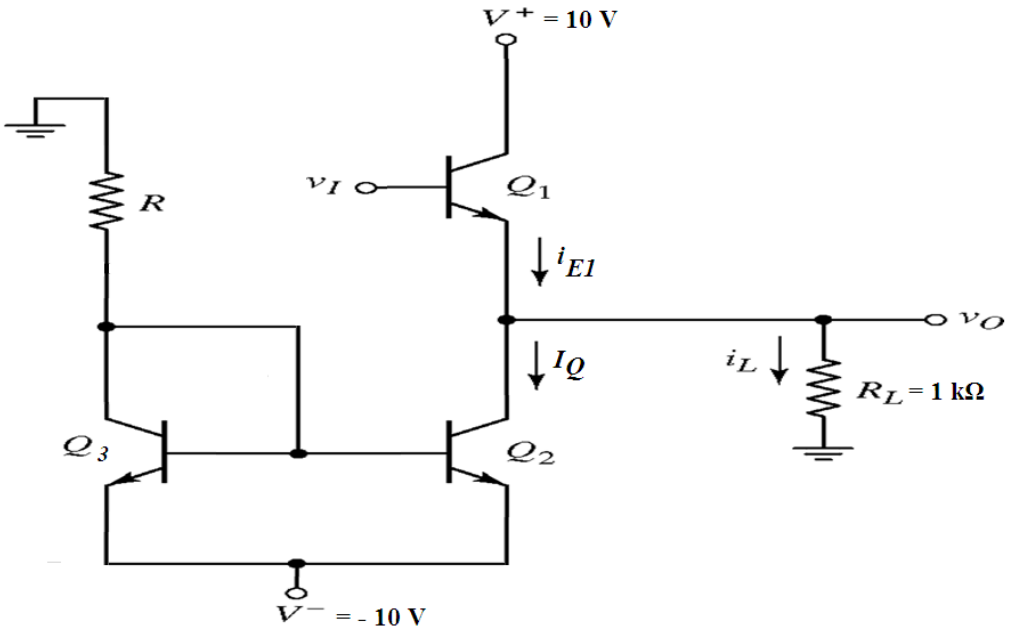

Figure 3

Question 4 [20 marks]

The **MC14573 CMOS op amp,** as shown in **Figure 4**, is used in a sensor circuit requiring a very high-degree of accuracy. The **open-loop gain** of this op amp is required to be **100 dB**. **Design** the circuit to achieve this.

Given: $V^+ = +5$ **V**, $V^- = -5$ **V**, and $I_{set} = 10$ **mA** with $V_{SD5}(\text{sat}) = 1.5$ **V**.
The transistor parameters are: $|V_T| = 2$ **V**, $(1/2)\mu_n C_{ox} = 20$ **μA/V²**, $(1/2)\mu_p C_{ox} = 10$ **μA/V²**, $\lambda_n =$ **0.01 V⁻¹**, and $\lambda_p = 0.02$ **V⁻¹**.
The transistor **aspect ratios** are $(W/L)_{5,6,8} = 10$. Let the aspect ratios of **all other transistors** be the same.

[20 marks]

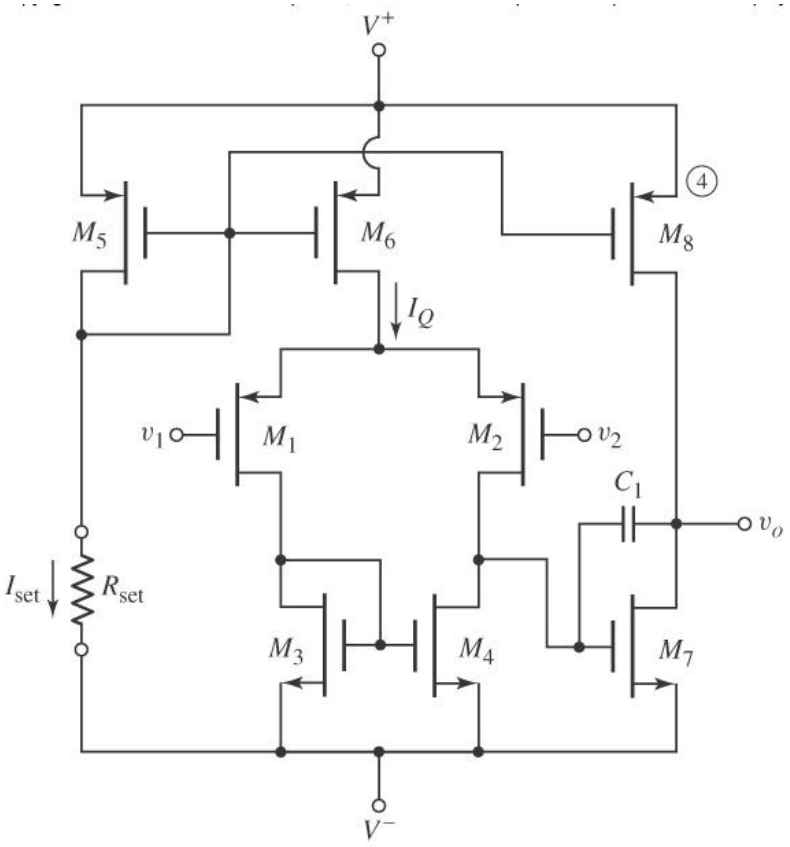

Figure 4

Question 5 [15 marks]

Consider the **standard 741 operational amplifier** circuit as in **Figure 5a**. The operational amplifier is supplied by **±5 V DC** voltage. The transistors have β_n **= 200**, β_p **= 50**, $V_{AN} = V_{AP}$ **= 50 V**, V_{BE}**(on) =** V_{EB}**(on) = 0.65 V (EXCEPT for** V_{BE10}**)**, and the reverse saturation current I_S **=** 5×10^{-16} **A**. Neglect base current in your calculations. Let I_{C16} **= 13.2 µA** and I_{C17} **= 0.165 mA**.

(a) Study the bias circuit **very carefully**. If the current I_{C9} **= 10 µA** and I_{REF} **= 0.22 mA**, **determine** R_4. [5 marks]

(b) **Determine** the operational amplifier **overall differential mode voltage gain** if the resistor values for R_1, R_2 and R_8 are changed to **0 (zero)**, and the small signal voltage gain of the gain stage A_{v2} = **-100**. You may use the ac equivalent circuits as in **Figure 5b** and **Figure 5c** to assist your calculations. [10 marks]

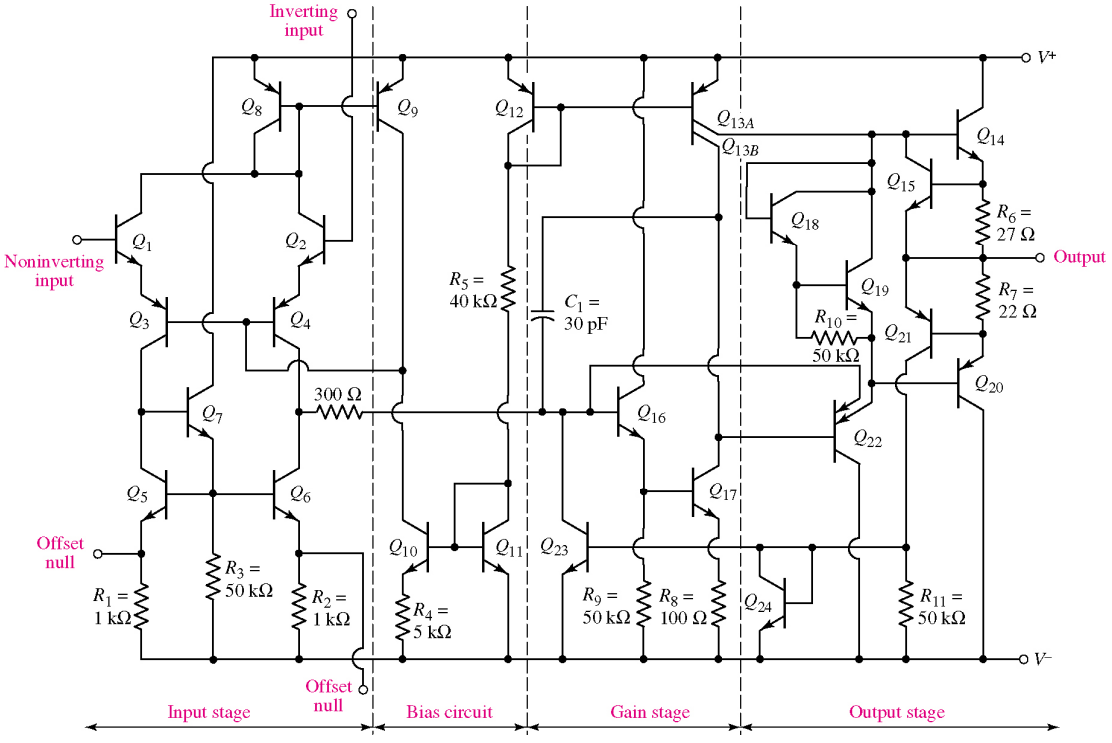

Figure 5a

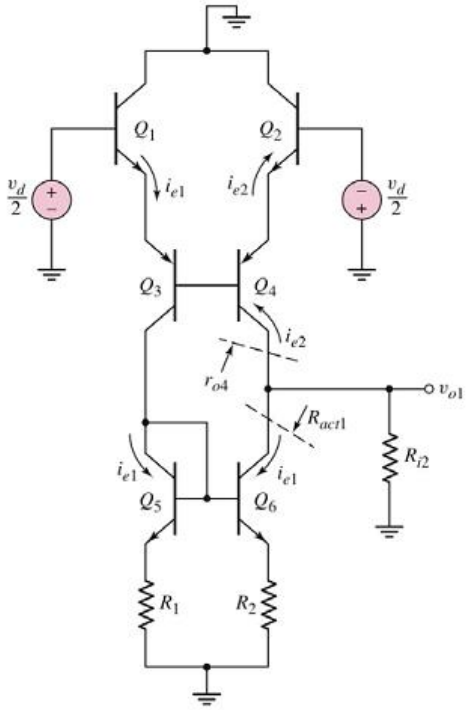

Figure 5b

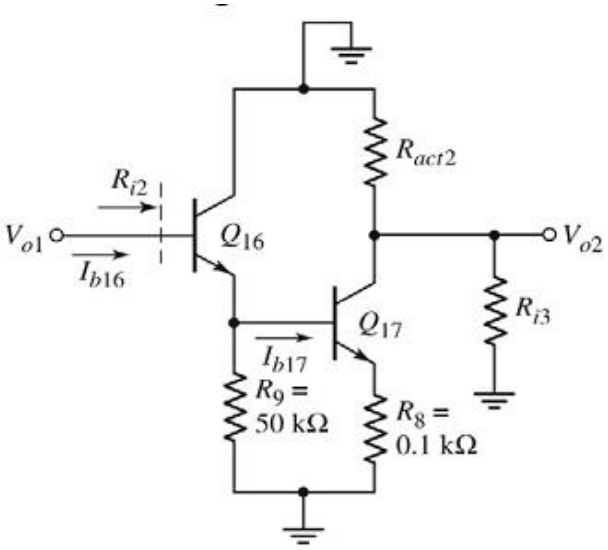

Figure 5c

Question 6 [20 marks]

(a) Using **feedback resistor** of **30 kΩ**, **draw** the following circuits using **inverting op-amp** configuration:

(i) An **inverting amplifier** with a closed-loop gain of **-15**. [4 marks]

(ii) A **voltage follower**. [4 marks]

(b) Consider the **non-inverting op-amplifier** shown in **Figure 6a**. Assume the op-amp is ideal. **Design** the circuit to produce a closed-loop gain of **20**, with the **minimum resistor value** in the circuit is to be **15 kΩ**. [4 marks]

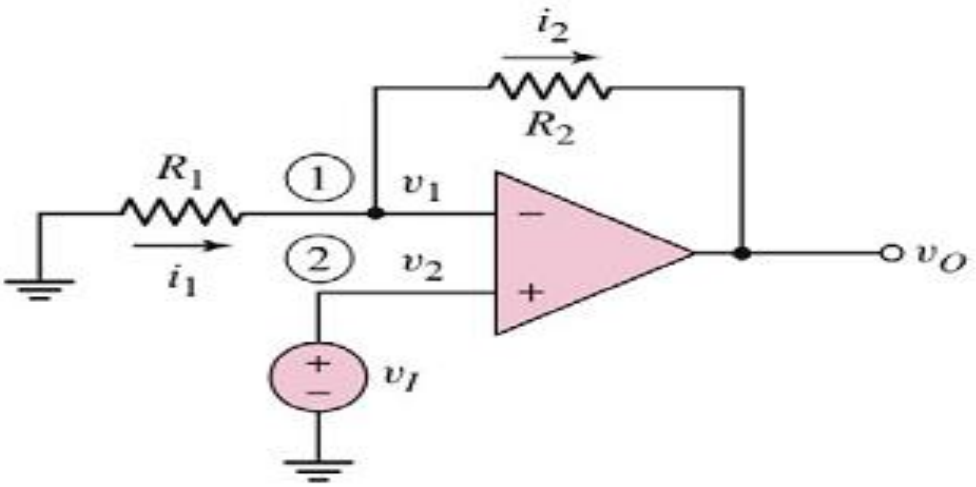

Figure 6a

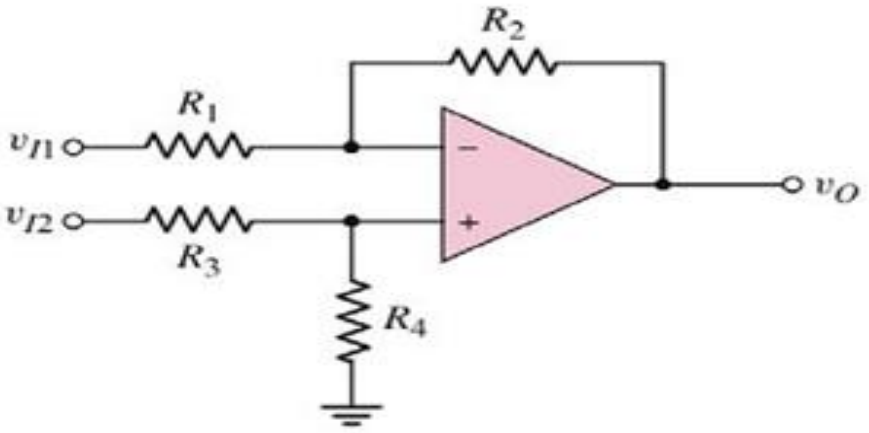

Figure 6b

(c) **A general output equation** for a difference amplifier shown in **Figure 6b** is

$$v_O = A_d v_d + A_{cm} v_{cm}$$

For the difference amplifier in **Figure 6b**, the circuit parameters are R_1 **= 15 kΩ,** R_2 **= 90 kΩ,** R_3 **= 15 kΩ,** and R_4 **= 120 kΩ** and the **output voltage (**v_O**)** equation is as follows:

$$v_O = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4 / R_3}{1 + R_4 / R_3}\right) v_{I2} - \left(\frac{R_2}{R_1}\right) v_{I1}$$

where $$v_{I1} = v_{cm} - \frac{v_d}{2}$$

and $$v_{I2} = v_{cm} + \frac{v_d}{2}$$

Calculate A_d**,** A_{cm}**,** and the ***CMRR*** **in dB** for the circuit. [8 marks]

-END OF QUESTION PAPER-

APPENDIX

BASIC FORMULA

BJT

$i_C = I_S e^{v_{BE}/V_T}$; NPN

$i_C = I_S e^{v_{EB}/V_T}$; PNP

$i_C = \beta i_B = \alpha i_E$

$i_E = i_B + i_C$

$\alpha = \dfrac{\beta}{\beta + 1}$

; Small signal

$\beta = g_m r_\pi$

$r_\pi = \dfrac{\beta V_T}{I_{CQ}}$

$g_m = \dfrac{I_{CQ}}{V_T}$

$r_o = \dfrac{V_A}{I_{CQ}}$

MOSFET

; N – MOSFET

$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$

$i_D = K_n[v_{GS} - V_{TN}]^2$

$K_n = \dfrac{\mu_n C_{ox} W}{2L} = \dfrac{k_n'}{2} \cdot \dfrac{W}{L}$

; P – MOSFET

$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$

$i_D = K_p[v_{SG} + V_{TP}]^2$

$K_p = \dfrac{\mu_p C_{ox} W}{2L} = \dfrac{k_p'}{2} \cdot \dfrac{W}{L}$

; Small signal

$g_m = 2\sqrt{K_? I_{DQ}}$

$r_o \cong \dfrac{1}{\lambda I_{DQ}}$