COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 2 2013 / 2014

PROGRAMME	**: Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	**: EEEB273**
SUBJECT	**: ELECTRONIC ANALYSIS AND DESIGN II**
DATE	**: January 2014**
TIME	**: 3 hours**

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **Six** (6) questions in **Nine** (9) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided. **Use pen** to write your answer.
4. Write answer to different question on **a new page**.
5. For all calculations, assume that V_T **= 26 mV**.

THIS QUESTION PAPER CONSISTS OF NINE (9) PRINTED PAGES INCLUDING THIS COVER PAGE.

Question 1 [20 marks]

You are required to design a differential amplifier with passive load using **NPN bipolar junction transistors (BJT)** with the following specifications. You **DO NOT** need to design the biasing circuit for the differential amplifier.

Two-transistor NPN BJT current source is biasing a **1.2 mA** constant current. The circuit parameters are power supplies of **+10 V** and **−10 V**. The voltages measured at v_{C1} and v_{C2} of the differential amplifier are **4 Volts**.

The transistors parameters are matched NPN BJTs with β **= 50,** V_{BE}**(on) = 0.7 V,** and $V_A = \infty$**,** and various resistors with precise values are made available.

Design the differential amplifier described above with its biasing circuit. **Draw and label** the circuit diagram of your design clearly. **Show all calculations** and values as accurate as possible with regard to the design. Based on your assumption for the design, **calculate** the values for v_d**,** v_{cm}**,** and V_E (i.e. voltage at a point where emitters for both transistors in the differential amplifier are connected).

[20 marks]

Question 2 [15 marks]

Figure 2 shows a basic differential amplifier. A two-transistor current source is used to bias a constant current source of **0.25 mA** (Note: I_Q **= 0.25 mA**). The differential amplifier is using **a pair of PNP transistors as its active load**. The output voltage, v_O, of the differential amplifier is taken as v_{C2}.

The transistors parameters are: β **= 150**, V_{BE}**(on) =** V_{EB}**(on) = 0.7 V**, V_{AN} **= 120 V**, and V_{AP} **= 100 V**.

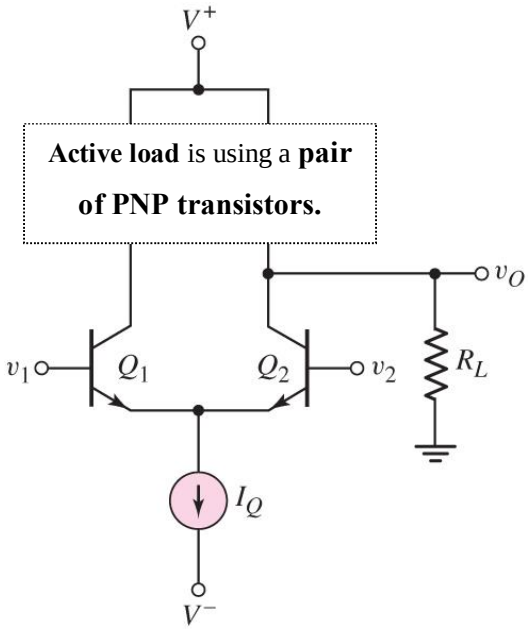

Figure 2

(a) **Draw** a complete differential amplifier circuit including the pair of PNP transistors as active load and the two-transistor current source as biasing circuit.

[5 marks]

(b) **Determine** the differential-mode voltage gain of the circuit, $A_d = v_O/v_d$.

[6 marks]

(c) **Calculate** the differential-mode voltage gain if the load resistance, R_L, is **100 k**Ω.

[4 marks]

Question 3 [10 marks]

(a) **Describe** the operation of **a class-B** output stage by means of crossover distortion. [3 marks]

(b) A **class-AB** output stage with BJTs is shown in **Figure 3**. **Reverse saturation current** for each transistor is $\boldsymbol{I_S = 2\times10^{-15}}$ **A**.

(i) **Find** $\boldsymbol{V_{BB}}$ when $\boldsymbol{v_I = 0}$, as such producing $\boldsymbol{i_{Cn} = i_{Cp} = 1}$ **mA**. [2 marks]

(ii) **Calculate** $\boldsymbol{i_{Cn}}$, $\boldsymbol{i_{Cp}}$, and $\boldsymbol{v_I}$ to obtain $\boldsymbol{v_O = -3.5}$ **V**. [3 marks]

(iii) **Calculate** the power dissipated in $\boldsymbol{R_L}$. [2 marks]

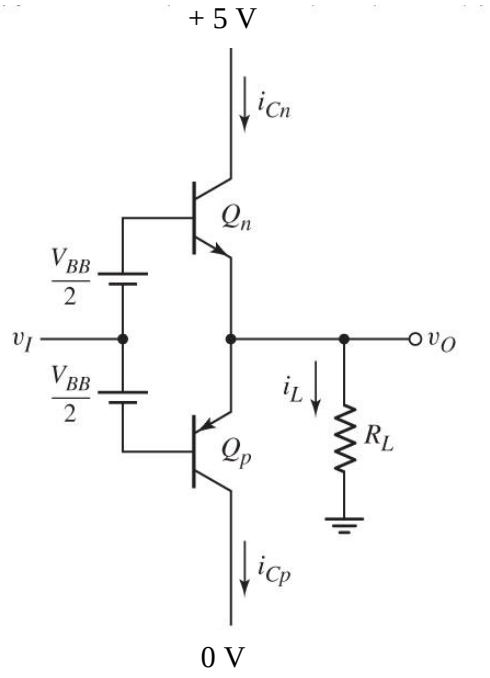

Figure 3

Question 4 [20 marks]

A MOSFET op-amp circuit as shown in **Figure 4** is biased with I_Q = **200 µA**. The transistor parameters are k'_n = **100 µA/V²**, k'_p = **40 µA/V²**, V_{TN} = **0.4 V**, V_{TP} = **-0.4 V**, and $\lambda_n = \lambda_p$ = **0**. The transistor aspect ratios are $(W/L)_1 = (W/L)_2$ = **20**, $(W/L)_3$ = **50**, and $(W/L)_4$ = **40**.

(i) **Design** the circuit such that I_{D3} = **150 µA**, I_{D4} = **200 µA**, and v_o = **0** for $v_1 = v_2$ = **0 V**.

[9 marks]

(ii) **Find** the differential voltage gain (A_d) of the differential amplifier in the circuit.

[4 marks]

(iii) **Determine** the voltage gain for the gain stage (A_2), **made up by transistor M_3**, in the circuit. A_2 can be calculated using $A_2 = -g_{m3} R_{D2}$.

[3 marks]

(iv) **Calculate** the overall small-signal voltage gain (A_v) of the multi-stage amplifier circuit. You may assume value for the voltage gain of the output stage (A_3) **made up by transistor M_4**.

[4 marks]

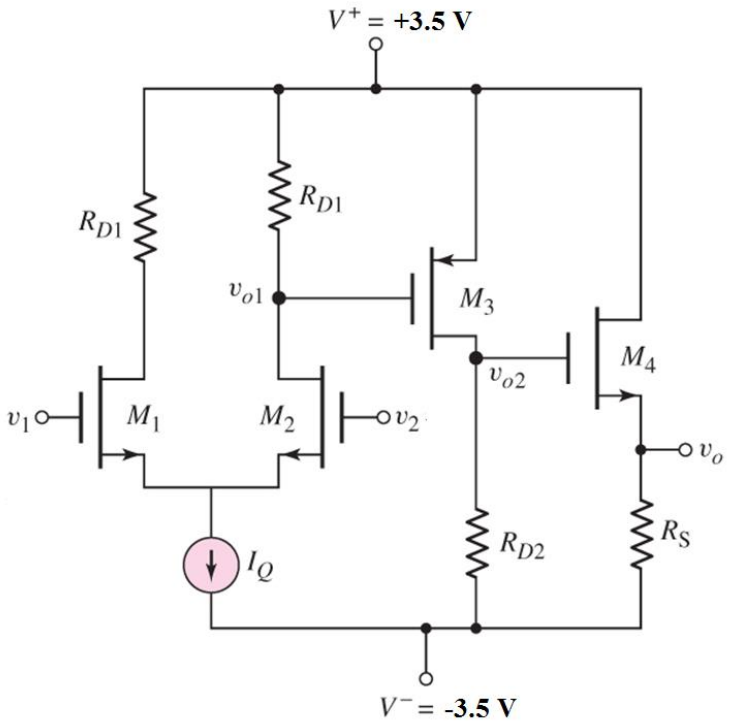

Figure 4

Question 5 [15 marks]

Consider a **standard 741 operational amplifier** (op-amp) circuit as shown in **Figure 5a**. Study **Figure 5a** carefully and observe the values for resistors in the circuit. Load resistance connected to the Output of the 741 op-amp is R_L **= 2 kΩ**. The op-amp is supplied by **±15 V DC** voltages.

The transistors have β_n **= 200**, β_p **= 50**, V_{AN} **=** V_{AP} **= 50 V**, V_{BE}**(on) =** V_{EB}**(on) = 0.6 V**, and the reverse saturation current I_S **=** 5×10^{-16} **A**.

From **DC analysis**, bias currents for selected transistors are I_{C13A} **= 0.18 mA**, I_{C13B} **= 0.54 mA**, I_{C16} **= 15.8 µA,** I_{C17} **= 0.54 mA,** I_{C20} **= 0.138 mA,** and I_{C22} **= 0.18 mA.**

Figure 5b shows the AC equivalent circuit for the gain stage of the 741 op-amp. **Figure 5c** shows the AC equivalent circuit for the output stage of the 741 op-amp, which is used to determine R_{i3} in the **Figure 5b**.

With analysis, the voltage gain for the gain stage (A_{v2}) of the 741 op-amp can be calculated using the following formula:

$$A_{v2} = \frac{v_{o2}}{v_{o1}} = \frac{-\beta_n (1+\beta_n) R_9 \left(R_{act2} \| R_{i3} \| R_{o17} \right)}{R_{i2} \left\{ R_9 + \left[r_{\pi 17} + (1+\beta_n) R_8 \right] \right\}}$$

Where: $R_{act2} = r_{o13B}$

$$R_{i3} = r_{\pi 22} + (1+\beta_p) \left[R_{19} \| R_{20} \right]$$

$$R_{19} \cong R_{13A} = r_{o13A}$$

$$R_{20} = r_{\pi 20} + (1+\beta_p) R_L$$

Calculate the voltage gain for the gain stage (A_{v2}) of the 741 op-amp. Neglect base current in your calculations.

[15 marks]

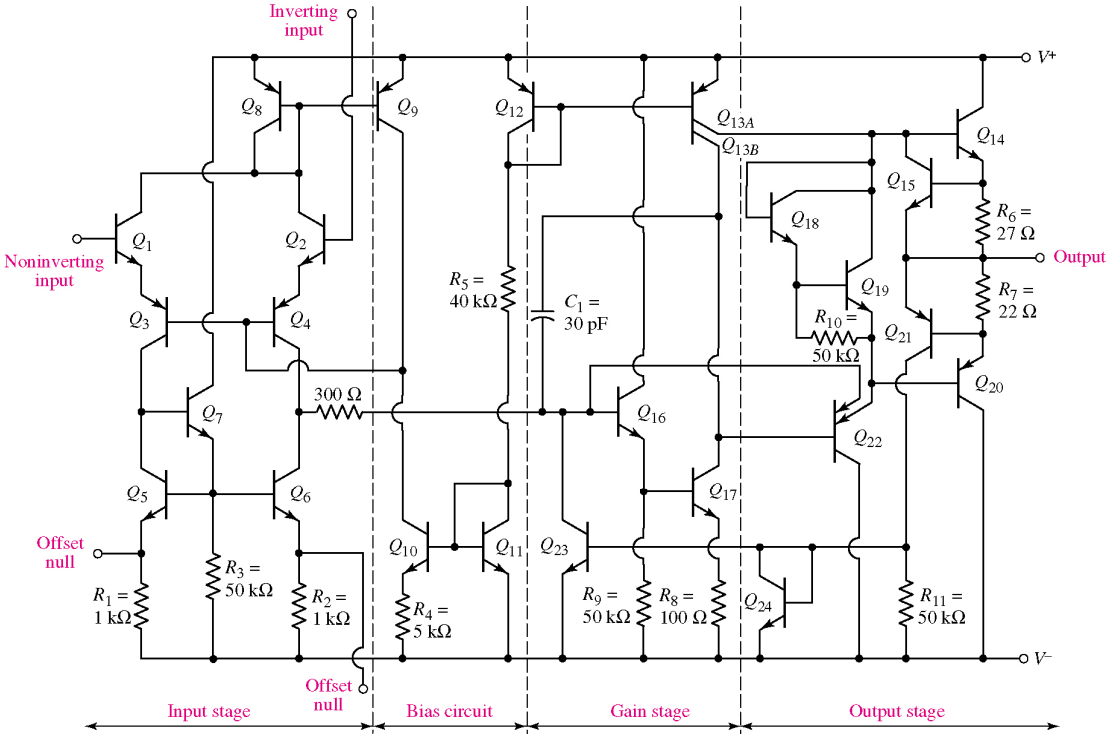

Figure 5a

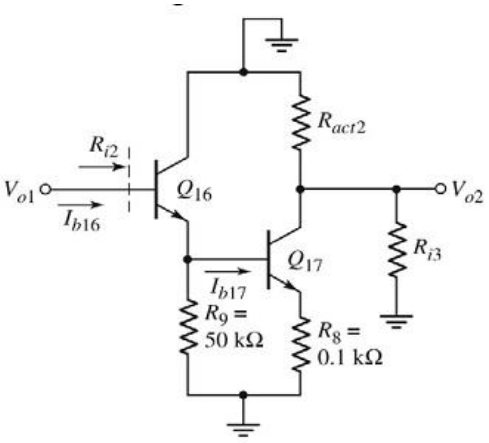

Figure 5b

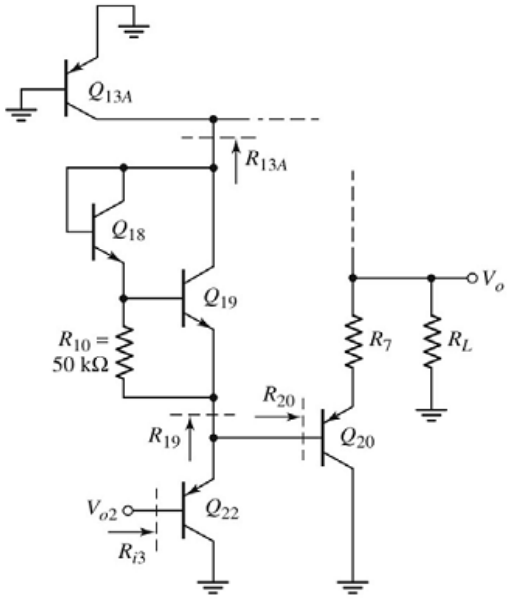

Figure 5c

Question 6 [20 marks]

(a) **EXCEPT** for standard inverting and non-inverting amplifier circuits using op-amp, **state** three (3) other applications using the op-amp and **sketch** those three (3) other op-amp based circuits. You are required to sketch the circuit to include all external components connected to the op-amp, in order for the overall circuit to function its intended application.

[6 marks]

(b) With a feedback resistor of **200 kΩ**, **design** an amplifier using **op-amp** with a **closed-loop gain** which can be **varied between -10 to -25** using a **potentiometer**. **Draw clearly** your circuit design. [6 marks]

(c) For the instrumentation amplifier shown in **Figure 6**, the circuit parameters are $R_1 = 20$ kΩ, $R_2 = 115$ kΩ, $R_3 = 50$ kΩ, and $R_4 = 200$ kΩ. For input signals of $v_{I1} = 0.60 - 0.30 \sin \omega t$ (V) and $v_{I2} = 0.60 + 0.30 \sin \omega t$ (V), **determine** v_{O1}, v_{O2}, and v_O.

[8 marks]

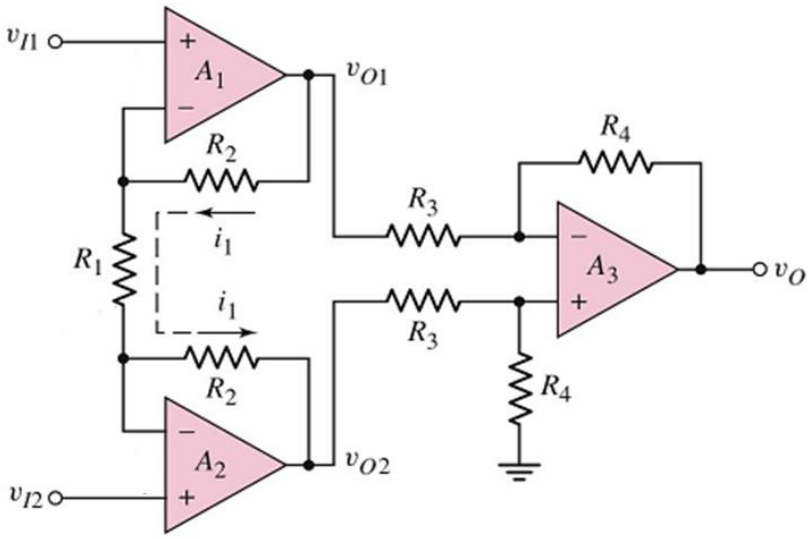

Figure 6

-END OF QUESTION PAPER-

APPENDIX

BASIC FORMULA

BJT

$i_C = I_S e^{v_{BE}/V_T}$; NPN

$i_C = I_S e^{v_{EB}/V_T}$; PNP

$i_C = \beta i_B = \alpha i_E$

$i_E = i_B + i_C$

$\alpha = \dfrac{\beta}{\beta + 1}$

; Small signal

$\beta = g_m r_\pi$

$r_\pi = \dfrac{\beta V_T}{I_{CQ}}$

$g_m = \dfrac{I_{CQ}}{V_T}$

$r_o = \dfrac{V_A}{I_{CQ}}$

MOSFET

; N – MOSFET

$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$

$i_D = K_n[v_{GS} - V_{TN}]^2$

$K_n = \dfrac{\mu_n C_{ox} W}{2L} = \dfrac{k_n'}{2} \cdot \dfrac{W}{L}$

; P – MOSFET

$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$

$i_D = K_p[v_{SG} + V_{TP}]^2$

$K_p = \dfrac{\mu_p C_{ox} W}{2L} = \dfrac{k_p'}{2} \cdot \dfrac{W}{L}$

; Small signal

$g_m = 2\sqrt{K_? I_{DQ}}$

$r_o \cong \dfrac{1}{\lambda I_{DQ}}$