COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SPECIAL SEMESTER 2013 / 2014

PROGRAMME	**: Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	**: EEEB273**
SUBJECT	**: ELECTRONIC ANALYSIS AND DESIGN II**
DATE	**: April 2014**
TIME	**: 3 hours**

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **Six** (6) questions in **Nine** (9) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided.
4. Write answer to different question on **a new page**.
5. For all calculations, assume that V_T **= 26 mV**.

THIS QUESTION PAPER CONSISTS OF NINE* (9) *PRINTED PAGES INCLUDING THIS COVER PAGE.

Question 1 [20 marks]

Design a differential amplifier using **NPN** bipolar junction transistors **(**BJT) biased by a three-transistor current source, also using NPN BJT.

The three-transistor NPN BJT current source (consists of Q_1, Q_2, Q_3, and R_1) is biasing the differential amplifier (consists of Q_4, Q_5, and resistors R_C) with a **1 mA** constant current.

The transistor parameters are: β **= 100,** V_{BE}**(on) = 0.7 V** and $V_A = \infty$. The circuit parameters are: V^+ **= 5 V**, V^- **= -5 V**. For the differential amplifier $V_{B4} = V_{B5} =$ **0,** and R_C is given as **2 kΩ.**

(i) **Draw and label** the circuit diagram of your design clearly. [5 marks]

(ii) **Show clearly** all calculations and values as accurate as possible with regard to the design. You are required, in particular, to calculate the values of the resistor in the current source, V_{CE2}, and V_{CE4}. [15 marks]

Question 2 [10 marks]

The circuit in **Figure 1** shows a pair of PNP bipolar junction transistors as input devices and a pair of NPN bipolar junction transistors connected as an active load. The biasing current $\boldsymbol{I_Q}$ = **0.2 mA,** and the transistor parameters are $\boldsymbol{\beta}$ **= 100**, and $\boldsymbol{V_A}$ **= 100 V**.

(i) **Determine** $\boldsymbol{I_O}$ such that the dc currents in the differential amplifier are **balanced**. [3 marks]

(ii) **Calculate** the open-circuit differential-mode voltage gain, $\boldsymbol{A_d}$. [4 marks]

(iii) **Find** the differential-mode voltage gain if a load resistance $\boldsymbol{R_L}$ **= 250 kΩ** is connected to the output. [3 marks]

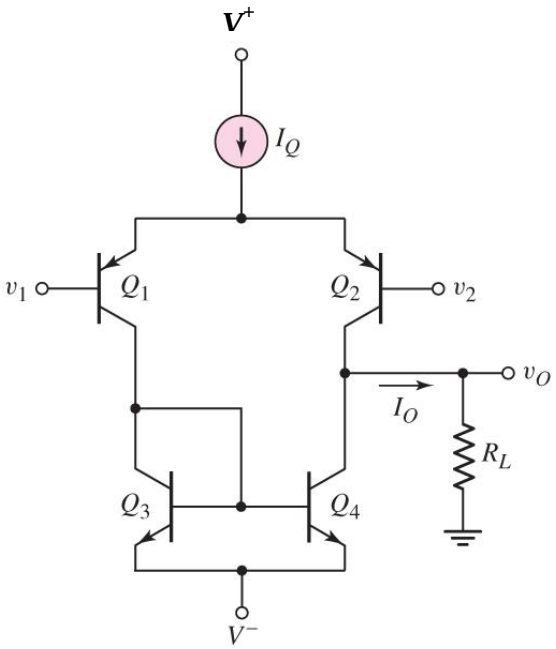

Figure 1

Question 3 [15 marks]

(a) An **idealized class-B** output stage, with a complementary pair transistors, as in **Figure 2** has $V^+ = V_{CC} = 10$ V, $V^- = -10$ V, and $R_L = 200\ \Omega$. Output signal voltage reads $v_O = 6 \sin \omega t$ V. The average power supplied by V^+ and V^- to a **class-B** output stage is $2V_{CC}[V_p/(\pi R_L)]$.

Determine the following:

(i) The average current in the circuit. [2 marks]

(ii) The average power delivered to the load. [3 marks]

(iii) The average power dissipated in each transistor. [4 marks]

(iv) The power conversion efficiency (η) of the output stage. [3 marks]

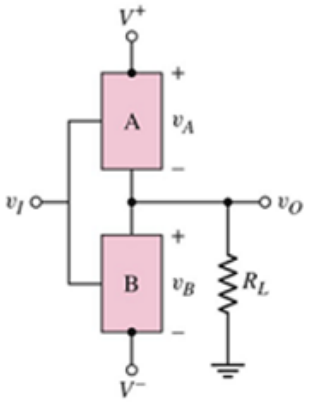

Figure 2

(b) **Describe** the operation of a **class-B** output stage as in **Figure 3**. The cut-in voltage for both transistors is **0.7 V**. How is this output stage different from the **idealized class-B** output stage? [3 marks]

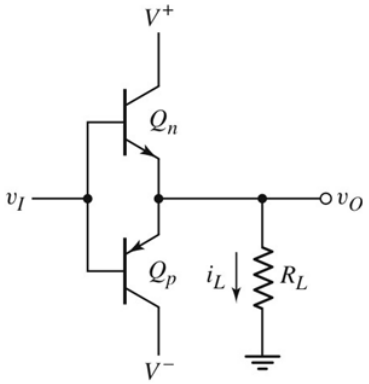

Figure 3

Question 4 [20 marks]

Consider the Darlington pair and emitter follower portion of the circuit in **Figure 4**. The parameters are $\boldsymbol{I_{C7} = I_Q = 0.5\ mA}$, $\boldsymbol{I_{C8} = 2\ mA}$, $\boldsymbol{R_4 = 5\ k\Omega}$, and $\boldsymbol{R_3 = 0.1\ k\Omega}$. For all transistors, the current gain is **90**. $\boldsymbol{Q_{11}}$ has **Early** voltage of **120 V**, while Early voltage for $\boldsymbol{Q_7}$ is ∞.

When necessary, redraw circuit or label the circuit parameters and state your assumptions when **finding the values** of the following;

(i) The input resistance ($\boldsymbol{R_i}$) of the Darlington pair. [8 marks]

(ii) The small signal voltage gain of the Darlington pair. [12 marks]

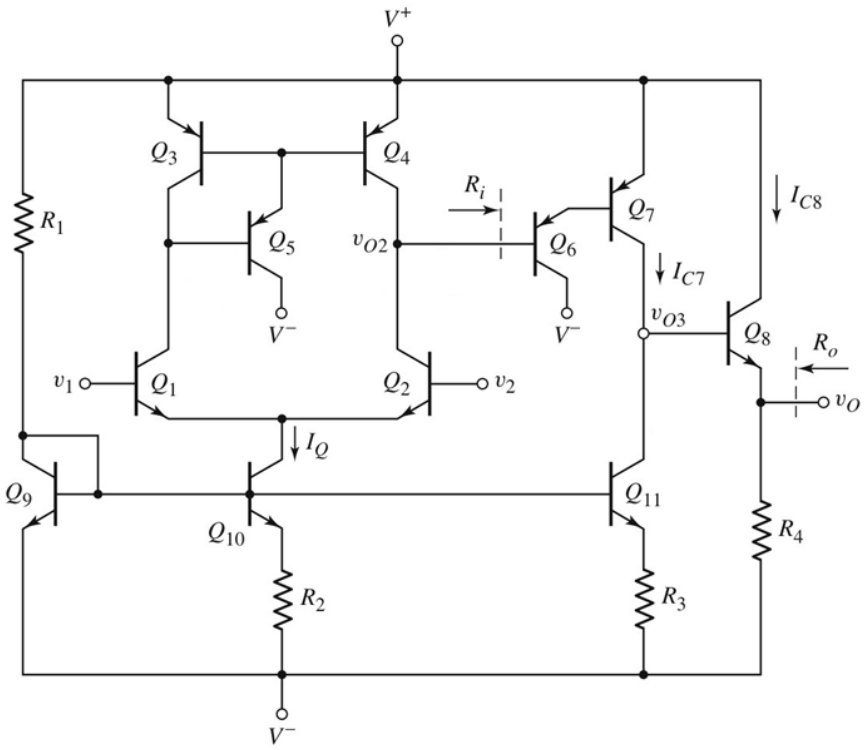

Figure 4

Question 5 [15 marks]

Study the bias circuit and input stage of **741 operational amplifier (op-amp)** shown in **Figure 5** carefully. Given that V^+ = **+12 V** and V^- = **-12 V**. Assume V_{BE} for npn = V_{EB} for pnp = **0.6 V** (EXCEPT for V_{BE10}). Neglect dc **base currents**.

(i) **Determine** the value of resistor R_5 if bias current for Q_1 is **8 µA**, and V^+ = **+12 V** and V^- = **-12 V**. [10 marks]

(ii) Assuming dc currents in the input stage are exactly **balanced**, therefore dc voltage at collector of Q_6 = dc voltage at collector of Q_5. **Calculate** V_{C6}. [5 marks]

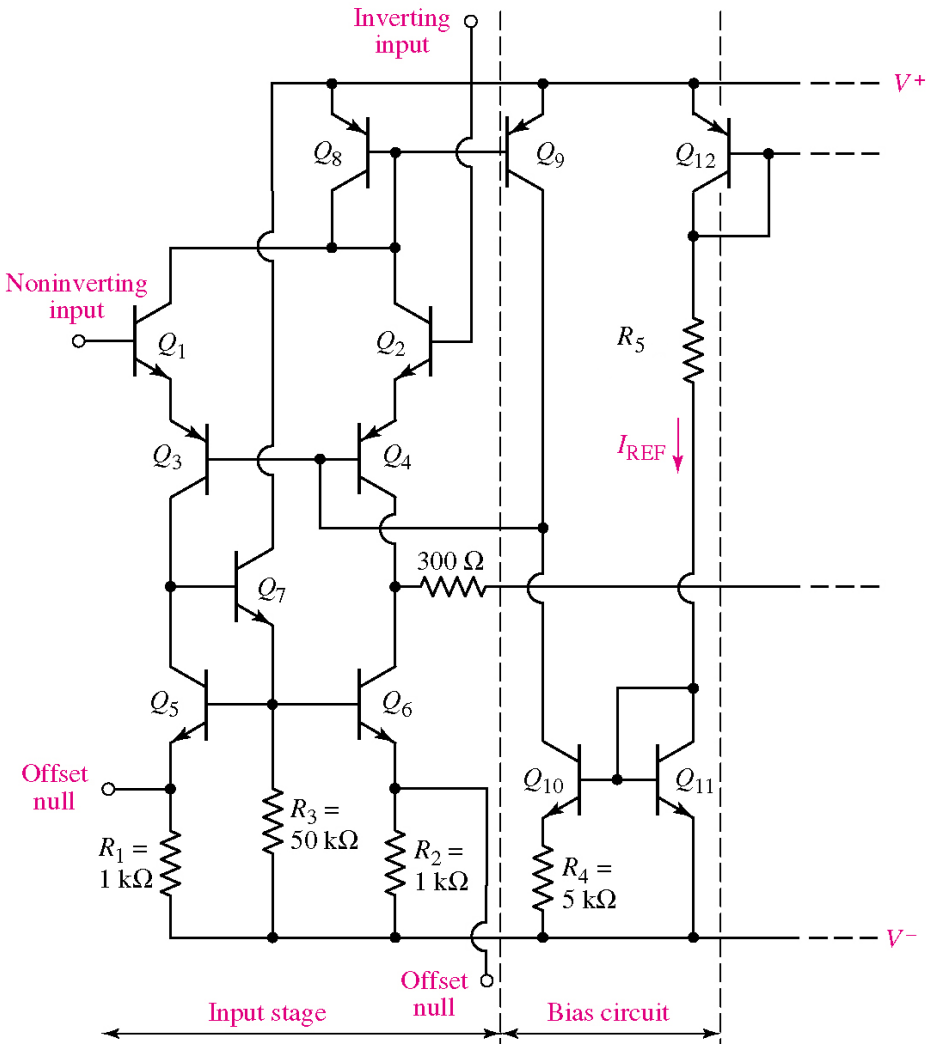

Figure 5

Question 6 [20 marks]

(a) With a feedback resistor ($\boldsymbol{R_2}$) of **250 kΩ**, **design** an amplifier using op-amp in non-inverting configuration with a **closed-loop gain** which can be **varied between 11 to 26 V/V.** The closed-loop gain can be varied using a potentiometer ($\boldsymbol{R_{1V}}$) and a fixed-value resistor ($\boldsymbol{R_{1F}}$). **Draw clearly** your circuit design.

[6 marks]

(b) For an **amplifier circuit** using op-amps shown in **Figure 6**, use appropriate ideal op-amp characteristics to **show** that

$$\boldsymbol{v_O = v_{I1} + v_{I2}}$$

when $\boldsymbol{R_1 = R_2 = R_F = 100\ k\Omega}$. [6 marks]

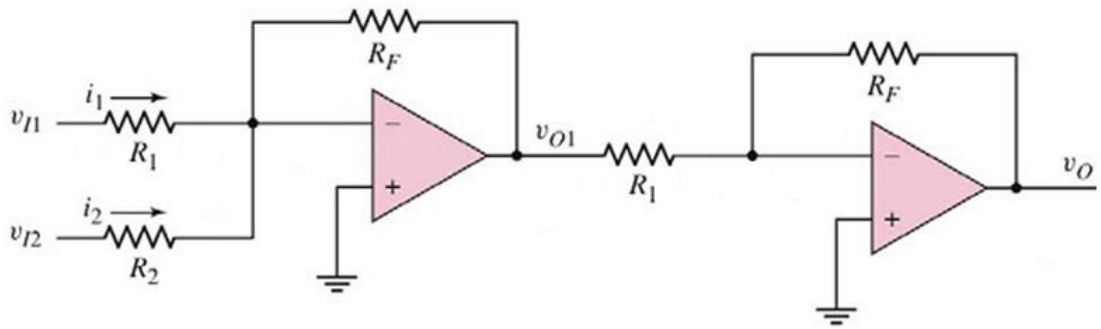

Figure 6

(c) For a **generalized summing op-amp** as shown in **Figure 7** the total output voltage (**v_O**) is the sum of the individual terms, or

$$v_O = -\frac{R_F}{R_1}v_{I1} - \frac{R_F}{R_2}v_{I2} + \left(1+\frac{R_F}{R_N}\right)\left(\frac{R_P}{R_A}v_{I3} + \frac{R_P}{R_B}v_{I4}\right)$$

where $R_N = R_1 \| R_2$

$R_P = R_A \| R_B \| R_C$

With the **smallest resistor value** allowable in the circuit is **25 kΩ, design** a summing op-amp similar to **Figure 6b** to produce the output of

$$v_O = -5v_{I1} - 10v_{I2} + 5v_{I3} + 2v_{I4}$$

[8 marks]

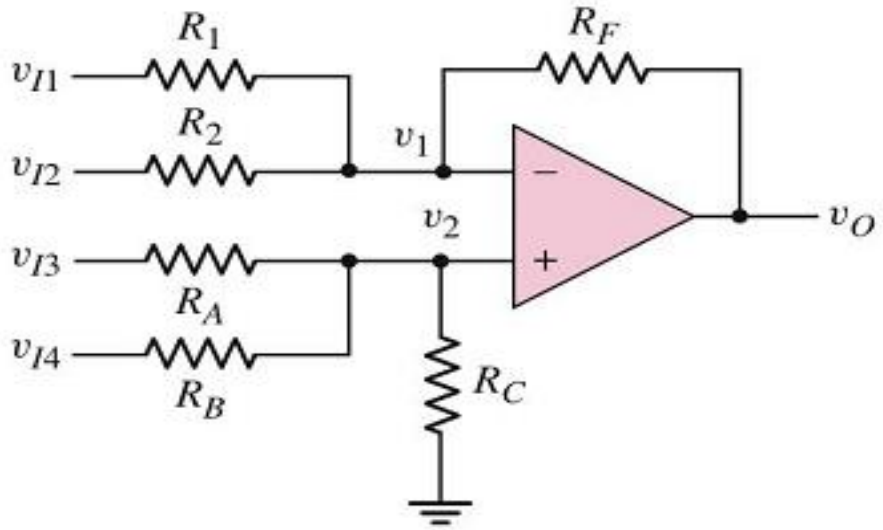

Figure 7

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APPENDIX

BASIC FORMULA

BJT

$$i_C = I_S e^{v_{BE}/V_T} ; \text{NPN}$$

$$i_C = I_S e^{v_{EB}/V_T} ; \text{PNP}$$

$$i_C = \beta i_B = \alpha i_E$$

$$i_E = i_B + i_C$$

$$\alpha = \frac{\beta}{\beta + 1}$$

;Small signal

$$\beta = g_m r_\pi$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

MOSFET

$$;\text{N} - \text{MOSFET}$$

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n [v_{GS} - V_{TN}]^2$$

$$K_n = \frac{\mu_n C_{ox} W}{2L} = \frac{k_n^{'}}{2} \cdot \frac{W}{L}$$

$$;\text{P} - \text{MOSFET}$$

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p [v_{SG} + V_{TP}]^2$$

$$K_p = \frac{\mu_p C_{ox} W}{2L} = \frac{k_p^{'}}{2} \cdot \frac{W}{L}$$

;Small signal

$$g_m = 2\sqrt{K_? I_{DQ}}$$

$$r_o \cong \frac{1}{\lambda I_{DQ}}$$