Name:
Student ID Number:
Section: **01 A/B**

UNIVERSITI TENAGA NASIONAL

College of Engineering

Department of Electronics and Communication Engineering

Test 1

SEMESTER 3, ACADEMIC YEAR 2013/2014

Subject Code	:	**EEEB273**
Course Title	:	**Electronics Analysis & Design II**
Date	:	**13 March 2014**
Time Allowed	:	**2 hours**

Instructions to the candidates:

1. Write your Name and Student ID number. Circle your section number.
2. **Write all your answers using pen**. **DO NOT USE PENCIL** except for the diagram.
3. **ANSWER ALL QUESTIONS.**
4. **WRITE YOUR ANSWER ON THIS QUESTION PAPER.**
5. For BJT, use V_T = **26 mV** where appropriate.
6. Use at least **4 significant numbers** in all calculations.

NOTE: DO NOT OPEN THE QUESTION PAPER UNTIL INSTRUCTED TO DO SO.

☺ **GOOD LUCK!** ☺

Question No.	1	2	3	3	Total
Marks					

Question 1 **[35 marks]**

Figure 1 shows a two-transistor MOS current mirror. The transistor parameters are assumed to be V_{TP} **= -0.4** V, k'_p **= 60** μ**A/V**^{2}, and λ = **0**. The transistor width-to-length ratios are $(W/L)_1$ **= 25**, $(W/L)_2$ **= 15**, and $(W/L)_3$ **= 5**.

(a) Calculate I_O, I_{REF}, V_{SG1}, and V_{SG3}. [20 marks]

(b) Design the circuit such that I_O **= 80** μ**A**, I_{REF} **= 220** μ**A**, and $V_{SD2}(sat)$ **= 0.35** V. [15 marks]

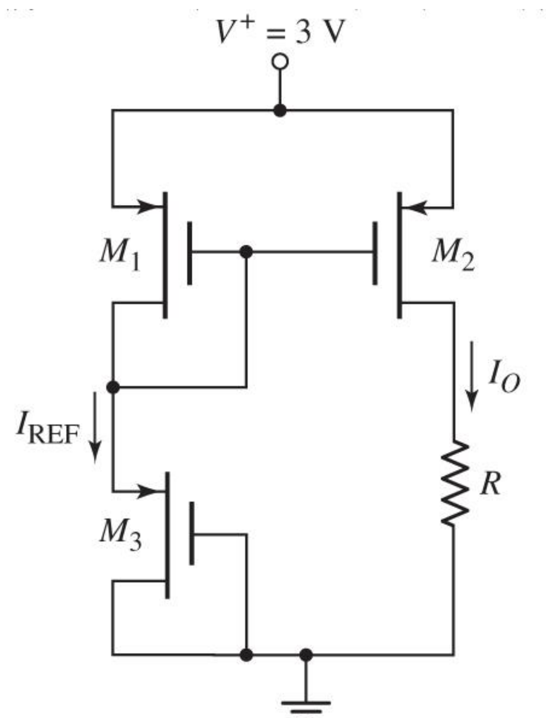

Figure 1

Answers for Question 1

Answers to Q1

(a) Calculate I_O, I_{REF}, V_{SG1}, and V_{SG3}. [20 marks]

$I_{REF} = \left(\frac{k'_p}{2}\right)\left(\frac{W}{L}\right)_1 (V_{SG1} + V_{TP})^2 = \left(\frac{k'_p}{2}\right)\left(\frac{W}{L}\right)_3 (V_{SG3} + V_{TP})^2$é (1) [5]

$V_{SG3} = 3 - V_{SG1}$ é (2) [2]

$\sqrt{25}(V_{SG1} - 0.4) = \sqrt{5}(3 - V_{SG1} - 0.4)$ [5]

$3.26V_{SG1} = 3.4944 \rightarrow V_{SG1} = 1.08\ V \text{ and } V_{SG3} = 1.92\ V$ [4]

Substituting the values,

$I_{REF} = \left(\frac{60}{2}\right)(25)(1.08 - 0.4)^2 = 0.347\ mA$ [2]

$I_O = \left(\frac{60}{2}\right)(15)(1.08 - 0.4)^2 = 0.208\ mA$ [2]

(b) Design the circuit such that I_O = **80** μ**A**, I_{REF} = **220** μ**A**, and $V_{SD2}(sat)$ = **0.35** V. [15 marks]

$V_{SD2}(sat) = 0.35 = V_{SG2} + V_{TP} - 0.4 \rightarrow V_{SG2} = 0.75\ V$ [3]

$I_{REF} = 220\mu = \left(\frac{60}{2}\right)\left(\frac{W}{L}\right)_1 (0.75 - 0.4)^2 \rightarrow \left(\frac{W}{L}\right)_1 = 59.9$ [3]

$I_O = 80\mu = \left(\frac{60}{2}\right)\left(\frac{W}{L}\right)_2 (0.75 - 0.4)^2 \rightarrow \left(\frac{W}{L}\right)_2 = 21.8$ [3]

$V_{SG3} = 3 - 0.75 = 2.25\ V$ [3]

$220 = \left(\frac{60}{2}\right)\left(\frac{W}{L}\right)_3 (2.25 - 0.4)^2 \rightarrow \left(\frac{W}{L}\right)_{32} = 2.14$ [3]

Question 2 **[25 marks]**

Figure 2 shows a differential amplifier has a pair of pnp bipolar as input devices and a pair of npn bipolar connected as an active load. The circuit has $\boldsymbol{I_Q}$ **= 0.2 mA** bias current and the transistor parameters are β **= 100** and $\boldsymbol{V_A}$ **= 100 V**.

(a) Calculate $\boldsymbol{I_O}$ such that the dc currents in the diff-amp are balanced. [6 marks]

(b) Determine the open-circuit differential-mode voltage gain, $\boldsymbol{A_d}$. [12 marks]

(c) Find the differential-mode voltage gain if a load resistance $\boldsymbol{R_L}$ **= 250 kΩ** is connected to the output. [7 marks]

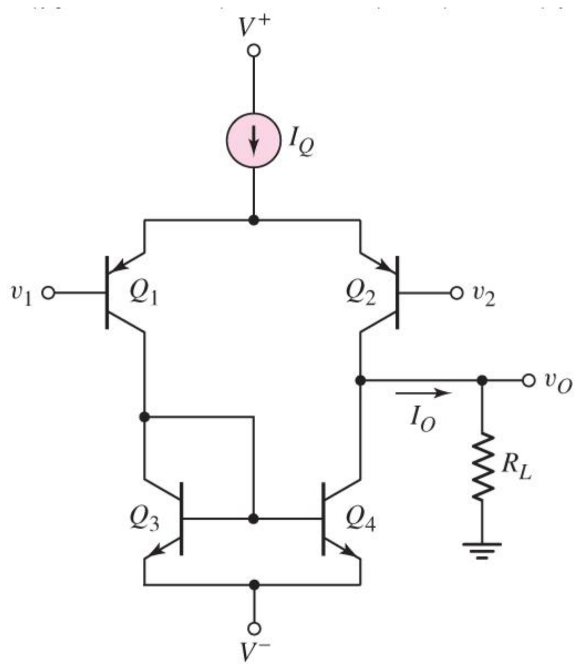

Figure 2

Answers for Question 2

(a) Calculate I_O such that the dc currents in the diff-amp are balanced. [6 marks]

$I_O = I_{B3} + I_{B4}$ [3]

$I_O \approx \frac{I_Q}{\beta} = \frac{0.2m}{100} = 2\ \mu A$ [3]

(b) Determine the open-circuit differential-mode voltage gain, A_d. [12 marks]

$r_{O2} = r_{O4} = \frac{V_A}{I_{CQ}} = \frac{100}{0.1m} = 1000k\Omega$ [4]

$g_m = \frac{I_{CQ}}{V_T} = \frac{0.1m}{0.026} = 3.846\ mA/V$ [4]

$\therefore A_d = g_m(r_{O2}||r_{O4}) = (3.846m)(1000k||1000k) = 1923$ [4]

(c) Find the differential-mode voltage gain if a load resistance $R_L = 250\ k\Omega$ is connected to the output. [7 marks]

$A_d = g_m(r_{O2}||r_{O4}||R_L)$ [3]

$A_d = (3.846m)(1000k||1000k||250k) = 641$ [4]

Question 3 **[20 marks]**

The circuit parameters for the **emitter follower** circuit in **Figure 3** is V^+ **= 5 V,** V^- **= -5 V,** and R_L **= 1 kΩ**. The transistor parameters are V_{BE}**(on) = 0.6 V,** V_{CE}**(sat) = 0.3 V,** and $V_A = \infty$. **Neglect** base currents. The **output voltage** is varying from **-4.5 V** to **+4.5 V**.

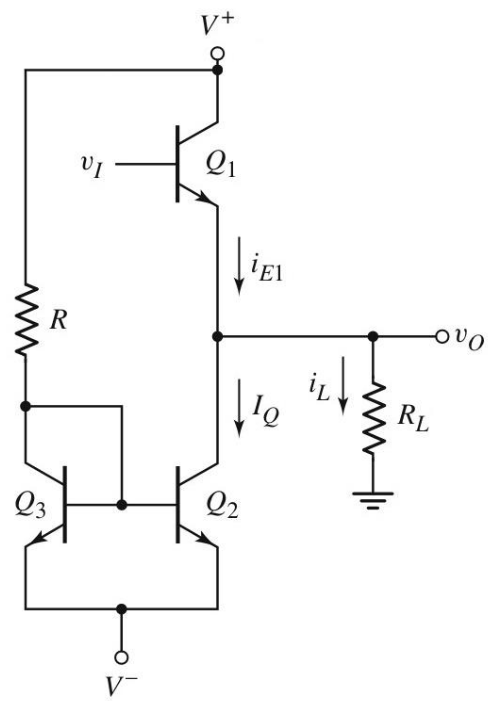

Figure 3

(a) **Find** the required I_Q and the value of R. [6 marks]

(b) For v_O **= 0 V**, **find** the power dissipated in the transistor Q_1, and the power dissipated in the current source (Q_2, Q_3, and R). [9 marks]

(c) **Determine** the conversion efficiency for a symmetric sine-wave output voltage with peak value of **8 V**. [5 marks]

Answers for Question 3

i) Find the minimum required I_Q and the value of R. [6 marks]

I_{Qmin} = |most negative I_L| = |vomin/R_L| [2]
= |-4.5V/1kq | = 4.5 mA [1]

R =$(V^+ - V_{BE3(on)} - V^-) / I_Q$ [2]
=(5 - 0.6 - (-5))/4.5m = 2.09 kq [1]

ii) For v_o = 0, find the power dissipated in the transistor Q_1, and the power dissipated in the current source (Q_2, Q_3, and R). [9 marks]

P_{Q1} = $(I_{C1})(V_{CE1})$ [1]
= $(I_Q)(V_{C1}-V_{E1})$ = (4.5m)(5-0) = 22.5 mW [1]

P_{Q2} = $(I_{C2})(V_{CE2})$ [1]
= $(I_Q)(V_{C2}-V_{E2})$ = (4.5m)(0--5) = 22.5 mW [1]

P_{Q3} = $(I_{C3})(V_{CE3})$ [1]
= $(I_Q)(V_{BEon})$ = (4.5m)(0.6) = 2.7 mW [1]

$P_{Resistor}$ = $(I)^2(R)$ [1]
= $(4.5m)^2(2.09k)$ = 42.3 mW [2]

iii) Determine the conversion efficiency for a symmetric sine-wave output voltage with peak value of 8V. [5 marks]

P_L = $0.5(Vp)^2/R_L$ [1]
= $0.5(4.5)^2/(1k)$ = 10.125 mW [1]
P_S = $(V^+-(V^-))(2I_Q)$ [1]
= (10)(2x4.5m) = 90 mW [1]
Power conversion efficiency = P_L/P_S x 100%
Efficiency = 10.125m/90mx100% = 11.25% [1]

Question 4 **[20 marks]**

For the circuit in **Figure 4**, the transistor parameters are $\boldsymbol{\beta = 100}$ and $V_A = \infty$. The dc bias currents are as indicated in the figure.

(a) Determine the input resistance $\boldsymbol{R_i}$. [12 marks]

(b) Determine the output resistance $\boldsymbol{R_o}$. [8 marks]

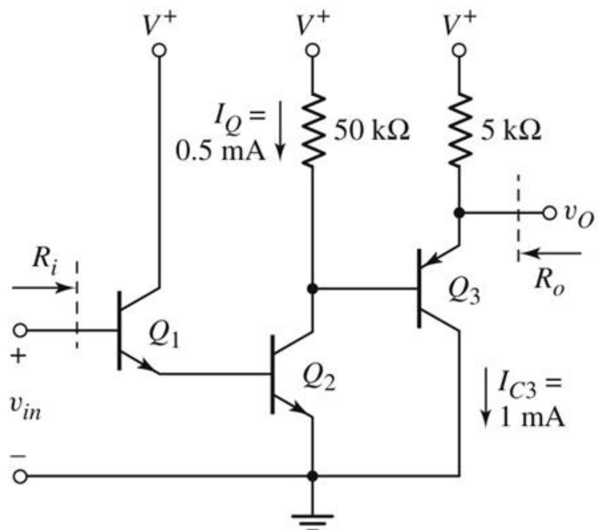

Figure 4

Answers for Question 4

I_{C1} = I_{C2} / (1+ɓ) = 0.5m/(101) = 4.95µA [2]

r´ 1 = ɓV_T / I_{C1} = (100)(0.026)/4.95µ = 530.5kÝ [2]

I_{C2} = I_Q + I_{B3} = 0.5m + I_{C3}/ɓ = 0.5m+0.01m = 0.51mA [2]

r´ 2 = ɓV_T / I_{C2} = (100)(0.026)/0.51m) = 5.098kÝ [3]

Ri = r´ 1 + (1+ɓ)r´ 2 = 530.5k +(101)(5.2k) = 1.056MÝ [3]

r´ 3 = ɓV_T / I_{C3} = (100)(0.026)/(1m) = 2.6kÝ [2]

ro2 = Ð

Re3 = r´ 3 + 50k//ro2 = r´ 3 + 50k = 52.6kÝ [3]

Ro = 5k // [Re3/(1+ɓ)] = 472Ý [3]

Appendix: BASIC FORMULA

BJT

$$i_C = I_S e^{v_{BE}/V_T} \text{ ; npn}$$

$$i_C = I_S e^{v_{EB}/V_T} \text{ ; pnp}$$

$$i_C = \alpha i_E = \beta i_B$$

$$i_E = i_B + i_C$$

$$\alpha = \frac{\beta}{\beta + 1}$$

;Small signal

$$\beta = g_m r_\pi$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

MOSFET

; N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n[v_{GS} - V_{TN}]^2$$

$$K_n = \frac{k_n^{'}}{2} \cdot \frac{W}{L}$$

; P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p[v_{SG} + V_{TP}]^2$$

$$K_p = \frac{k_p^{'}}{2} \cdot \frac{W}{L}$$

;Small signal

$$g_m = 2K_n\left(V_{GSQ} - V_{TN}\right) = 2\sqrt{K_n I_{DQ}}$$

$$r_o \cong \frac{1}{\lambda I_{DQ}}$$