UNIVERSITI TENAGA NASIONAL

COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 2 2014 / 2015

PROGRAMME	: **Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	: **EEEB273**
SUBJECT	: **ELECTRONIC ANALYSIS AND DESIGN II**
DATE	: **February 2015**
TIME	: **3 hours**

<u>INSTRUCTIONS TO CANDIDATES:</u>

1. This paper contains **Six** (6) questions in **Ten** (10) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided. **Use pen** to write your answer.
4. Write answer to different question on **a new page**.
5. For all calculations, assume that V_T = **26 mV**.

THIS QUESTION PAPER CONSISTS OF TEN* (10) *PRINTED PAGES INCLUDING THIS COVER PAGE.

<u>Question 1 [15 marks]</u>

The differential amplifier in **Figure 1** is biased by a two-transistor BJT current source (consists of R_1, Q_3 and Q_4). The transistor parameters are: β **= 100** and V_{EB}**(on) = 0.7 V.** The **Early** voltage for transistors Q_3 and Q_4 is $V_{A3} = V_{A4}$ **= 100 V;** while the **Early** voltage for transistors Q_1 and Q_2 is $V_{A1} = V_{A2} = \infty$**.** The differential amplifier **differential-mode gain is 40** and the **common-mode voltage gain is –0.005**. <u>State your assumptions</u> when you answer the following questions:

(a) **Determine** v_E and v_{EC1} for common-mode input voltage $v_1 = v_2 = v_{cm}$ = **-2.5 V**.

[5 marks]

(b) **Determine** the **output voltage** of the differential amplifier if for the inputs v_1 **= 210** $\sin \omega t$ μ**V** and v_2 **= 90** $\sin \omega t$ μ**V**. [6 marks]

(c) **Determine** the **common-mode input resistance** of the differential amplifier if

$$2R_{icm} = r_\mu \parallel [(1+\beta)(2R_o)] \parallel [(1+\beta)r_o]$$

[4 marks]

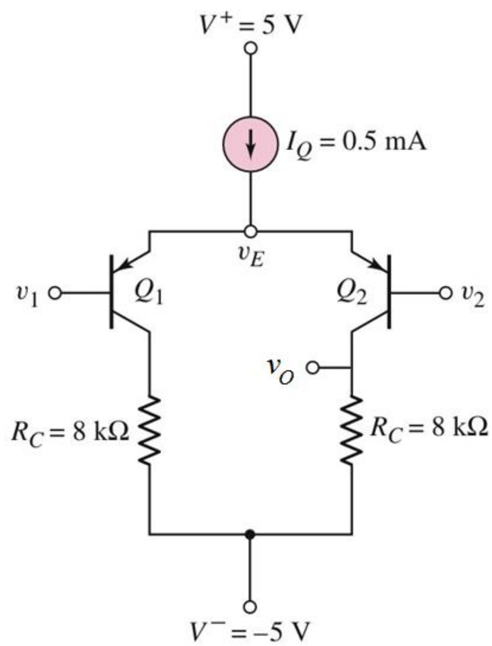


Figure 1

Q1 (a)

$V_E = V_1$ ï $V_{BE(on)}$ = -2.5 -0.7 = -3.2 [1.5]

V_{EC1} = v_E ï $I_{C1}R_C$ ï V- [1]

I_{C1} = [ɓ/(1+ɓ)]I_{E1} = [ɓ/(1+ɓ)]I_Q/2 = (100/101)(0.5m/2) = 0.2475mA [1.5]

V_{EC1} = -3.2 ï (0.2475m)(8k) ï (-5) = - 0.18V [1]

Q1(b)

$A_d = v_o/v_d = g_{m2}R_C/2$

OR

v_o = = ($g_{m2}R_C$/2) v_d [2]

g_{m2}= I_{C2}/V_T = 0.2475m/0.026 = 9.519mA/V [1]

v_d = v1 ï v2 = 210sin(wt) -90sin(wt) µV = 120 sin (wt) µV [1.5]

v_o = [(9.519m)(8k)(120µ sin(wt)]/2 = 4.569 sin (wt) µV [1.5]

Q1(c)

Assume rµ very large [0.5]

ro2 for for the diff-amp transistor is Ð [0.5]

Thus

2Ricm ≅ (1+ɓ)(2Ro) [1]

Ro is the output of a two-transistor current source [0.5]

Ro = V_A/I_Q = 100/0.5m = 200kÝ [1]

Ricm = (1+ɓ)Ro = (101)(200k) = 20.20MÝ [0.5]

Question 2 [15 marks]

Figure 2 shows a **MOSFET diff-amp with a cascode active load**. Assume that **NMOS** devices are available with the following parameters: V_{TN} **= 0.5 V**, k'_n **= 80** μ**A/V**^{2}, λ_n **= 0.02 V**$^{-1}$, and $(W/L)_1 = (W/L)_2$ **= 10**. Assume that **PMOS** devices are available with the following parameters: V_{TP} **= -1.0 V**, k'_p **= 40** μ**A/V**^{2}, and λ_p **= 0.02 V**$^{-1}$**.** The circuit parameters are V^+ **= 5 V** and V^- = **–5 V**. The bias current is I_Q **= 0.2 mA.**

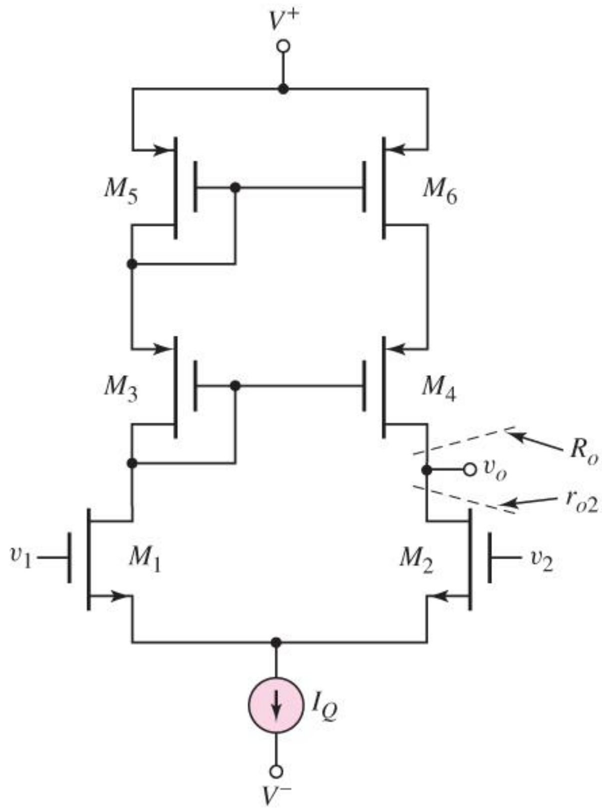


Figure 2

(a) **Determine** the output resistance, R_O, of the cascode active load. [9 marks]

(b) **Find** the differential-mode voltage gain, A_d. [6 marks]

Q2(a)

$R_O = r_{O4} + r_{O6}\,(1 + g_m r_{O4})$ **OR** R_O å $g_m\, r_{O4}\, r_{O6}$ [1]

and $r_O = \frac{1}{\lambda I_{DQ}}$ [1]

$I_{DQ} = {}^{I_Q}/_2 = {}^{0.2m}/_2 = 0.1mA$ [1]

$r_{O4} = r_{O6} = \frac{1}{\lambda I_{DQ}} = \frac{1}{(0.02)(0.1m)} = 500k\Omega$ [2]

Given that $g_m = 2\sqrt{K_{n} I_{DQ}}$; [1]

$$g_m = 2\sqrt{\frac{0.08}{2}(10)(0.1m)} = 0.4\frac{mA}{V}$$ [1]

$\therefore R_O = r_{O4} + r_{O6}\,(1 + g_m r_{O4}) = 500k + 500k\,(1 + (0.4)(500k)) =$ 101 MΩ [2]

OR R_O å $g_m\, r_{O4}\, r_{O6} = (0.4)(500k)(500k) =$ 100 MΩ [2]

Q2(b)

$A_d = g_m(r_{O2}\,||\,R_O)$ [2]

$A_d = 0.4m(500k\,||\,101M)$ [2]

$A_d = 200$ [2]

Question 3 [15 marks]

(a) **Describe** the operation of a **class-B** output stage as in **Figure 3**. The cut-in voltage for both transistors is **0.7 V**. How is this output stage different from the **idealized class-B** output stage? [3 marks]

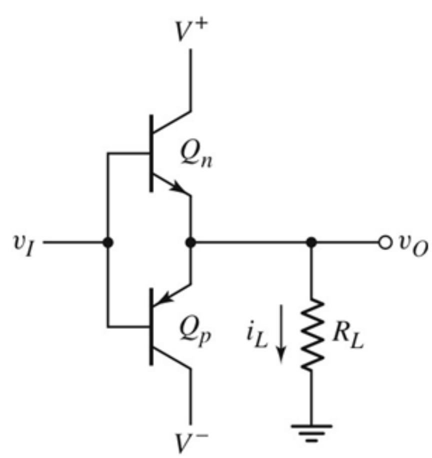


Figure 3

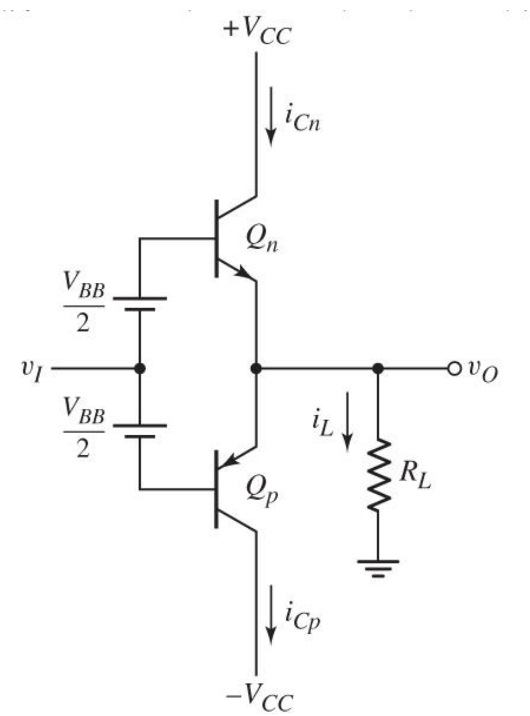


Figure 4

(b) A **class-AB** output stage with BJTs is shown in **Figure 4**. **Reverse saturation current** for every transistor is $\boldsymbol{I_S = 2\times10^{-15}}$ **A**. Assume $+V_{CC}$ **= +5 V**, $-V_{CC}$ **= 0 V**, and $\boldsymbol{R_L = 1\ k\Omega}$.

(i) **Find** V_{BB} when $\boldsymbol{v_I = 0}$, as such producing $\boldsymbol{i_{Cn} = i_{Cp} = 1}$ **mA**. [2 marks]

(ii) **Calculate** i_{Cn}, i_{Cp}, and v_I to obtain $\boldsymbol{v_O = -3.5}$ **V**. [8 marks]

(iii) **Calculate** the power dissipated in R_L. [2 marks]

<u>Q3 Answers:</u>

Q3(a)

Any of the following key-phrases:

(I) $v_I > +0.7$V, Q_n turns on and operates as emitter follower [1]
I_L is positive, supplied thru Q_n, B-E junction of Q_p is reverse-biased

(II) $v_I < -0.7$V, Q_p turns on and operates as emitter follower [1]
Q_p sinks I_L, which is negative, B-E junction of Q_n is reverse-biased

(III) v_O remains zero as long as $-0.7\text{V} \le v_I \le +0.7\text{V}$ [1]
Dead band: range of input voltage where v_O is zero
→ Where both transistors are cut-off

Q3(b)

(i) **Find V_{BB}:**

$i_{Cn} = I_S \exp(V_{BE}/V_T)$

$V_{BE} = V_T \ln(i_{Cn}/I_S) = (26\text{m}) \ln(1\text{m}/2\text{x}10^{-15}) = 0.7004$ V [1]

$V_{BB} = 2\, V_{BE} = 2 \text{ x } 0.7004 = 1.40077$ V [1]

(ii) **Calculate i_{Cn}, i_{Cp},** and v_I to obtain $v_O = -3.5$ **V**. [Total = 8]

$v_O = -3.5 \text{ V} = i_L R_L$

➔ $i_L = v_O/R_L = (-3.5\text{V})/(1\text{k}\Omega) = -3.5$ mA [1]

Therefore, Q_p is conducting and Q_n is OFF.

Approximate value, $i_{Cp} \approx i_L$

$i_{Cp} = I_S \exp(V_{EB}/V_T) = 3.5$ mA [0.5]

$V_{EB} = V_T \ln(i_{Cp}/I_S) = (26\text{m}) \ln(3.5\text{m}/2\text{x}10^{-15}) = 0.7329$ V [0.5]

$V_{BE} = V_{BB} - V_{EB} = 1.40077 - 0.7329 = 0.6678$ V [0.5]

➔ $i_{Cn} = I_S \exp(V_{BE}/V_T) = (2\text{x}10^{-15}) \exp(0.6678/0.026) = 0.2857$ mA [0.5]

$i_{Cn} = i_{Cp} + i_L$

➔ $i_{Cp} = i_{Cn} - i_L = 0.2857\text{m} - (-3.5\text{m}) = = 3.7857$ mA [0.5]

$V_{EB} = V_T \ln(i_{Cp}/I_S) = (26\text{m}) \ln(3.7857\text{m}/2\text{x}10^{-15}) = 0.734997$ V [0.5]

Actual values:

$V_{BE} = V_{BB} - V_{EB} = 1.40077 - 0.734997 = 0.66577$ V [0.5]

➔ $i_{Cn} = I_S \exp(V_{BE}/V_T) = (2\text{x}10^{-15}) \exp(0.66577/0.026) = 0.2642$ mA [0.5]

➔ $i_{Cp} = i_{Cn} - i_L = 0.2642\text{m} - (-3.5\text{m}) = 3.764$ mA [1]

$v_I = v_O - V_{EB} + V_{BB}/2 = -3.5 - 0.735 + 0.7004 = -3.535$ V [2]

(iii) The power dissipated in R_L,

$P_{RL} = i_L^2 R_L = (3.5)^2(1\text{k}) = 12.25$ mW [2]

Question 4 [20 marks]

Consider the multistage circuit in **Figure 5**. There are three distinctive stages namely the differential amplifier stage, the gain stage, and the output stage. The dc analysis performed by a software tool **LTSpice** on the multistage circuit resulted in an undesired value for the output voltage $\boldsymbol{v_O}$ **= -0.3625 V** (Refer to Appendix A). You are **to analyse the dc characteristics of the circuit by hand analysis** (manual analysis) using only your scientific calculator. Let the bias current from the **Widlar** current source be **0.4 mA**. Following the dc analysis, **identify assumptions** you have made that leads to the undesired output voltage. Thus, **advise** on how to rectify the output voltage to an ideal dc value and how to increase the small signal voltage gain to $\mathbf{10^4}$ **V/V**. You may illustrate your ideas by redrawing or redefining the circuit parameters.

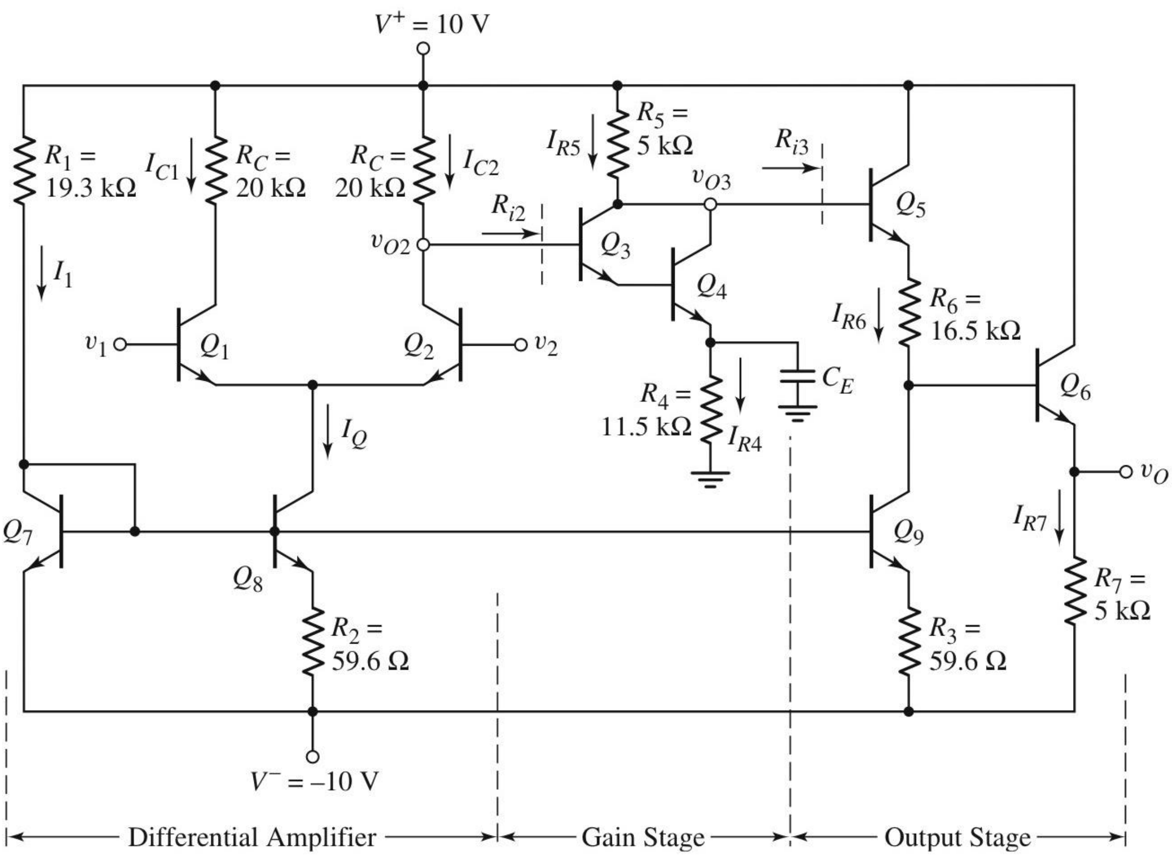


Figure 5

Q4

Input stage:

I_Q = 0.4 mA

I_{C2} = 0.2 mA (Neglect base current in Q1 and Q2) [2]

vo2 = V^+ - $I_{C2}R_C$ = 10 ï (0.2m)(20k) = 6.0V

Gain stage:

I_{R4} = [vo2 ï V_{BE3} ï V_{BE4}]/R4 (Assume V_{BE3} and V_{BE4} = 0.7V) [2]

I_{R4} = [6 - 2(0.7)]/11.5k = 0.4mA

I_{R4} = I_{R5} (Neglect base currents in Q3 and Q4) [2]

vo3 = V^+ - (I_{R5}R5) = 10-(04m)(5k) = 8V

Output Stage:

I_{R6} = I_Q (Parallel transistors with R3 = R2) [2]

(Neglect base current in Q6) [2]

vb6 = vo3 ï V_{BE5} ï I_{R6}R6 (Assume V_{BE5} = 0.7V) [2]

vb6 = 8- 0.7 ï (0.4m)(16.5k) = 0.7 V

vo = vb6-V_{BE7} = 0 (Assume V_{BE7} = 0.7V) [2]

The solution:

i. Base currents are neglected in all stages, dc voltage levels have been shifted several times through the stages. If the base currents are taken into account, the actual output voltage, vo, would not be at the ideal level of zero volt. Instead the dc level should be higher than calculated. In order to adjust the dc level shifts, due to neglecting the base currents, one of the following suggestions can be used to lover the output voltage to zero:
   a. R1 and R2 can be reduced to increase IQ
   b. R_C can be increased to reduce vo2
   c. R5 can be increased to reduce vo3
   d. R6 can be increased to raise the vb6 to a value equals to V_{BE7}

ii. The assumptions made for V_{BE} = 0.7 V for all transistors is also the cause for output voltage to shift several times throughout the stages. If V_{BE} = 0.6 V is used in the calculations, the output voltage, vo would be lower towards a negative value. To increase the output voltage back to zero level, the following can be suggested:
   a. Increase R2 and R3 to reduce I_Q
   b. Reduce R_C to increase vo2
   c. Reduce R5 to increase vo3
   d. Reduce R6 to increase vb6

<u>Marking Criteria:</u>

<u>Every assumption made</u> and mentioned in the analysis deserves 1 mark ï capped at [5 marks]

Analysis that leads to a value of vo = ± 0.5 V [5 marks]

Suggest any <u>two solutions</u> in (i) OR (ii) with explanation /reason for suggestions [6 marks]

Solution/s to improve gain to 10^4 - use active loads for diff-amp circuit [2 marks]

and specific configuration of active loads [2 marks]

<u>Question 5 [15 marks]</u>

Consider the bias circuit portion of the 741 op-amp in **Figure 6**. Assume that the transistor parameters of $\boldsymbol{I_S = 5 \times 10^{-16}}$ **A.** The bias voltages are given as $\pm$**15 V**.

(a) **Redesign** the bias circuit to obtain $\boldsymbol{I_{REF} = 0.4}$ **mA** and $\boldsymbol{I_{C10} = 40\ \mu}$**A**. **Determine** the values of $\boldsymbol{V_{BE11}}$, $\boldsymbol{V_{EB12}}$, and $\boldsymbol{V_{BE10}}$. **Neglect** the base currents. [9 marks]

(b) **Determine** the values of $\boldsymbol{I_{REF}}$ and $\boldsymbol{I_{C10}}$, using the <u>resistor values found in (a)</u> if $\boldsymbol{V_{BE}}$**(on) =** $\boldsymbol{V_{EB}}$**(on) = 0.6 V.** [6 marks]

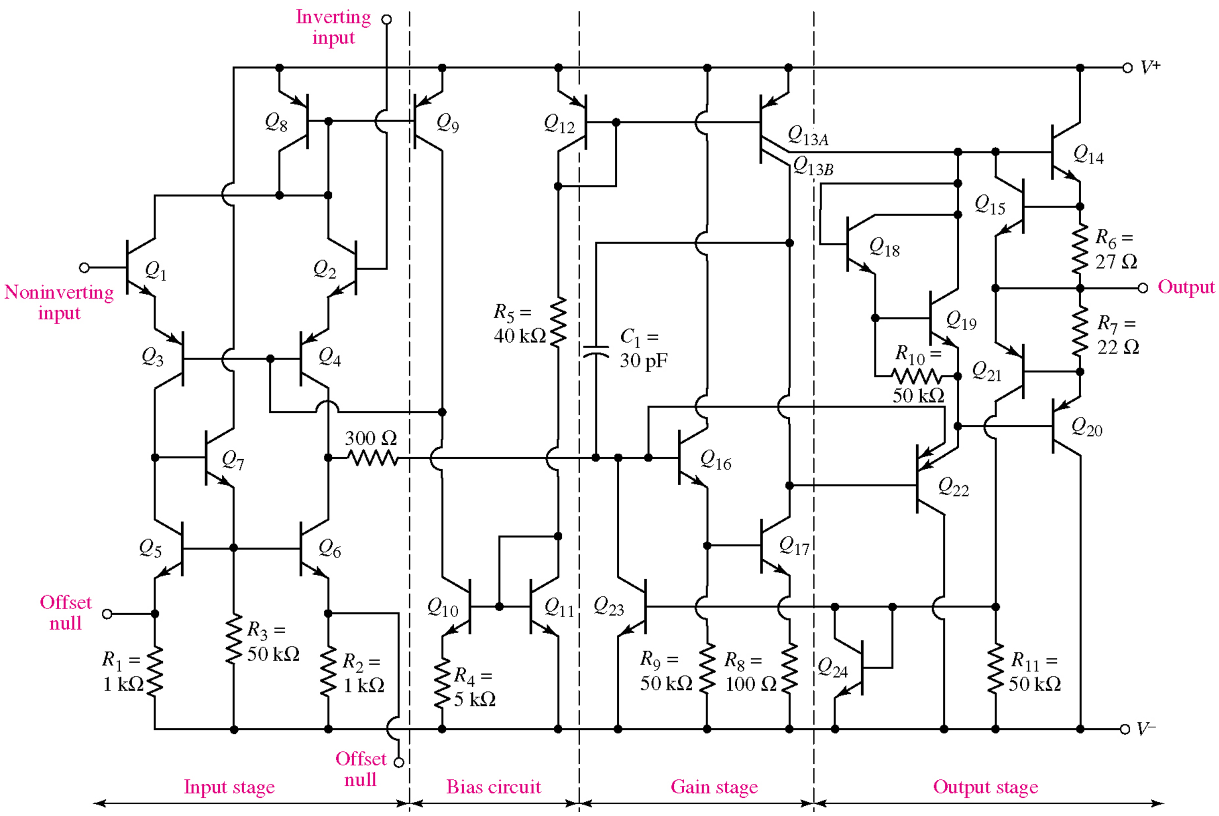


Figure 6

Q5(a)

Using the equation, $I_C = I_S exp^{V_{BE}/V_T}$ [1]

$V_{BE11} = V_{BE12} = V_T \ln\left(\frac{I_C}{I_S}\right)$ [1]

$V_{BE11} = 0.026 \ln\left(\frac{0.5 \times 10^{-3}}{5 \times 10^{-6}}\right) = \mathbf{0.7126\ V}$ [1]

Find R_5 and R_4;

$R_5 = \frac{V^+ - V_{EB12} - V_{BE11} - V^-}{I_{C10}} = \frac{15 - 0.7126 - 0.7126 + 15}{0.4m} = \mathbf{71.44\ k\Omega}$ [2]

$I_{C10} R_4 = V_T ln \frac{I_{REF}}{I_{C10}}$

$R_4 = \frac{0.026}{0.04m} ln \frac{0.4m}{0.04m} = \mathbf{1.497\ k\Omega}$ [2]

$V_{BE10} = V_{BE11} - I_{C10} R_4 = 0.7126 - 0.04m(1.497k) = \mathbf{0.6527\ V}$ [2]

Q5(b)

$I_{REF} = \frac{V^+ - V_{EB12} - V_{BE11} - V^-}{R_5} = \frac{15 - 0.6527 - 0.6527 + 15}{71.44k} = \mathbf{0.4017\ mA}$ [3]

$I_{C10} R_4 = V_T ln \frac{I_{REF}}{I_{C10}}$

$I_{C10}(1.497k) = (0.026) ln \frac{0.4017m}{I_{C10}} = \mathbf{0.05987\ mA}$ [3]

Question 6 [20 marks]

(a) With a **feedback resistor (R_2) of 250 kΩ**, **design** an amplifier using **op-amp** with a **closed-loop gain** which can be **varied between -10 to -25 V/V.** The closed-loop gain can be varied using a **potentiometer** (R_{1V}) and a fixed-value resistor (R_{1F}). **Draw clearly** your circuit design. [6 marks]

(b) Refer to **Figure 7**. Op-amp is ideal.

(i) **Derive** the expression for output v_O as a function of inputs v_{I1} and v_{I2}. [4 marks]

(ii) **Calculate** v_O when R_1 **= 50 kΩ**, R_2 **= 100 kΩ**, R_3 **= 20 kΩ**, R_4 **= 40 kΩ**, R_5 **= 20 kΩ**, v_{I1} **= +0.25 V**, and v_{I2} **= -0.40 V**. [2 marks]

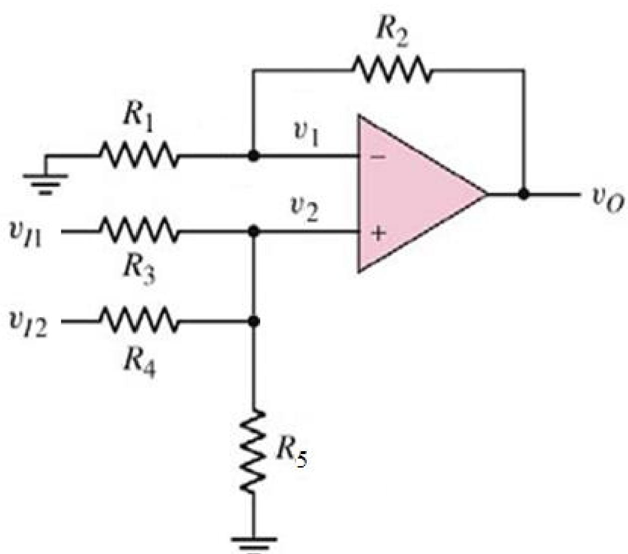


Figure 7

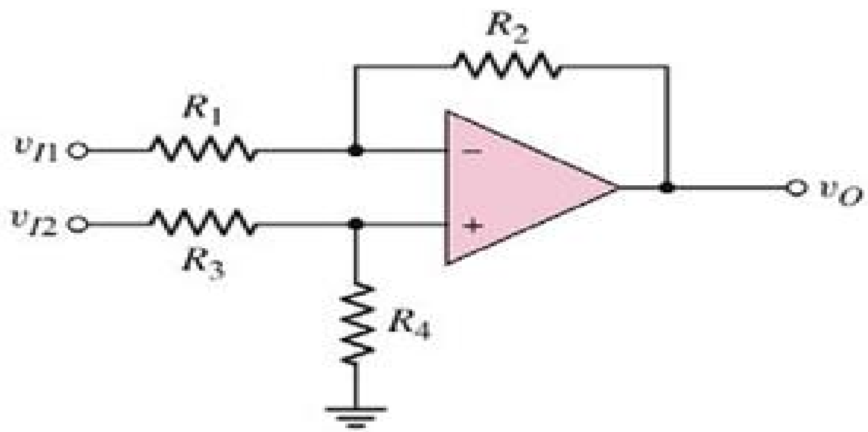


Figure 8

(c) **A general output equation** for a **difference amplifier** shown in **Figure 8** is

$$v_O = A_d v_d + A_{cm} v_{cm}$$

For the **difference amplifier** in the **Figure 8**, the circuit parameters are $\boldsymbol{R_1 = R_3 = 10}$ **kΩ,** $\boldsymbol{R_2 = 100}$ **kΩ,** and $\boldsymbol{R_4 = 110}$ **kΩ** and the output voltage equation is as follows:

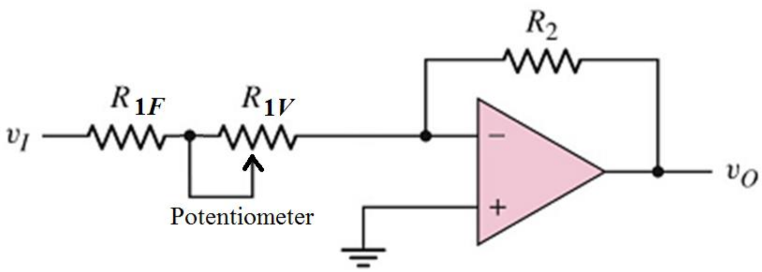
$$v_O = \left(1+\frac{R_2}{R_1}\right)\left(\frac{R_4/R_3}{1+R_4/R_3}\right)v_{I2} - \left(\frac{R_2}{R_1}\right)v_{I1}$$

where $v_{I1} = v_{cm} - \frac{v_d}{2}$ and $v_{I2} = v_{cm} + \frac{v_d}{2}$

Find A_d, A_{cm}, and then **calculate** the ***CMRR*** **in dB**. [8 marks]

-END OF QUESTION PAPER-

Q6(a)



[2]

A_v = $-R_2/(R_{1F} + R_{1V})$ [1]

R_2 = 250 kq . R_{1F} is a constant value resistor.

R_{1V} is a potentiometer. Gain is maximum, i.e. -25, when R_{1V} = 0 q .

A_{v1} = -25 = $-R_2/(R_{1F} + R_{1V})$ = -250k/(R_{1F} + 0) [1]

R_{1F} = 10 kq [0.5]

A_{v2} = -10 = $-R_2/(R_{1F} + R_{1V})$ = -250k/(10k + R_{1V}) [1]

R_{1V} = 15 kq [0.5]

Q6(b)(i)

$$v_O = \left(1 + \frac{R_2}{R_1}\right) v_1$$ [0.5]

$$v_1 = v_2$$ [0.5]

$$\frac{v_{I1} - v_2}{R_3} + \frac{v_{I2} - v_2}{R_4} = \frac{v_2 - 0}{R_5}$$ [1]

$$\frac{v_{I1}}{R_3} + \frac{v_{I2}}{R_4} = v_2\left(\frac{1}{R_3} + \frac{1}{R_4} + \frac{1}{R_5}\right)$$

$$v_2 = \frac{\frac{v_{I1}}{R_3} + \frac{v_{I2}}{R_4}}{\left(\frac{1}{R_3} + \frac{1}{R_4} + \frac{1}{R_5}\right)}$$ [1]

$$v_O = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{\left(\frac{1}{R_3} + \frac{1}{R_4} + \frac{1}{R_5}\right)} \left(\frac{v_{I1}}{R_3} + \frac{v_{I2}}{R_4}\right)$$ [1]

Q6(b)(ii)

$$v_O = \left(1+\frac{R_2}{R_1}\right)\frac{1}{\left(\frac{1}{R_3}+\frac{1}{R_4}+\frac{1}{R_5}\right)}\left(\frac{v_{I1}}{R_3}+\frac{v_{I2}}{R_4}\right) \quad [0.5]$$

$$v_O = \left(1+\frac{100k}{50k}\right)\frac{1}{\left(\frac{1}{20k}+\frac{1}{40k}+\frac{1}{20k}\right)}\left(\frac{0.25}{20k}+\frac{-0.40}{40k}\right) \quad [1]$$

$$v_O = (3)\frac{40k}{5}\left(\frac{0.25}{20k}+\frac{-0.40}{40k}\right) = 0.06\text{ V} \quad [0.5]$$

Q6(c)

$R_1 = R_3 = 10$ kΩ, $R_2 = 100$ kΩ, and $R_4 = 110$ kΩ

$$v_O = \left(1+\frac{R_2}{R_1}\right)\left(\frac{R_4/R_3}{1+R_4/R_3}\right)v_{I2} - \left(\frac{R_2}{R_1}\right)v_{I1}$$

$$v_O = \left(1+\frac{100\text{k}}{10\text{k}}\right)\left(\frac{110\text{k}/10\text{k}}{1+110\text{k}/10\text{k}}\right)v_{I2} - \left(\frac{100\text{k}}{10\text{k}}\right)v_{I1}$$

$$v_O = (1+10)\left(\frac{11}{12}\right)v_{I2} - 10v_{I1} \quad \boxed{2}$$

$$v_O = 10.083v_{I2} - 10v_{I1} = 10.083(v_{cm}+\frac{v_d}{2}) - 10(v_{cm}-\frac{v_d}{2})$$

$$v_O = 10.0415v_d + 0.083v_{cm} \quad \boxed{2}$$

***A_d* = 10.0415, *A_{cm}* = 0.083** $\boxed{1, 1}$

***CMRR* = 20 $\log_{10}$[10.0415/0.083] = 41.65 dB** $\boxed{2}$

APPENDIX A

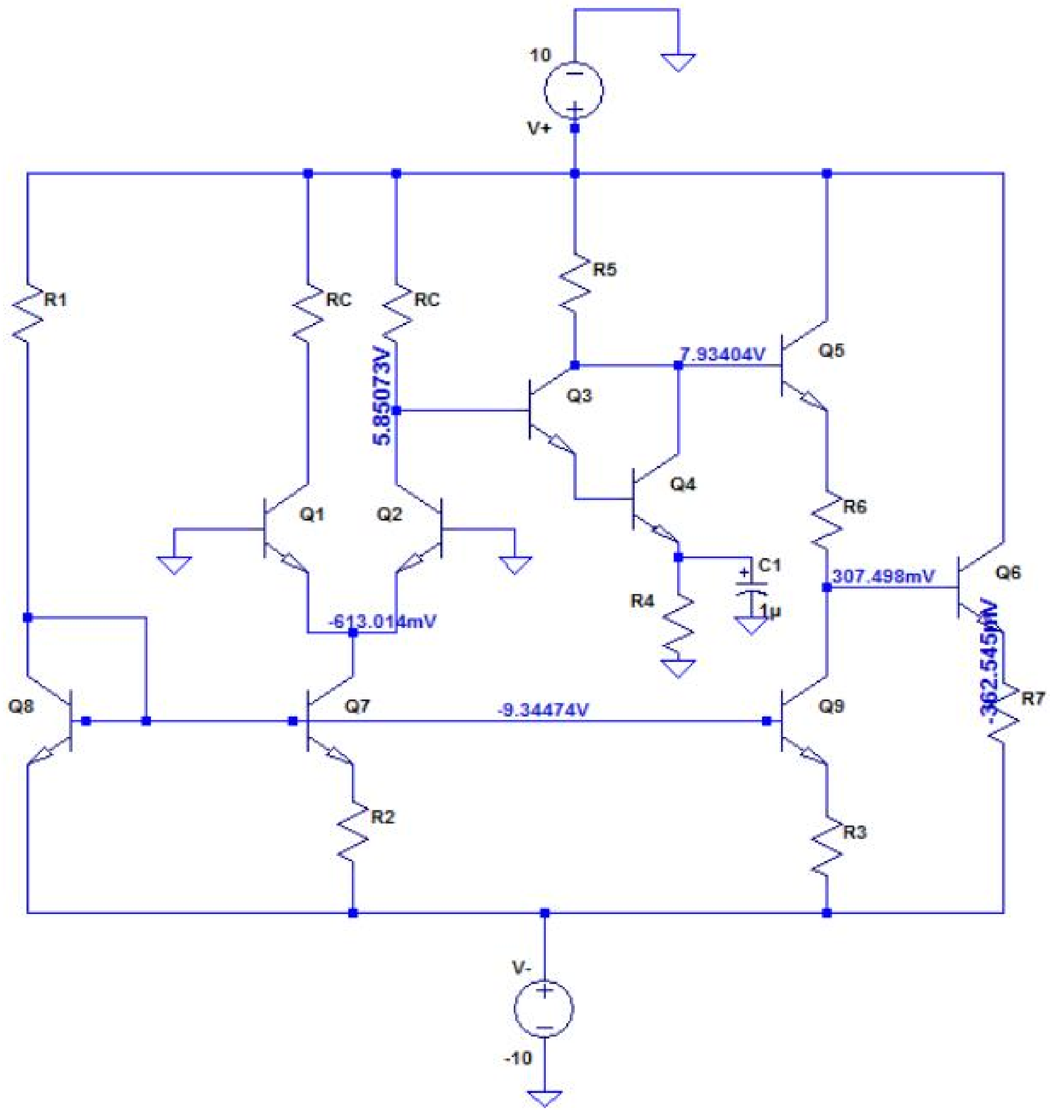


Figure A-1: LTSpice Simulation for Figure 5 in Question 4.

APPENDIX B

BASIC FORMULA

BJT

$$i_C = I_S e^{v_{BE}/V_T} \text{; NPN}$$

$$i_C = I_S e^{v_{EB}/V_T} \text{; PNP}$$

$$i_C = \beta i_B = \alpha i_E$$

$$i_E = i_B + i_C$$

$$\alpha = \frac{\beta}{\beta + 1}$$

;Small signal

$$\beta = g_m r_\pi$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

MOSFET

;N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n[v_{GS} - V_{TN}]^2$$

$$K_n = \frac{\mu_n C_{ox} W}{2L} = \frac{k_n'}{2} \cdot \frac{W}{L}$$

;P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p[v_{SG} + V_{TP}]^2$$

$$K_p = \frac{\mu_p C_{ox} W}{2L} = \frac{k_p'}{2} \cdot \frac{W}{L}$$

;Small signal

$$g_m = 2\sqrt{K_? I_{DQ}}$$

$$r_o \cong \frac{1}{\lambda I_{DQ}}$$