Name:
Student ID Number:
Section:
Table Number:
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UNIVERSITI TENAGA NASIONAL

College of Engineering
Department of Electronics and Communication Engineering

Test 2

SEMESTER 2, ACADEMIC YEAR 2014/2015

Subject Code	:	**EEEB273**
Course Title	:	**Electronics Analysis & Design II**
Date	:	**17 January 2015**
Time Allowed	:	**1 hour 45 minutes**

Instructions to the candidates:

1. Write your Name, Student ID Number, Section, and Table number. Indicate your Lecturer.
2. Write all your answers **using pen**. **DO NOT USE PENCIL** except for the diagram.
3. **ANSWER ALL QUESTIONS.**
4. **WRITE YOUR ANSWER ON THIS QUESTION PAPER.**
5. For all calculations, use $V_T = 26$ **mV** when necessary.

NOTE: DO NOT OPEN THE QUESTION PAPER UNTIL INSTRUCTED TO DO SO.

☺ **GOOD LUCK!** ☺

Question No.	1	2	3	Total
Marks				

Question 1 **[40 marks]**

The circuit in **Figure 1** has a pair of npn bipolar transistors as input devices and three-pnp-bipolar-transistor circuit connected as an active load. The differential amplifier circuit is biased with a constant current source I_Q **= 0.2 mA** that has and output resistance R_{OCS} **= 50 MΩ**. The transistor parameters are: β **= 100**, $V_{A1} = V_{A2}$ **= 100 V**, $V_{A3} = V_{A4}$ **= 60 V**, and $V_{A5} = \infty$.

(a) **Calculate** I_O such that the dc currents in the differential amplifier are **balanced**, that is $I_1 = I_2 = I_3 = I_4$. [10 marks]

(b) **Calculate** the open-circuit differential-mode voltage gain A_d. [15 marks]

(c) **Determine** R_L such that the differential-mode voltage gain is reduced to **90%** of its open-circuit value. [8 marks]

(d) **Design** a better active load circuit that can replace the active load in **Figure 1**. **Discuss** why your design is better than the circuit in **Figure 1**. [7 marks]

Answer for Question 1

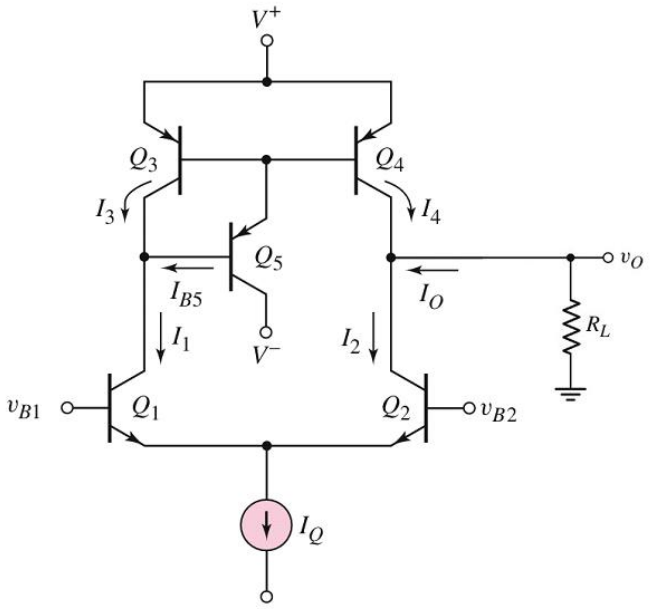


Figure 1

Answer for Question 1

(a)

$I_O = I_{B5}$ [1]

$I_{B5} = I_{E5}/(1+ \beta)$ [1]

$= (I_{B3}+I_{B4})/(1+ \beta)$ [2] must indicate currents in Figure 1

$= (I_{C3}+I_{C4})/[\beta(1+ \beta)]$ [1]

$= (I_{C1}+I_{C2})/[\beta(1+ \beta)]$ [1]

$= \beta(I_{E1}+I_{E2})/[(1+ \beta)(\beta)(1+ \beta)]$ [1]

$= \beta I_Q/[(1+ \beta)(\beta)(1+ \beta)]$ [1]

$= (100)(0.2m)/[(101)(100)(101)]$ [1]

$= 19$ nA [1]

(b) $I_{C2} = \beta I_E/(1+ \beta)$ [1]

$= \beta I_Q/[2(1+ \beta)]$ [1]

$= (100)(0.2m)/2(101) = 0.0990$ mA [1]

$r_{O2} = V_{A2}/I_{C2} = 100/0.0990$ m $= 1.01$ MÝ [3]

$r_{O4} = V_{A4}/I_{C4} = 60/0.0990$ m $= 606.1$ kÝ [2]

$R_O = r_{O2} \text{Ɛ} r_{O4} = 1.01\text{MƐ}\ 606.1\text{k} = 378.8$ kÝ [2]

$g_m = I_{C2}/V_T = (0.0990\text{m})/(0.026) = 3.808$ mA/V [2]

$A_d = g_m(R_O) = (3.808\ \text{m})(\ 378.8\ \text{k}) = 1442$ [3]

(c) New $R_{ON} = R_O \text{Ɛ}\ R_L$ [2]

$= R_O R_L/(R_O+R_L)$

$A_{vN} = (90\%)(1442) = 1298$ [1]

Thus $1298 = g_m(R_{ON}) = [g_m R_O R_L]/(R_O+R_L)$ [2]

$1298(R_O+R_L) = 1442R_L$

$R_L = (1298\ R_O)/(1442-1298)$

$= (1298)(378.8\text{k})/144 = 3414$ kÝ [3]

(d) Use cascode current source as active load [2]

Draw the circuit incorporated in diff-amp [1]

OR

Use wilson current source as active load

Advantage: Increases output resistance of the diff-amp, help reduces the loading effect when load is connected because output resistance of cascode configuration is βr_{O4} which is at least 10X larger than that in the circuit in Figure 1.

This larger output resistance definitely increase the differential mode voltage gain of the diff-amp. [2]

Disadvantage: The dc level shifts at the output need to be corrected. [1]

NOTE: Part (d) can have any reasonable and logical answer provide the justification.

Question 2 **[30 marks]**

A **Class-B output stage**, with a complementary pair transistors, as in **Figure 2** has V_{CC} = ±**10 V,** V_{BE}**(on) = 0.6 V**, and R_L **= 100 Ω.** The output signal voltage is v_O **= 10 sin** ω**t V**. The average power supplied by V^+ and V^- to a **Class-B** output stage is given as $2V_{CC}[Vp/(\pi R_L)]$**.**

(a) **Determine** the input voltage, V_I, to ensure that V_O **= 0**. **Sketch** the voltage transfer characteristics of the output stage. [5 marks]

(b) **Describe** the operation of a *complementary push-pull* output stage based on **Figure 2**. [3 marks]

(c) **Calculate** the average power to the load, $\overline{P}_L$. [6 marks]

(d) **Calculate** the average power dissipated in **each transistor**. [6 marks]

(e) **Determine** the conversion efficiency, η, of the output stage. [10 marks]

Answer for Question 2

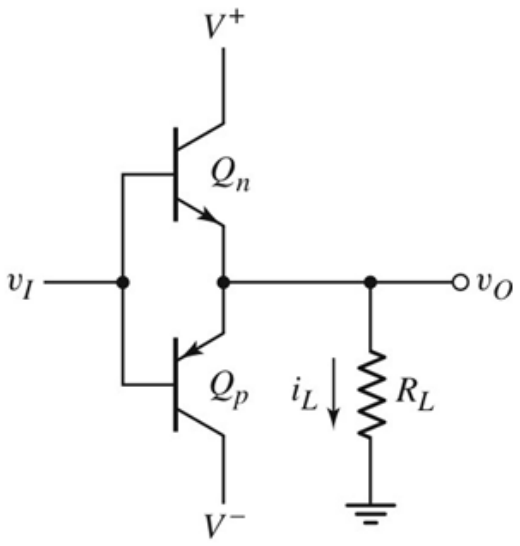
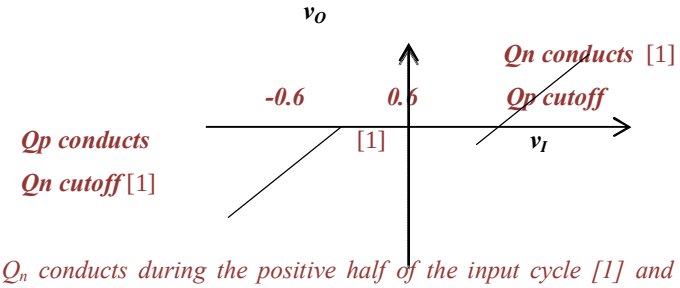


Figure 2

Answer for Question 2

(a) *The cut-in voltage is 0.6 V, so, -0.6 ≤ V_I ≤ 0.6 V* [2].

The voltage transfer characteristics of the output stage is: [5 marks]



(b) *Q_n conducts during the positive half of the input cycle [1] and Q_p conducts during the negative half-cycle [1]. Only one transistor conducts at one time [1].* [3 marks]

(c) Calculate the average power to the load, $\overline{P}_L$. [6 marks]

$\overline{P_L} = \frac{1}{2}\frac{V_p^2}{R_L}$ [2]

$\overline{P_L} = \frac{1}{2}\frac{(10)^2}{100}$ [2]

P_L= **0.5 W** [2]

(d) Calculate the average power dissipated in each transistor. [6 marks]

For 0 Òωt Òπ ;

$\overline{P_Q} = \frac{V_{CC}V_p}{\pi R_L} - \frac{V_p^2}{4R_L}$ [2]

$\overline{P_Q} = \frac{(10)(10)}{100\pi} - \frac{10^2}{4(100)}$ [2]

$\overline{P_Q}$= **0.06826 W** [2]

(e) Determine the conversion efficiency, η, of the output stage. [10 marks]

$\overline{P_S} = 2V_{CC}\left(\frac{V_p}{\pi R_L}\right)$ [2]

$\overline{P_S} = 2(10)\left(\frac{10}{100\pi}\right)$ [2]

= **0.6365 W** [2]

Hence,

$\eta = \frac{\overline{P_L}}{P_S} \times 100\%$ [2]

= 0.5/0.6365 × 100% = **78.5%** [2]

Question 3 **[30 marks]**

A simplified bipolar op-amp is designed as shown in **Figure 3**. ***Note that biasing for amplifiers in the circuit is provided by two-transistor current mirrors***. Study the figure carefully. Neglect base currents. Assume parameters for all transistors are: V_{BE}**(on)** = 0.7V, β **= 100,** and $V_A = \infty$.

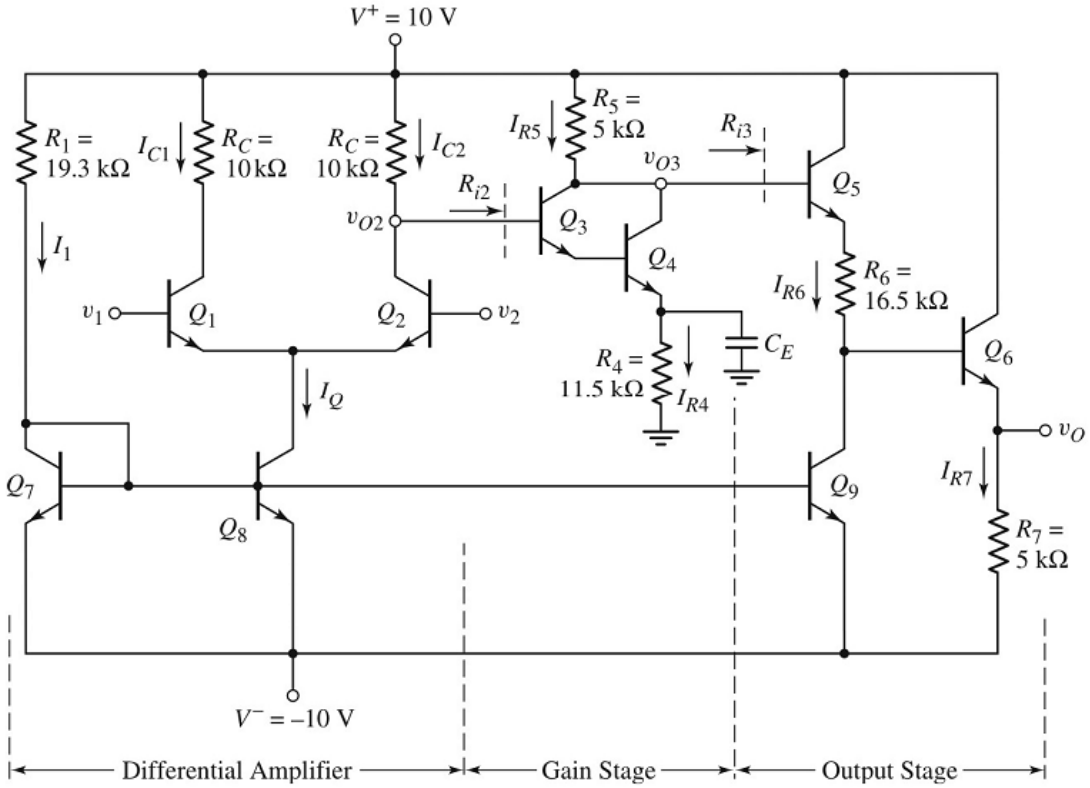


Figure 3

(a) Referring to **Figure 3,** given I_Q **= 1 mA.** Find I_{C2}**,** I_{R4}**,** I_{R5}**,** v_{O2}**,** and v_{O3} for $v_1 = v_2 = 0$ **V.** [15 marks]

(b) With small-signal analysis values for A_{d1}**,** $r_{\pi 3}$**,** R_{i2}**,** and A_2 can be found using the following formula:

$$A_{d1} = \left(\frac{V_{o2}}{v_d}\right) = \frac{g_{m2}}{2}\left(R_C \| R_{i2}\right)$$

$$r_{\pi 3} \cong \beta r_{\pi 4}$$

$$R_{i2} = r_{\pi 3} + (1+\beta) r_{\pi 4}$$

$$A_2 \cong \frac{I_{R4}}{2V_T}\left(R_5\right)$$

Calculate A_{d1}**,** A_2**,** and the total overall small-signal voltage gain, A_d**.** [15 marks]

Answer for Question 3

(a)

Given I_Q **= 1 mA**

I_{C2} **=** I_Q **/ 2** **= 0.5 mA** **[3]**

v_{O2} **=** V^+ **-** I_{C2} R_C **= 10 – (0.5m)(10k) = 5 V** **[3]**

I_{R4} **=** $(v_{O2}$ **- 2** V_{BE}**(on)) / (**R_4**)**

= (5 – 1.4) / (11.5k) **= 0.313 mA** **[3]**

I_{R5} **≈** I_{R4} (neglecting base currents) **= 0.313 mA** **[3]**

v_{O3} **=** V^+ **-** I_{R5} R_5 **= 10 – (0.313m)(5k) = 8.44 V** **[3]**

(b)

Using I_{C2} **= 0.5 mA,** I_{R4} **= 0.313 mA:**

A_{d1} **=** $(g_m$ **/ 2)(**R_C **||** R_{i2}**)**

g_{m2} **=** I_{C2} **/** V_T **= (0.5mA)/(26mV) = 19.23 mA/V** **[2]**

$r_{\pi 4}$ **=** βV_T **/** I_{R4} **= (100x26m)/(0.313m) = 8.306 kΩ** **[2]**

$r_{\pi 3}$ **≈** β $r_{\pi 4}$ **= 830.6 kΩ** **[2]**

R_{i2} **=** $r_{\pi 3}$ **+ (1 +** β**)** $r_{\pi 4}$

= 830.6k + (101)(8.306k) **= 1669.5 kΩ** **[2]**

A_{d1} **= (19.23m/2)(10k || 1669.5k) = 95.58** **[2]**

A_2 **≈ (**I_{R4} **/2**V_T**)** R_5 **= (0.313m/(2x26m))(5k) = 30** **[2]**

A_3 **≈ 1** **[1]**

A_d **=** A_{d1} A_2 A_3 **= 95.58 x 30 x 1 = 2867** **[2]**