COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 2 2015 / 2016

PROGRAMME	: **Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	: **EEEB273**
SUBJECT	: **ELECTRONIC ANALYSIS AND DESIGN II**
DATE	: **February 2016**
TIME	: **3 hours**

<u>INSTRUCTIONS TO CANDIDATES:</u>

1. This paper contains **FIVE** (5) questions in **NINE** (9) pages.
2. Answer **ALL** questions.
3. Write **ALL** answers in the answer booklet provided. **Use pen** to write your answer.
4. Write answer to different question on **a new page**.
5. **Show clearly all calculations, complete with proper Unit for every parameter.**

THIS QUESTION PAPER CONSISTS OF NINE* (9) *PRINTED PAGES INCLUDING THIS COVER PAGE.

Question 1 [20 marks]

Figure 1 shows a BJT differential amplifier **biased by a BJT cascode current source**. Transistor Q_1 and Q_2 in the differential amplifier have the transistor parameters of $\beta = 150$, $V_{BE}(on) = 0.7$ V, and $V_A = \infty$. Transistor Q_3, Q_4, Q_5, and Q_6 in the **cascode** current source have the transistor parameters of $\beta = 50$, $V_{BE}(on) = 0.7$ V, and $V_A = 250$ V.

The circuit parameters are: $V^+ = 10$ V, $V^- = -10$ V, and $I_{REF} = 0.5$ mA. Output for the differential is taken as **one-sided output** at v_{C2}.

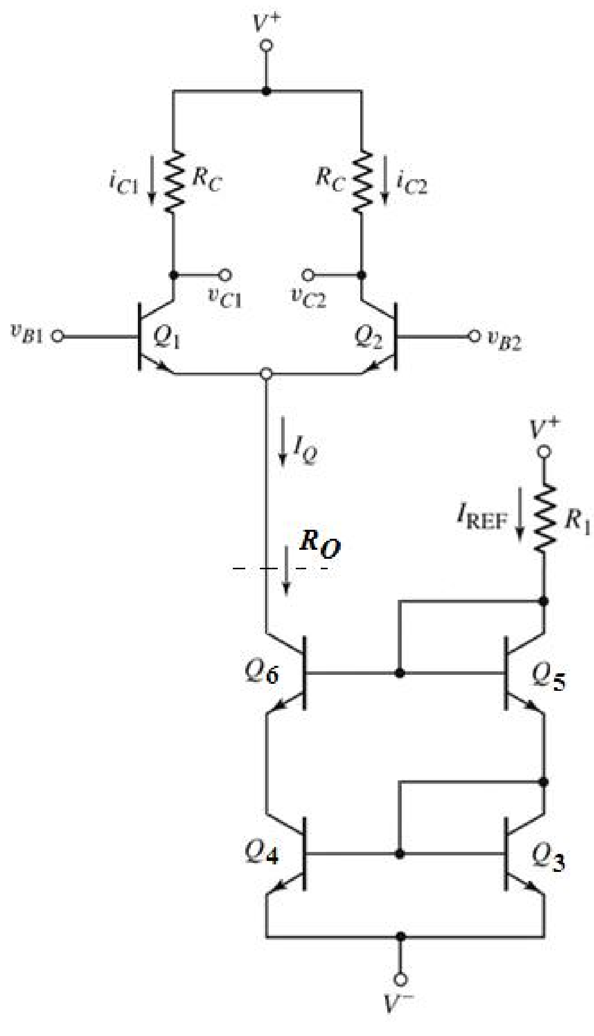


Figure 1

(a) **Calculate R_1** and the **output resistance (R_O)** of the **cascode** current source looking into the collector of Q_6. [7.5 marks]

(b) **Determine** the **value of R_C** if the **differential-mode voltage gain (A_d)** of the differential amplifier is **200 V/V**? [5 marks]

(c) **Find** the **common-mode voltage gain (A_{cm})** of the differential amplifier using the values found in **part (a)** and **(b)**. The equation for calculating A_{cm} is given as

$$A_{cm} = \frac{-g_{m2}R_C}{1 + \dfrac{2(1+\beta)R_O}{r_{\pi 2}}}$$ [6 marks]

(d) **Suggest how** the common-mode voltage gain (A_{cm}) can be reduced. [1.5 marks]

Question 2 [20 marks]

Figure 2 shows a differential amplifier with a pair of **PMOS** transistors as input devices. The circuit is biased with $I_Q = 0.2$ **mA**, and the transistor parameters are: $g_m = 0.2$ **mA/V**, $K_n = K_p = 0.1$ **mA/V**^{2}, $\lambda_n = 0.01$ **V**$^{-1}$, $\lambda_p = 0.015$ **V**$^{-1}$, $V_{TN} = 1$ **V**, and $V_{TP} = -1$ **V**. A pair of **NMOS** transistors is then connected to the circuit as an active load.

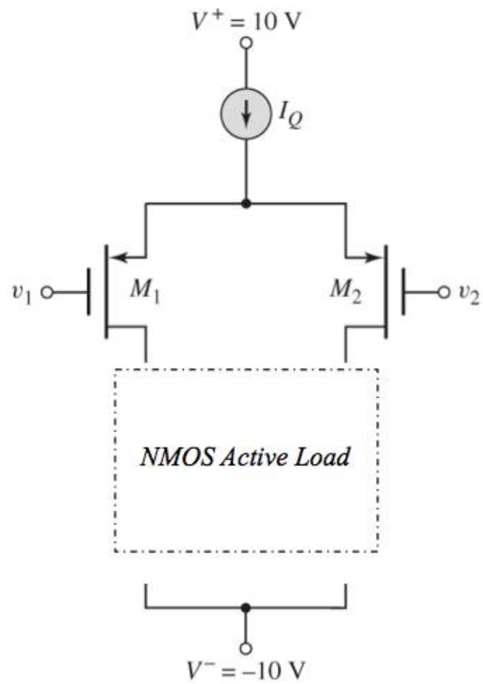


Figure 2

(a) **Draw** the complete circuit of a differential amplifier with NMOS active load, as shown in **Figure 2**. [5 marks]

(b) **Find** the **quiescent drain-to-source voltage** in each transistor (i.e. V_{DS} or V_{SD} of each transistor) when $V_{G1} = V_{G2} = 0$ Volt. [5 marks]

(c) **Determine** the open-circuit differential-mode voltage gain, A_d. [5 marks]

(d) **Calculate** the output resistance, R_O, of differential amplifier with active load in **Figure 2**. [5 marks]

Question 3 [20 marks]

(a) Consider the **Class-A** emitter-follower circuit shown in **Figure 3**. The circuit parameters are V^+ **= 12 V** and V^- **= -12 V**. Assume all transistors are matched with V_{BE}**(on)** = **0.7 V**, V_{CE}**(sat)** = **0.2 V**, and $V_A = \infty$. **An average power** of **50 mW** is to be delivered to the load R_L = **25 Ω**. **Design** the circuit such that the **minimum current** i_{E1} is **20%** of I_Q.

[10 marks]

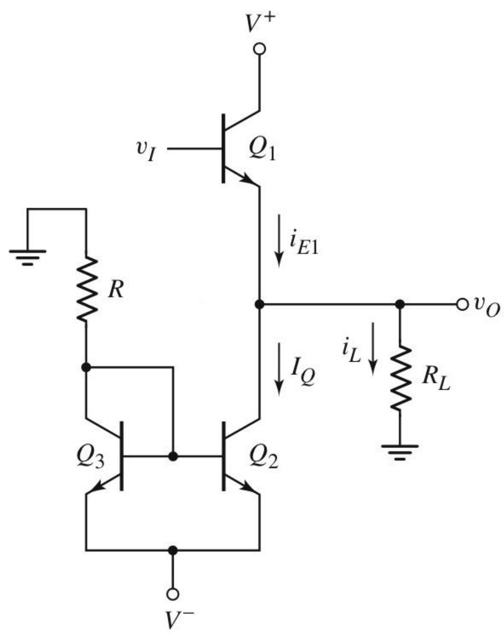


Figure 3

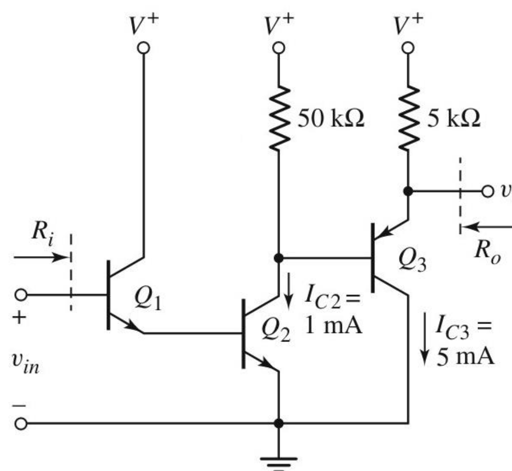


Figure 4

(b) **Determine** the **input resistance** (**R_i**) and **output resistance** (**R_o**) of the circuit in **Figure 4**. Let the transistor parameters β = **60** and $V_A = \infty$.

[10 marks]

Question 4 [20 marks]

Assume the transistor parameters of $|V_T|$ **= 0.6 V** and λ **= 0.015 V^{-1}** for **all** transistors, k'_n **= 100 μA/V^2**, k'_p **= 40 μA/V^2**, and circuit parameters of V^+ **= +5 V** and V^- **= -5 V**, and R_{set} **= 150 kΩ**. **Given** that the aspect ratios $(W/L)_{3,4}$ **= 10** for transistors M_3 and M_4, and (W/L) **= 20** for other transistors, **determine** the **overall small signal differential-mode voltage gain** for the **MC14573** op-amp in **Figure 5**. [20 marks]

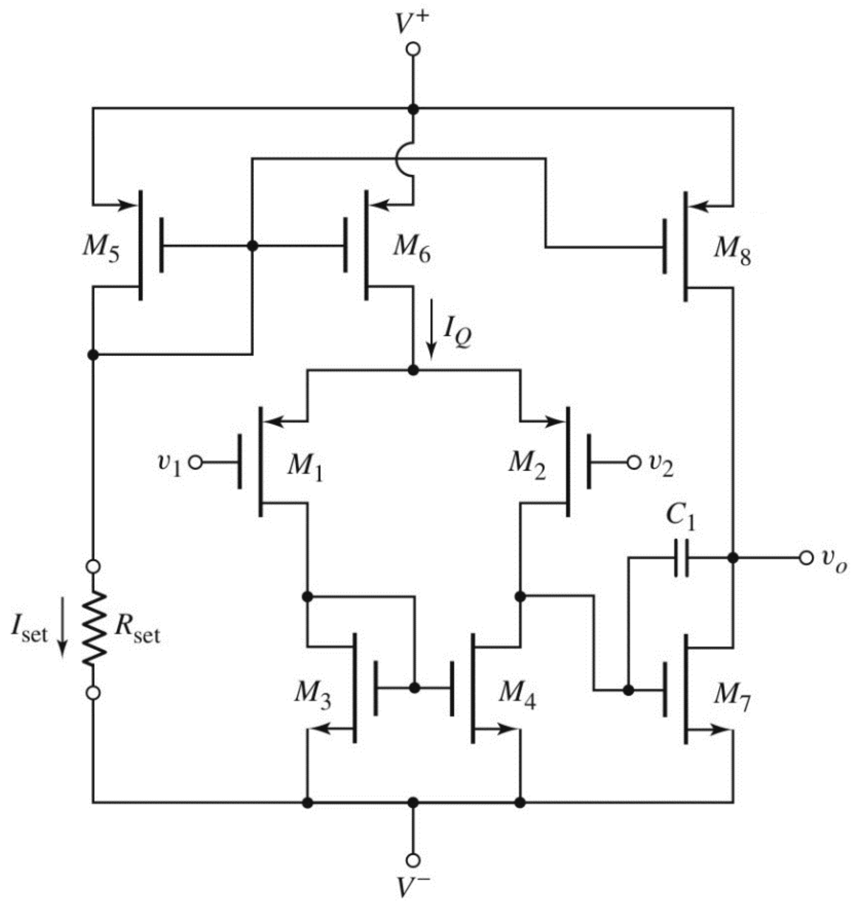


Figure 5

Question 5 [20 marks]

(a) With a **feedback resistor (R_2)** of **250 kΩ**, **design** an amplifier using op-amp in non-inverting configuration with a **closed-loop gain** which can be **varied from 11 to 51 V/V.** The closed-loop gain can be varied using a **potentiometer (R_{1V})** and a **fixed-value resistor (R_{1F})**. **Draw and label clearly** your circuit design. [6 marks]

(b) For an **amplifier circuit** using op-amps shown in **Figure 6**, use appropriate ideal op-amp characteristics to **show** that

$$v_O = v_{I1} + v_{I2}$$

when $R_1 = R_2 = R_F = 100\ \text{k}\Omega$. [6 marks]

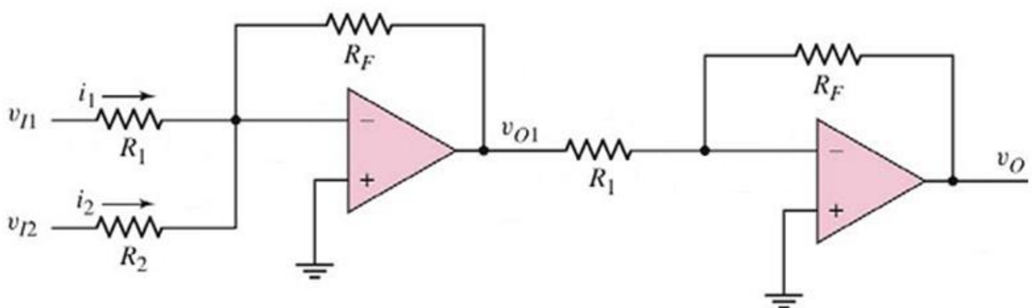


Figure 6

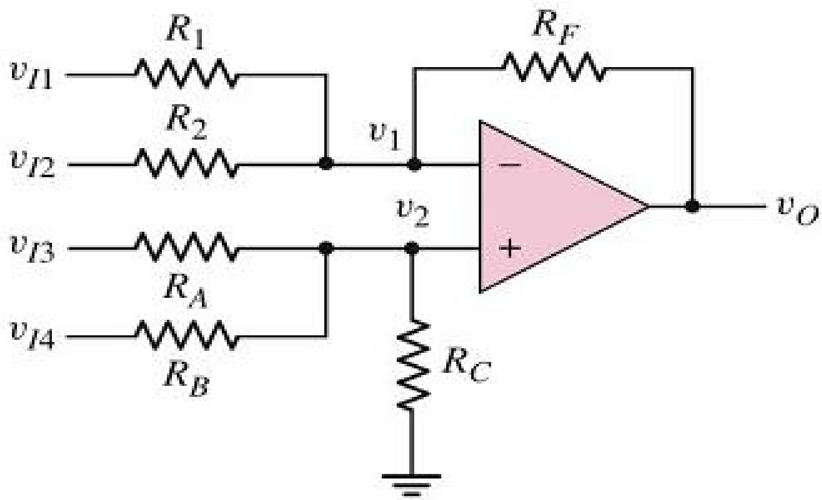


Figure 7

(c) For a **generalized summing op-amp** shown in **Figure 7** the **total output voltage (v_O)** is the **sum of the individual terms**, or

$$v_O = -\frac{R_F}{R_1}v_{I1} - \frac{R_F}{R_2}v_{I2} + \left(1+\frac{R_F}{R_N}\right)\left(\frac{R_P}{R_A}v_{I3} + \frac{R_P}{R_B}v_{I4}\right)$$

where $R_N = R_1 \| R_2$

$R_P = R_A \| R_B \| R_C$

With the **smallest resistor value** allowable in the circuit is **25 kΩ, design** a summing op-amp similar to **Figure 7** to produce the output of

$$v_O = -10v_{I1} - 5v_{I2} + 2v_{I3} + 5v_{I4}$$

[8 marks]

-END OF QUESTION PAPER-

APPENDIX:

A) BASIC FORMULA FOR TRANSISTOR

BJT

$$i_C = I_S e^{v_{BE}/V_T} \quad ;\text{NPN}$$

$$i_C = I_S e^{v_{EB}/V_T} \quad ;\text{PNP}$$

$$i_C = \beta i_B = \alpha i_E$$

$$i_E = i_B + i_C$$

$$\alpha = \frac{\beta}{\beta + 1}$$

;Small signal

$$\beta = g_m r_\pi$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

$$V_T = 26\,\text{mV}$$

MOSFET

;N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n[v_{GS} - V_{TN}]^2$$

$$K_n = \frac{\mu_n C_{ox} W}{2L} = \frac{k_n^{'}}{2} \cdot \frac{W}{L}$$

;P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p[v_{SG} + V_{TP}]^2$$

$$K_p = \frac{\mu_p C_{ox} W}{2L} = \frac{k_p^{'}}{2} \cdot \frac{W}{L}$$

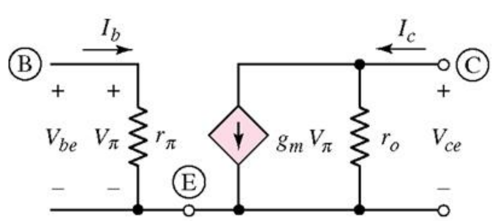
;Small signal

$$g_m = 2\sqrt{K_? I_{DQ}}$$

$$r_o \cong \frac{1}{\lambda I_{DQ}}$$

B) HYBRID-´ EQUIVALENT CIRCUITS

BJT



MOSFET