COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION
SOLUTION
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PROGRAMME	: Bachelor of Electrical & Electronics Engineering (Honours) Bachelor of Electrical Power Engineering (Honours)
SUBJECT CODE	: EEEB273
SUBJECT	: ELECTRONIC ANALYSIS AND DESIGN II
DATE	: September 2016
TIME	: 3 Hours

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **FIVE** (5) questions in **EIGHT** (8) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided. **Use pen** to write your answer.
4. Write answer to different question on **a new page**.
5. For all calculations, assume that V_T **= 26 mV**.

THIS QUESTION PAPER CONSISTS OF EIGHT* (8) *PRINTED PAGES INCLUDING THIS COVER PAGE.

QUESTION 1 [20 MARKS]

(a) Consider the Widlar current-source circuit with multiple output shown in **Figure 1**. Assume that V_{BE1}**(on) = 0.7 V**. The circuit parameters are R_1 **= 10 kΩ**, R_{E2} **= 1 kΩ**, and R_{E3} **= 2 kΩ**. Calculate I_{REF}, I_{O2}, and I_{O3}. **[10 marks]**

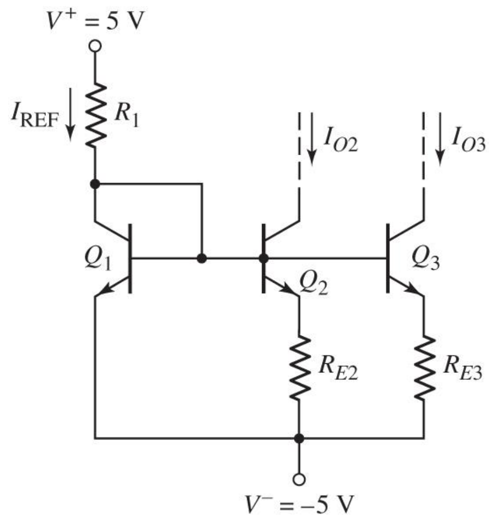


Figure 1

Answers:

Using KVL rule, $I_{REF} = \frac{V^+ - V_{BE1} - V^-}{R_1} = \frac{5-0.7-5}{10k} =$ **0.9300 mA** **[2, 1, 1 marks]**

Solving for Widlar CS,

$I_{O2}R_{E2} = V_T ln\left(\frac{I_{REF}}{I_{O2}}\right)$é **[2 marks]**

$I_{O2}R_{E2} = V_T ln\left(\frac{I_{REF}}{I_{O2}}\right) \rightarrow I_{O2}(1k) = (0.026) ln\left(\frac{0.9300m}{I_{O2}}\right)$

$I_{O2} \cong$ **68 μA** **[2 marks]**

$I_{O3}R_{E3} = V_T ln\left(\frac{I_{REF}}{I_{O3}}\right) \rightarrow I_{O3}(2k) = (0.026) ln\left(\frac{0.9300m}{I_{O3}}\right)$

$I_{O3} \cong$ **40.7 μA** **[2 marks]**

(b) The circuit shown in **Figure 2** has circuit and transistor parameters as $\boldsymbol{V^+} = \mathbf{+3\ V}$, $\boldsymbol{V^-} = \mathbf{-3\ V}$, $\boldsymbol{R_D} = \mathbf{360\ k\Omega}$, $\boldsymbol{V_{TP}} = \mathbf{-0.4\ V}$, $\boldsymbol{K_p} = \mathbf{30\ \mu A/V^2}$, and $\boldsymbol{\lambda} = \mathbf{0}$. The bias current is given as $\boldsymbol{I_Q} = \mathbf{12\ \mu A}$. Calculate **voltage** $\boldsymbol{V_{SD1}}$ for $\boldsymbol{v_1} = \boldsymbol{v_2} = \mathbf{0}$. **[10 marks]**

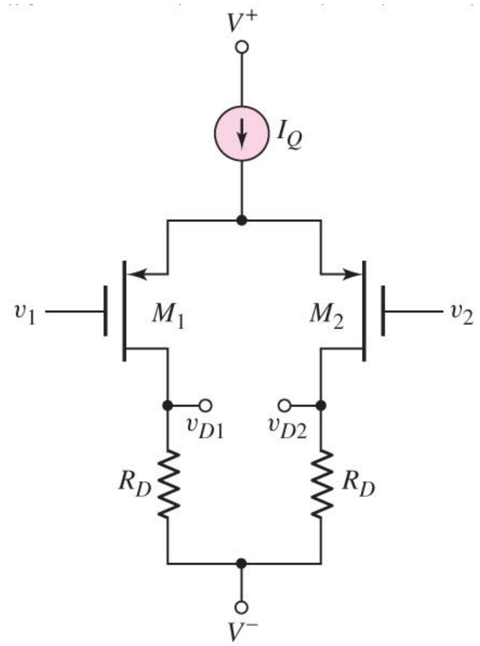


Figure 2

Answers:

As $v_1 = v_2 = 0$,

$I_D = K_p(V_{SG} + V_{TP})^2$ é **[1 mark]**

$I_D = I_Q/2 = 12\mu/2 =$ $\underline{\mathbf{6\ \mu A}}$ **[2 marks]**

$V_{SG} = \sqrt{\frac{I_D}{K_p}} - V_{TP} \rightarrow \sqrt{\frac{6\mu}{30}} + 0.4 =$ $\underline{\mathbf{0.8470\ V}}$ **[2 marks]**

$V_S =$ $\underline{\mathbf{0.8470\ V}}$ **[1 mark]**

$V_D = I_D R_D + V^ï$ = $(6\mu)(360\text{k})$ +(ï 3) = $\underline{\mathbf{-0.8400\ V}}$ **[2 marks]**

So, the Q-point is $V_{SD} = V_S$ ï V_D = 0.8470 ï (ï 0.8400) = $\underline{\mathbf{1.690\ V}}$ **[2 marks]**

QUESTION 2 [20 MARKS]

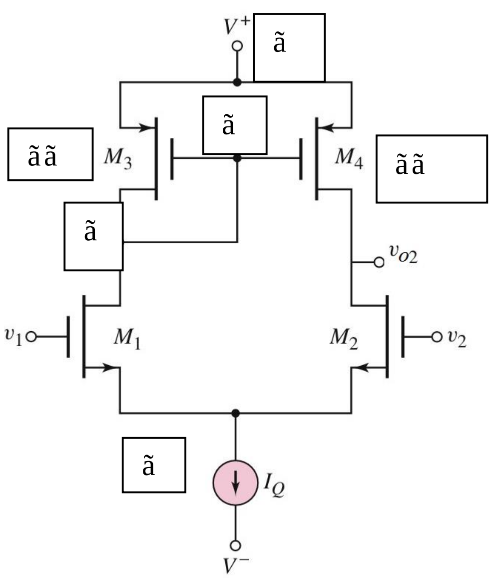
(a) The differential amplifier shown in **Figure 3** is biased by a **0.20 mA** constant current source (i.e. $\boldsymbol{I_Q}$ **= 0.20 mA**). It is to be redesigned to use an active load in order to increase its differential-mode voltage gain ($\boldsymbol{A_d}$). The active load to be used is a **Current Mirror** using **PMOS transistors** to replace the resistors ($\boldsymbol{R_D}$) in the differential amplifier. Let supply voltages be ±5V.
Assume that NMOS devices are available with the following parameters: $\boldsymbol{K_n = 400\ \mu A/V^2}$, $\boldsymbol{V_{TN} = 0.5\ V}$, and $\boldsymbol{\lambda_n = 0.02\ V^{-1}}$
Assume that PMOS devices are available with the following parameters: $\boldsymbol{K_p = 200\ \mu A/V^2}$, $\boldsymbol{V_{TP} = -1\ V}$, and $\boldsymbol{\lambda_p = 0.02\ V^{-1}}$

(i) **Draw the new circuit** incorporating the **active load's full circuit diagram**. Label the circuit correctly and clearly with appropriate symbols and numbering for transistors used in circuit. Leave $\boldsymbol{I_Q}$ symbol as it is in **Figure 3**. **[4 marks]**

(ii) Determine the **differential-mode voltage gain** (A_d) of the circuit. **[6 marks]**

Question 2a

(i)



ã = 0.5 mark

Total **[4]**

(ii) $v_{O2} = g_{m2}\, v_d\, (r_{O2} \parallel r_{O4})$ **[1 mark]**

$\boldsymbol{A_d = v_{O2} / v_d = g_{m2}\, (r_{O2} \parallel r_{O4})}$ **[1 mark]**

$g_{m2} = 2\sqrt{(K_n I_Q/2)} = 2\sqrt{[(400u)(0.2m/2)]} =$ **0.4 mA/V** **[1.5 marks]**

$r_{O2} = 1/(\lambda_n I_Q/2) = 1/[(0.02)(0.2m/2)] =$ **500 kΩ** **[1 mark]**

$r_{O4} = 1/(\lambda_p I_Q/2) = 1/[(0.02)(0.2m/2)] =$ **500 kΩ** **[0.5 mark]**

$r_{O2} \parallel r_{O4}$ = 250 kq **[0.5 mark]**

$A_d = (0.4m)(250k) =$ **100** **[0.5 mark]**

(b) Consider an **idealized class-B** output stage as shown in **Figure 4**. The output stage is to deliver **50 W of average power to the load** at a **maximum output voltage of 11.3 V**. Let the power supply voltages be **±12 volts**. The average current supplied by the supply units can be calculated by using $I_{av} = I_p$ / ´ .

(i) Calculate the **peak output current**, I_p. **[4 marks]**

(ii) Calculate the **total average power supplied** by the supply units **[4 marks]**

(iii) Calculate the **power conversion efficiency** for this circuit. **[2 marks]**

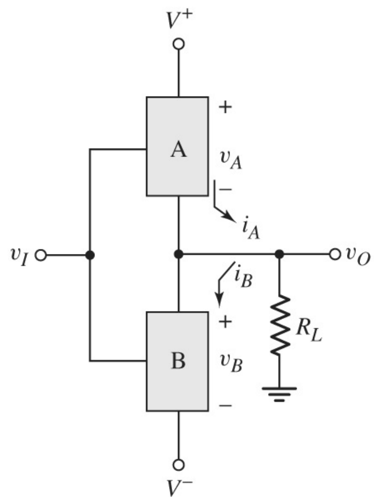


Figure 4

<u>Question 2b</u>

$P_L = V_p I_p / 2 = 50$ **[2]**

$I_p = 2\, P_L / V_p = 2(50)/11.3 = 8.85$ A **[2]**

$I_{ave} = I_p / \pi = 8.85/\pi = 2.817$ A **[2]**

$P_{S(ave)} = 2V_{CC}\, I_{ave} = 2(12)(2.817) = 67.61$ W **[2]**

$\eta = P_L / P_{S(ave)} = (50/67.61)\text{x}100 = 73.95\%$ **[2]**

<u>QUESTION 3 [20 MARKS]</u>

Figure 5 shows a multistage amplifier circuit with transistor parameters of β **= 120** and $V_A = \infty$,
$V_{BE}(on) = V_{EB}(on)$ **= 0.7V.** It is given that V^+ **= 10 V**.

(a) Explain the functions of transistors Q_1, Q_2 and Q_3 in the multistage amplifier. **[5 marks]**

(b) The circuit is such that **zero dc output voltage** is established. Calculate the value of resistors R_{C2} and R_{C3} if currents I_Q **= 0.5 mA** and I_{C3} **= 1 mA**. **[10 marks]**

(c) **Determine** the output resistance, R_O. **[5 marks]**

<u>Question 3(a)</u>

Q1 & Q2 are Darlington Pair, **[1 mark]**
provides large gain **[0.5 mark]** and large input resistance **[0.5 mark]**

Q3 is an emitter follower / common collector amplifier. **[1 mark]**
The gain is unity **[0.5 mark]** and has low output resistance **[0.5 mark]**.
It acts as buffer / provides impedance matching to the load. **[1 mark]**

<u>Question 3(b)</u>

For	Vo = VE3 = 0V:		
	IC3 = (V^+ - Vo) / RC3	eqn 1	[2 marks]
So	RC3 = (V^+ - 0) / IC3 = 10/1mA = 10 / 1m = **<u>10 kΩ</u>**		[2 marks]
	IQ = (V^+ - VC2)/RC2	eqn 2	[2 marks]
	VC2 = VB3, VB3 = VE3 ï VEB3	eqn 3	[2 marks]
	VB3 = VE3 ï VEB3 = 0 ï 0.7V = - 0.7V = VC2		[1 mark]
	IQ = (V^+ - VC2)/RC2 = 10 ï (-0.7) / RC2 = 10.7/RC2		
So	RC2 = 10.7V/ IQ = 10.7 /0.5m = **<u>21.4 kΩ</u>**		[1 mark]

<u>Question 3(c)</u>

$R_O = R_{C3} \parallel \frac{r_{\pi 3}+[R_{C2} \parallel r_{o2}]}{1+\beta}$	[2 marks]
r·3 = бVT/IC3 = 120(26m)/1m = **3.12 kΩ**	[1 mark]
r_{o2} = VA/IC2 = VA/IQ = Đ/0.5m = ∞	[1 mark]
RC2 ‖ r_{o2} = RC2	
Ro = 10k ‖ [3.12k + 21.4k]/(1+120) = **<u>198.6 Ω</u>**	[1 mark]

QUESTION 4 [20 MARKS]

Consider a **standard 741 operational amplifier** (op-amp) circuit as shown in **Figure 6a**. Study **Figure 6a** carefully and observe labelling and values for the resistors in the circuit. Load resistance R_L **= 2 kΩ** is connected to the Output of the 741 op-amp. The op-amp is supplied by **±15 V DC** voltages.

The transistors have β_n **= 200**, β_p **= 50**, **Early voltages** $V_{AN} = V_{AP}$ **= 50 V**, V_{BE}**(on) =** V_{EB}**(on) = 0.6 V**, and the reverse saturation current I_S **= 5x10^{-16} A**.

From **DC analysis**, bias currents for selected transistors are I_{C13A} **= 0.18 mA**, I_{C13B} **= 0.54 mA**, I_{C16} **= 15.8 µA**, I_{C17} **= 0.54 mA**, I_{C20} **= 0.138 mA,** and I_{C22} **= 0.18 mA.**

Figure 6b shows the AC equivalent circuit for the gain stage of the 741 op-amp. **Figure 6c** shows the AC equivalent circuit for the output stage of the 741 op-amp, which is used to calculate R_{i3} in the **Figure 6b**.

With small-signal analysis, the voltage gain for the gain stage (A_{v2}) of the 741 op-amp can be calculated using the following formula:

$$A_{v2} = \frac{v_{o2}}{v_{o1}} = \frac{-\beta_n(1+\beta_n)R_9\left(R_{act2}\|R_{i3}\|R_{o17}\right)}{R_{i2}(R_9 + R_{b17})}$$

Where:

$$R_{act2} = r_{o13B}$$
$$R_{i3} = r_{\pi 22} + (1+\beta_p)[R_{19}\|R_{20}]$$
$$R_{19} \cong R_{13A}$$
$$R_{20} = r_{\pi 20} + (1+\beta_p)R_L$$
$$R_{b17} = r_{\pi 17} + (1+\beta_n)R_8$$

Calculate the voltage gain for the gain stage (A_{v2}) of the 741 op-amp if R_8 **is short circuit**. Neglect base current in your calculations. Apply appropriate assumptions and recall standard formula for parameters which are not given above. **[20 marks]**

Question 4

$$R_{i2} = r_{\pi 16} + (1+\beta_n)R_E^{'}$$ [1]

$$R_E^{'} = R_9 \| [r_{\pi 17} + (1+\beta_n)R_8] = R_9 \| R_{b17}$$ [1]

$$r_{\pi 16} = \frac{\beta_n V_T}{I_{C16}} = \frac{(200)(0.026)}{15.8\varepsilon} = 329\,\text{k}\Omega$$ [1]

$$r_{\pi 17} = \frac{\beta_n V_T}{I_{C17}} = \frac{(200)(0.026)}{0.54\text{m}} = 9.63\,\text{k}\Omega$$ [1]

$$R_{b17} = r_{\pi 17} + (1+\beta_n)R_8 = 9.63\text{k} + (1+200)(0) = 9.63\,\text{k}\Omega$$ [1]

$$\Rightarrow R_E^{'} = 50\text{k} \| 9.63\text{k} = 8.075\,\text{k}\Omega$$ [1]

$$\Rightarrow R_{i2} = 329\text{k} + (201)(8.075\text{k}) = 1.95\,\text{M}\Omega$$ [1]

$$R_{i3} = r_{\pi 22} + (1+\beta_p)[R_{19} \| R_{20}]$$

$$r_{\pi 22} = \frac{\beta_p V_T}{I_{C13A}} = \frac{(50)(0.026)}{0.18\text{m}} = 7.22\,\text{k}\Omega$$ [1, 1]

$$R_{19} \cong R_{13A} = r_{o13A} = \frac{V_A}{I_{C13A}} = \frac{50}{0.18\text{m}} = 278\,\text{k}\Omega$$ [1]

$$r_{\pi 20} = \frac{\beta_p V_T}{I_{C20}} = \frac{(50)(0.026)}{0.138\text{m}} = 9.42\,\text{k}\Omega$$ [1]

$$R_{20} = r_{\pi 20} + (1+\beta_p)R_L$$

$$R_{20} = 9.42\text{k} + (51)(2\text{k}) \cong 111\,\text{k}\Omega$$ [1]

$$\Rightarrow R_{i3} = 7.22\text{k} + (51)[278\text{k} \| 111\text{k}] = 4.05\,\text{M}\Omega$$ [1, 1]

$$R_{o17} = r_{o17}(1 + g_{m17}(r_{\pi 17} \| R_8)); R_8 = 0$$ [1]

$$\Rightarrow R_{o17} = r_{o17} = \frac{V_A}{I_{C17}} = \frac{50}{0.54\text{m}} = 92.6\,\text{k}\Omega$$ [1]

$$R_{act2} = r_{o13B} = \frac{V_A}{I_{C13B}} = \frac{50}{0.54\text{m}} = 92.6\,\text{k}\Omega$$ [1]

$$A_{v2} = \frac{-\beta_n(1+\beta_n)R_9\left(R_{act2} \| R_{i3} \| R_{o17}\right)}{R_{i2}(R_9 + R_{b17})}$$

$$A_{v2} = \frac{-(200)(201)(50\text{k})(92.6\text{k} \| 4.05\text{M} \| 92.6\text{k})}{1.95\text{M}(50\text{k} + 9.63\text{k})}$$ [2]

$$\Rightarrow A_{v2} = -792\ \text{V/V}$$ [1]

QUESTION 5 [20 MARKS]

(a) List down **two characteristics of an ideal op amp**. **[4 marks]**

(b) State **three applications** for ideal op amp. **[3 marks]**

(c) Refer to the **generalised summing amplifier** using ideal op amp in **Figure 7**. The output voltage is given by:

$$v_O = -\frac{R_F}{R_1}v_{I1} - \frac{R_F}{R_2}v_{I2} + \left(1 + \frac{R_F}{R_N}\right)\left[\frac{R_P}{R_A}v_{I3} + \frac{R_P}{R_B}v_{I4}\right]$$

Design the summing amplifier for $v_O = 2v_{I1} - 10v_{I2} + 3v_{I3} - v_{I4}$
Use 500 kq for the largest resistor value. **[13 marks]**

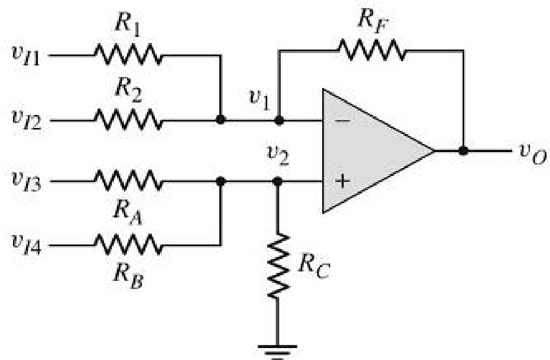


Figure 7

-END OF QUESTION PAPER-

<u>Question 5 (a)</u>

A_{od}: Internal differential gain (open loop gain) is considered to be Ð
(v_2 ï v_1): Differential input voltage is assumed to be 0. If A_{od} Ÿ Ð and v_O is finite, then v_2 å v_1
R_i: Effective input resistance is assumed to be Ð, so input currents i_1 and i_2 are essentially 0
R_o: Effective output resistance is assumed to be 0, so output voltage is independent of any load connected to the output.
CMRR: Common mode rejection ratio = Ð 2 x 2 = **[4 marks]**

<u>Question 5 (b)</u>

Voltage to current converter , current to voltage converter , summing amplifier, instrumentation amplifier, difference amplifier, integrator and differentiator 3 x 1 = **[3 marks]**

<u>Question 5 (c) [13 marks]</u>

Rearrange and using $v_O = -10v_{I1} - v_{I2} + 2v_{I3} + 3v_{I4}$

-RF/R1 = -10 [1]
-RF/R2 = -1 [1]
(1 + RF/RN)(RP/RA) = 2 [1]
(1 + RF/RN)(RP/RB) = 3 [1]

RF = 10R1 = R2
Let **RF = <u>500kΩ</u> = R2** [1], [1]
So **<u>R1 = 50kΩ</u>** [1]

RN = R1 || R2 = 500k || 50k = 45.5k [1.5]
So (1+RF/RN) = (1+500k/45.5k) = 12

Thus 12(RP/RA) = 2 and 12(RP/RB) = 3
So 2RA = 3RB i.e. RA/RB = 3/2
Let **<u>RA = 500kÝ</u>**, then **<u>RB = 333kÝ</u>** [1], [1]

RP = RA || RB || RC
RA || RB = 500k//333k = 199.98k = 200k

From 12(RP/RA) = 2
RP = 2RA/12 = 2(500k)/12 = 83.33k [1.5]

So 83.3k = 200k || RC
So **<u>RC = 142.9kΩ</u>** [1]