COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 1 2016 / 2017

PROGRAMME	: Bachelor of Electrical & Electronics Engineering (Honours) Bachelor of Electrical Power Engineering (Honours)
SUBJECT CODE	: EEEB273
SUBJECT	: ELECTRONIC ANALYSIS AND DESIGN II
DATE	: September 2016
TIME	: 3 Hours

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **FIVE** (5) questions.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided. **Use pen** to write your answer.
4. Write answer to different question on **a new page**.

THIS QUESTION PAPER CONSISTS OF EIGHT (8) PRINTED PAGES INCLUDING THIS COVER PAGE.

QUESTION 1 [20 MARKS]

(a) Consider the Widlar current-source circuit with multiple output shown in **Figure 1**. Assume that V_{BE1}**(on) = 0.7 V**. The circuit parameters are R_1 **= 10 kΩ**, R_{E2} **= 1 kΩ**, and R_{E3} **= 2 kΩ**. Calculate I_{REF}, I_{O2}, and I_{O3}. **[10 marks]**

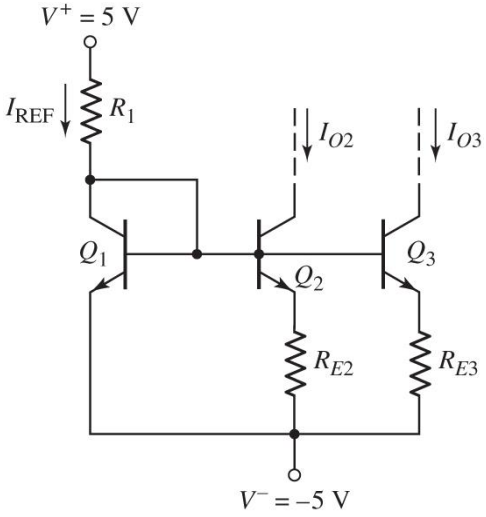

Figure 1

(b) The circuit shown in **Figure 2** has circuit and transistor parameters as V^+ **= +3 V**, V^- **= −3 V**, R_D **= 360 kΩ** , V_{TP} **= −0.4 V**, K_p **= 30 μA/V²**, and **λ = 0**. The bias current is given as I_Q **= 12 μA**. Calculate **voltage** V_{SD1} for $v_1 = v_2 = 0$. **[10 marks]**

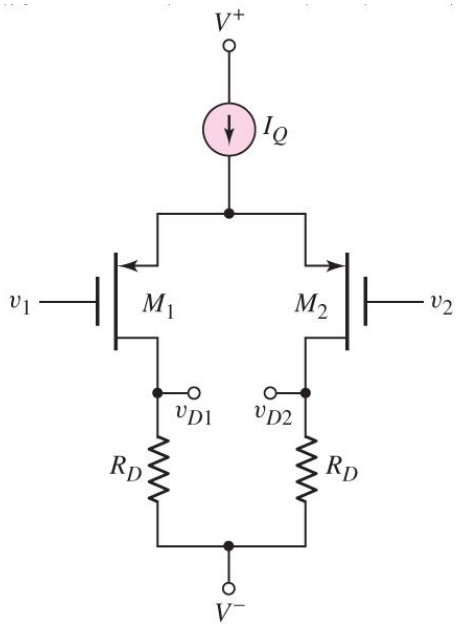

Figure 2

QUESTION 2 [20 MARKS]

(a) The differential amplifier shown in **Figure 3** is biased by a **0.20 mA** constant current source (i.e. I_Q = **0.20 mA**). It is to be redesigned to use an active load in order to increase its differential-mode voltage gain (A_d). The active load to be used is a **2-Transistor Current Source** using **PMOS transistors** to replace the resistors (R_D) in the differential amplifier. Let supply voltages be ±5V.

Assume that NMOS devices are available with the following parameters: K_n = **400 µA/V^2**, V_{TN} = **0.5 V,** and λ_n = **0.02 V^{-1}**

Assume that PMOS devices are available with the following parameters: K_p = **200 µA/V^2**, V_{TP} = **-1 V,** and λ_p = **0.02 V^{-1}**

(i) **Draw the new circuit** incorporating the **active load's full circuit diagram**. Label the circuit correctly and clearly with appropriate symbols and numbering for transistors used in circuit. Leave I_Q symbol as it is in **Figure 3**. **[4 marks]**

(ii) Determine the **differential-mode voltage gain** (A_d) of the circuit. **[6 marks]**

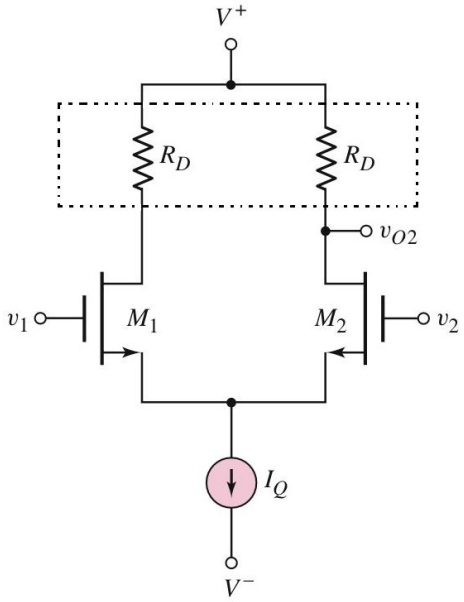

Figure 3

(b) Consider an **idealized class-B** output stage as shown in **Figure 4**. The output stage is to deliver **50 W of average power to the load** at a **maximum output voltage of 11.3 V**. Let the power supply voltages be **±12 volts**. The average current supplied by the supply units can be calculated by using $I_{av} = I_p / \pi$.

(i) Calculate the **peak output current**, I_p. **[4 marks]**

(ii) Calculate the **total average power supplied** by the supply units **[4 marks]**

(iii) Calculate the **power conversion efficiency** for this circuit. **[2 marks]**

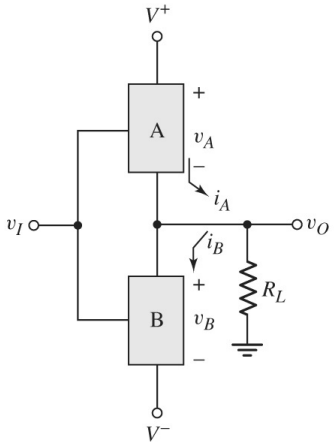

Figure 4

QUESTION 3 [20 MARKS]

Figure 5 shows a multistage amplifier circuit with transistor parameters of β **= 120** and $V_A = \infty$, $V_{BE}(on) = V_{EB}(on) = 0.7V$. It is given that $V^+ = 10$ **V**.

(a) Explain the functions of transistors Q_1, Q_2 and Q_3 in the multistage amplifier. **[5 marks]**

(b) The circuit is such that **zero dc output voltage** is established. Calculate the value of resistors R_{C2} and R_{C3} if currents $I_Q = 0.5$ **mA** and $I_{C3} = 1$ **mA**. **[10 marks]**

(c) **Determine** the output resistance, R_O. **[5 marks]**

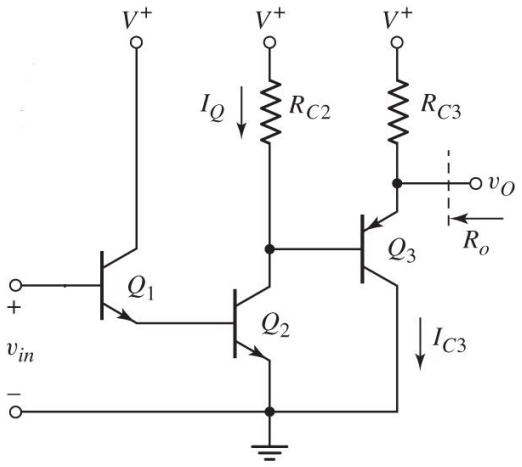

Figure 5

QUESTION 4 [20 MARKS]

Consider a **standard 741 operational amplifier** (op-amp) circuit as shown in **Figure 6a**. Study **Figure 6a** carefully and observe labelling and values for the resistors in the circuit. Load resistance R_L **= 2 kΩ** is connected to the Output of the 741 op-amp. The op-amp is supplied by **±15 V DC** voltages.

The transistors have β_n **= 200**, β_p **= 50**, **Early voltages** $V_{AN} = V_{AP}$ **= 50 V**, V_{BE}**(on) =** V_{EB}**(on) = 0.6 V**, and the reverse saturation current I_S **= 5x10^{-16} A**.

From **DC analysis**, bias currents for selected transistors are I_{C13A} **= 0.18 mA**, I_{C13B} **= 0.54 mA**, I_{C16} **= 15.8 µA,** I_{C17} **= 0.54 mA,** I_{C20} **= 0.138 mA,** and I_{C22} **= 0.18 mA.**

Figure 6b shows the AC equivalent circuit for the gain stage of the 741 op-amp. **Figure 6c** shows the AC equivalent circuit for the output stage of the 741 op-amp, which is used to calculate R_{i3} in the **Figure 6b**.

With small-signal analysis, the voltage gain for the gain stage (A_{v2}) of the 741 op-amp can be calculated using the following formula:

$$A_{v2} = \frac{v_{o2}}{v_{o1}} = \frac{-\beta_n(1+\beta_n)R_9\left(R_{act2} \| R_{i3} \| R_{o17}\right)}{R_{i2}(R_9 + R_{b17})}$$

Where:

$$R_{act2} = r_{o13B}$$

$$R_{i3} = r_{\pi 22} + (1+\beta_p)\left[R_{19} \| R_{20}\right]$$

$$R_{19} \cong R_{13A}$$

$$R_{20} = r_{\pi 20} + (1+\beta_p)R_L$$

$$R_{b17} = r_{\pi 17} + (1+\beta_n)R_8$$

Calculate the voltage gain for the gain stage (A_{v2}) of the 741 op-amp if R_8 **is short circuit**. Neglect base current in your calculations. Apply appropriate assumptions and recall standard formula for parameters which are not given above. **[20 marks]**

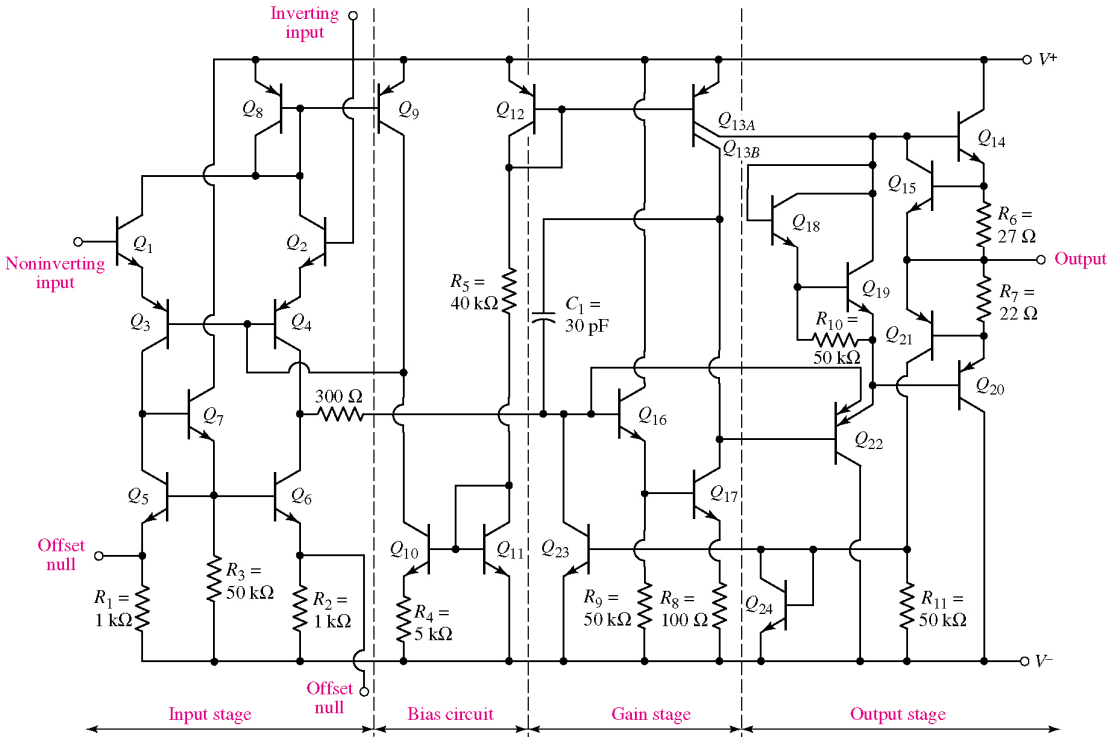

Figure 6a

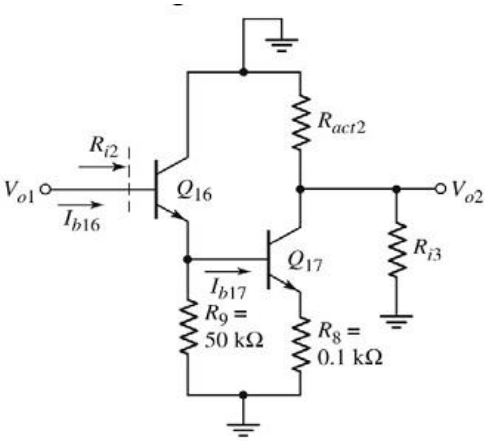

Figure 6b

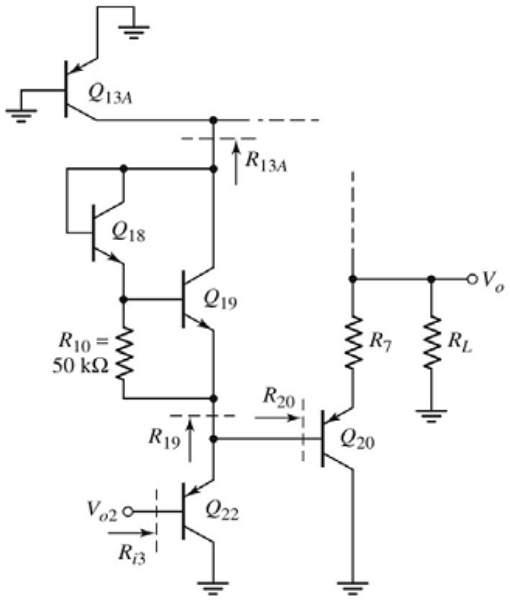

Figure 6c

QUESTION 5 [20 MARKS]

(a) Briefly describe **two characteristics of an ideal op amp**. **[4 marks]**

(b) State **three applications** for the ideal op amp. **[3 marks]**

(c) Refer to the **generalised summing amplifier** using ideal op amp in **Figure 7**. The output voltage is given by:

$$v_O = -\frac{R_F}{R_1}v_{I1} - \frac{R_F}{R_2}v_{I2} + \left(1+\frac{R_F}{R_N}\right)\left[\frac{R_P}{R_A}v_{I3} + \frac{R_P}{R_B}v_{I4}\right]$$

Where $R_N = R_1 \,//\, R_2$ and $R_P = R_A \,//\, R_B \,//\, R_C$

Design the summing amplifier for $v_O = 2v_{I1} - 10v_{I2} + 3v_{I3} - v_{I4}$

Use **500kΩ for the largest resistor** value. Design the circuit such that the **input impedance seen by each source** is the largest value possible. **[13 marks]**

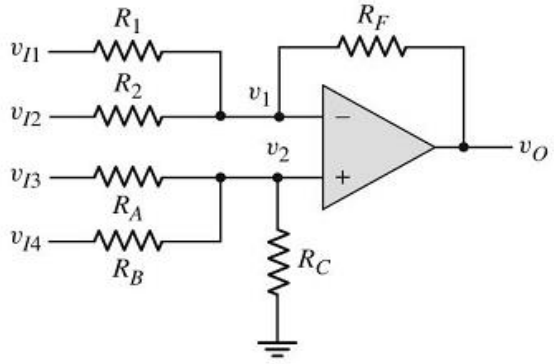

Figure 7

-END OF QUESTION PAPER-

APPENDIX:

A) BASIC FORMULA FOR TRANSISTOR

BJT

$i_C = I_S e^{v_{BE}/V_T}$; NPN

$i_C = I_S e^{v_{EB}/V_T}$; PNP

$i_C = \beta i_B = \alpha i_E$

$i_E = i_B + i_C$

$\alpha = \dfrac{\beta}{\beta + 1}$

; Small signal

$\beta = g_m r_\pi$

$g_m = \dfrac{I_{CQ}}{V_T}$

$r_\pi = \dfrac{\beta V_T}{I_{CQ}}$

$r_o = \dfrac{V_A}{I_{CQ}}$

$V_T = 26\,\text{mV}$

MOSFET

; N – MOSFET

$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$

$i_D = K_n[v_{GS} - V_{TN}]^2$

$K_n = \dfrac{\mu_n C_{ox} W}{2L} = \dfrac{k_n'}{2} \cdot \dfrac{W}{L}$

; P – MOSFET

$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$

$i_D = K_p[v_{SG} + V_{TP}]^2$

$K_p = \dfrac{\mu_p C_{ox} W}{2L} = \dfrac{k_p'}{2} \cdot \dfrac{W}{L}$

; Small signal

$g_m = 2\sqrt{K_? I_{DQ}}$

$r_o \cong \dfrac{1}{\lambda I_{DQ}}$

B) HYBRID-´ EQUIVALENT CIRCUITS