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UNIVERSITI TENAGA NASIONAL

College of Engineering

Department of Electronics and Communication Engineering

Test 2

SEMESTER 1, ACADEMIC YEAR 2016/2017

(SOLUTION)

Subject Code	:	**EEEB273**
Course Title	:	**Electronics Analysis & Design II**
Date	:	**19 August 2016**
Time Allowed	:	**1½ hours**

Instructions to the candidates:

1. Write your Name, Student ID number, and Section number. Indicate your Lecturer.
2. Write all your answers **using pen**. **DO NOT USE PENCIL** except for the diagram.
3. **ANSWER ALL QUESTIONS.**
4. **WRITE YOUR ANSWER ON THIS QUESTION PAPER.**
5. For all calculations, use V_T **= 26 mV** when necessary.

NOTE: DO NOT OPEN THE QUESTION PAPER UNTIL INSTRUCTED TO DO SO.

☺ **GOOD LUCK!** ☺

Question No.	1	2	3	Total
Marks				

Question 1 **[30 marks]**

A differential amplifier is shown in **Figure 1.** The circuit parameters are given as V^+ **= 10 V**, V^- **= −10 V**, and I_Q **= 1.5 mA**. The **NMOS** transistor parameters are V_{TN} **= 0.4 V**, k'_n **= 100** μ**A/V²**, λ_n = **0.025 V⁻¹**, $(W/L)_{1,2}$ **= 5** and $(W/L)_8$ **= 20**. The **PMOS** transistor parameters are V_{TP} **= −0.4 V**, k'_p **= 40** μ**A/V²**, λ_p = **0.04 V⁻¹** and $(W/L)_{3,4}$ **= 10**.

i. Determine the **range of the output voltage,** v_o**,** for the differential amplifier. [15 marks]

ii. Define **common mode rejection ratio**, **CMRR**. How can the circuit in **Figure 1** be **redesigned** to **improve** its CMRR? Explain what will happen to the **range of the output voltage** calculated in part i) if the circuit is redesigned. [5 marks]

iii. Find the **output resistance**, R_o, of the differential amplifier. [10 marks]

Answer for Question 1(i) – 15 marks

$V_o(\max) = V^+ - V_{SD4}(sat)$ [2]

$I_{D1} = I_Q / 2 = I_{D2} = I_{D3} = I_{D4} = 1.5mA/2 = 0.75mA$

$$V_{SG4} \Rightarrow I_{D4} = \left(\frac{k'_p}{2}\right)\left(\frac{W}{L}\right)_4 \left(V_{SG4} + V_{TP}\right)^2$$

$$0.75m = \left(\frac{40\mu}{2}\right)(10)\left(V_{SG4} + (-0.4)\right)^2$$

$\rightarrow V_{SG4} = 2.336V$ [2]

$V_{SD4}(sat) = V_{SG4} + V_{TP} = 2.336 + (-0.4) = 1.937V$ [1]

$V_o(\max) = 10 - (1.937) = 8.06V$ [1]

$V_o(\min) = V_{DS2}(sat) + V_{DS8}(sat) + V^-$ [2]

$$V_{GS2} \Rightarrow I_{D2} = \left(\frac{k'_n}{2}\right)\left(\frac{W}{L}\right)_2 \left(V_{GS2} - V_{TN}\right)^2$$

$$0.75m = \left(\frac{100\mu}{2}\right)(5)\left(V_{GS2} - 0.4\right)^2$$

$\rightarrow V_{GS1} = 2.132V$ [2]

$V_{DS2}(sat) = V_{GS2} - V_{TN} = 2.132 - 0.4 = 1.732V$ [1]

$$V_{GS8} \Rightarrow I_{D8} = \left(\frac{k'_n}{2}\right)\left(\frac{W}{L}\right)_8 \left(V_{GS8} - V_{TN}\right)^2$$

$$0.75m = \left(\frac{100\mu}{2}\right)(20)\left(V_{GS8} - 0.4\right)^2$$

$\rightarrow V_{GS8} = 1.625V$ [2]

$V_{DS8}(sat) = V_{GS8} - V_{TN} = 1.625 - 0.4 = 1.225V$ [1]

$V_o(\min) = 1.732 + 1.225 + (-10) = -7.04V$ [1]

Answer for Question 1(ii) – 5 marks

- Common mode rejection ratio, CMRR: Ability of Differential amplifier circuit to reject common-mode input signal. Ideally CMRR is infinity. [1.5 marks]

$$CMRR = \left| \frac{A_d}{|A_{cm}|} \right|$$ [1 mark]

- For Figure 1, CMRR is improved by lowering its common mode gain Acm [0.5 marks]
- Acm is decreased by using a current source circuit with higher output resistance, for example Cascode, Wilson or Widlar current source. [1 mark]
- Using Cascode, Wilson or Widlar as biasing circuit will increase the voltage across the current source, therefore the value of VO(min) calculated in part i) will be increased, i.e. the output voltage range is reduced. [1 mark]

Answer for Question 1(iii) – 10 marks

$R_o = (r_{o2} \| r_{o4})$ [2]

$$r_{o2} = \frac{1}{\lambda_n I_{D2}} = \frac{1}{(0.025)(0.75m)} = 53.33k\Omega$$ [3]

$$r_{o4} = \frac{1}{\lambda_p I_{D4}} = \frac{1}{(0.04)(0.75m)} = 33.33k\Omega$$ [3]

$R_o = (r_{o2} \| r_{o4}) = (53.33k \| 33.33k) = 20.51k\Omega$ [2]

Question 2 **[30 marks]**

(a) The circuit in **Figure 2** has a pair of npn bipolar transistors as input devices and three-pnp-bipolar- transistor circuit connected as an active load. The differential amplifier circuit is biased with a constant current source $\boldsymbol{I_Q = 0.2\ mA}$ that has and output resistance $\boldsymbol{R_{OCS} = 50\ M\Omega}$. The transistor parameters are: $\boldsymbol{\beta = 100}$, $\boldsymbol{V_{A1} = V_{A2} = 100\ V}$, $\boldsymbol{V_{A3} = V_{A4} = 60\ V}$, and $\boldsymbol{V_{A5}} = \infty$.

i. **Calculate the open-circuit** differential-mode voltage gain $\boldsymbol{A_d}$. [12 marks]

ii. **Determine** $\boldsymbol{R_L}$ such that the differential-mode voltage gain is reduced to **80%** of its open-circuit value. [8 marks]

Answer for Question 2(a)

(i) $I_{C2} = \beta I_E/(1+\beta)$ [1]
$= \beta I_Q/[2(1+\beta)]$ [1]
$= (100)(0.2m)/2(101) = 0.0990$ mA [1]

$r_{O2} = V_{A2}/I_{C2} = 100/0.0990m = 1.01$ MΩ [2]
$r_{O4} = V_{A4}/I_{C4} = 60/0.0990$ m $= 606.1$ kΩ [2]

$R_O = r_{O2} \| r_{O4} = 1.01M \| 606.1k = 378.8$ kΩ [2]

$g_m = I_{C2}/V_T = (0.0990m)/(0.026) = 3.808$ mA/V [2]

$A_v = g_m(R_O) = (3.808\ m)(\ 378.8\ k) = 1442$ [1]

(ii) New $R_{ON} = R_O \| R_L$ [2]
$= R_O R_L/(\ R_O+R_L)$
$A_{vN} = (80\%)(1442) = 1153.6$ [1]

Thus $1153.6 = g_m(R_{ON}) = [g_m R_O R_L]/(\ R_O+R_L)$ [2]
$1153.6(R_O+R_L) = 1442R_L$
$R_L = (1153.6\ R_O)/(1442-1153.6)$
$= (1153.6 \times 378.8k)/(288.4) = 1515.2$ kΩ [3]

OR (can be accepted)

(i) $I_{C2} = I_Q/2 = 0.2m/2 = 0.1$ mA [3]

$r_{O2} = V_{A2}/I_{C2} = 100/0.1m = 1$ MΩ [2]
$r_{O4} = V_{A4}/I_{C4} = 60/0.1m = 600$ kΩ [2]

$R_O = r_{O2} \| r_{O4} = 1M \| 600k = 375$ kΩ [2]

$g_m = I_{C2}/V_T = (0.1m)/(0.026) = 3.846$ mA/V [2]

$A_v = g_m(R_O) = (3.846m)(375k) = 1442$ [1]

(ii) New R_{ON} $= R_O \| R_L$ [2]
$= R_O R_L/(R_O+R_L)$
A_{vN} $= (80\%)(1442) = 1153.6$ [1]

Thus $1153.6 = g_m(R_{ON}) = [g_m R_O R_L]/(R_O+R_L)$ [2]
$1153.6(R_O+R_L) = 1442R_L$
$R_L = (1153.6\ R_O)/(1442-1153.6)$
$= (1153.6 \times 378.8k)/(288.4) = 1515.2\ k\Omega$ [3]

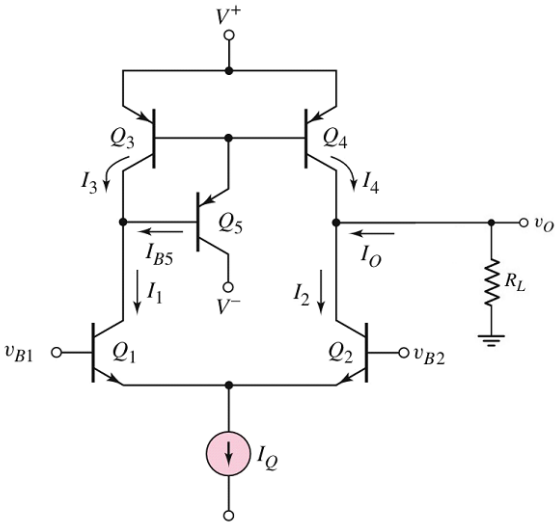


Figure 2

(b) Refer to **Figure 3**. It is given that $\boldsymbol{I_Q = I_{R4} = I_{R6} = 0.4\ mA}$, and $\boldsymbol{I_{R7} = 2\ mA}$. Neglect base currents and assume $\boldsymbol{V_{BE}(on) = 0.7\ V}$ for all transistors except Q_8 and Q_9 in the Widlar circuit. From small-signal analysis, $\boldsymbol{R_{i2} = 1.3M\ \Omega}$. **Calculate the overall gain of the circuit, $\boldsymbol{A_d = v_O/v_d}$.** State any assumptions. Assume $\boldsymbol{\beta = 100}$ and $\boldsymbol{V_A = \infty}$. It is given that the gain of the Darlington Pair can be calculated using:

$$A_{V2} = \left(\frac{I_{R4}}{2V_T}\right)\left(R_5 \parallel R_{i3}\right)$$

[10 marks]

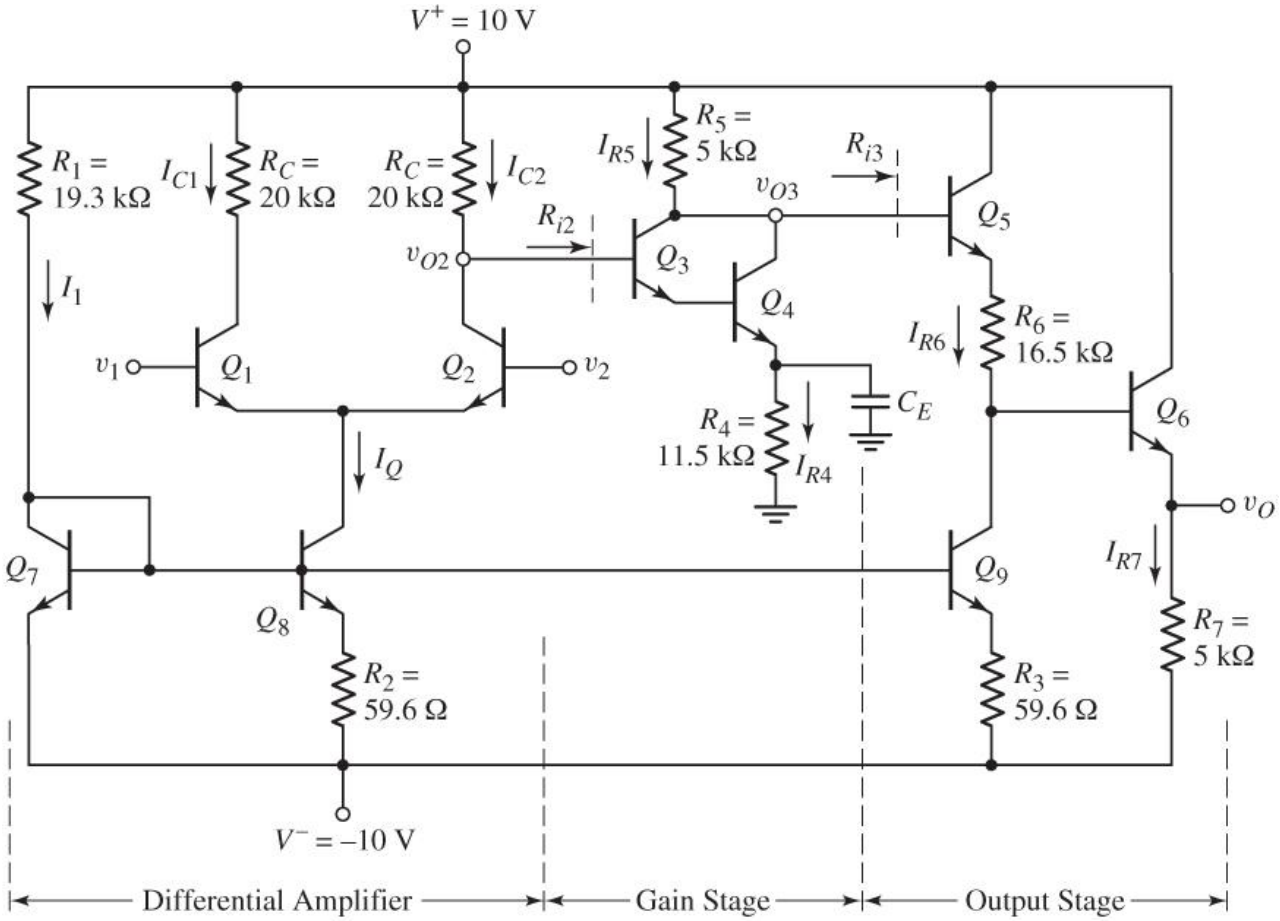


Figure 3

Answer for Question 2(b)

Ad = vo/vd = Ad1 x Av2 x Av3 [1 mark]

Ad1 = ½ gm1(Rc||ro2||Ri2) [1 mark]

Ic1 = IQ/2 = 0.4m/2 = 0.2mA
gm1 = Ic1/VT = 0.2m/26m = 7.692 mA/V [1/2 marks]

ro2 infinity

→ Ad1 = ½ (7.692 m)(20k||1.3M) = ½ (7.692 m)(19.7k)
= 75.75 V/V [1/2 marks]

Av2 = (IR4/2VT)(R5||Ri3)

Ri3 = rπ5 + (1+β)RE' [1 mark]
RE' = R6 + (Rb6||Rc9) = R6 + Rb6 since Rc9 infinity [1 mark]
Rb6 = rπ6 + (1+β)R7 [1 mark]

rπ6= βVT/Ic6 = (100)(26m)/2m = 1.3kΩ [1/2 marks]
rπ5= βVT/Ic5 = (100)(26m)/0.4m = 6.5kΩ [1/2 marks]

Rb6 = 1.3k + (1+100)(5k) = 506.3kΩ [1/2 marks]
RE' = R6 + Rb6 = 16.5k + 506.3k = 522.8kΩ
Ri3 = rπ5 + (1+β)RE' = 6.5k + (1+100)(522.8k) = 52.81 MΩ [1/2 marks]

→ Av2 = (0.4m/2x26m)(5k||52.81M) =38.46 V/V [1/2 marks]

Av3 = 1 V/V [1 mark]

→ Ad = vo/vd = 75.75 x 38.46 x 1 = 2913 V/V [1/2 marks]

Question 3 [40 marks]

(a) **Compare and contrast** the output stage classes (namely **class-A**, **class-B**, and **class-AB**). You might consider the **keywords**: percent (%) of time the output transistors are conducting; the power conversion efficiency; quiescent bias current; power dissipation. [15 marks]

Answer for Question 3(a)

	percent (%) of time the output transistors are conducting	power conversion efficiency	quiescent bias current
Class-A	***entire cycle*** *of the input signal* **[2 marks]**	$\eta(\max) = \frac{1}{4} \Rightarrow 25\%$ **[2 marks]** rarely used in high-power applications	Output transistor is ***biased*** *at a quiescent current* I_Q **[1 mark]**
Class-B	***Exactly one-half*** *of each sine-wave input cycle* **[2 marks]**	$\eta(\max) = \frac{\pi}{4} \Rightarrow 78.5\%$ **[2 marks]**	Zero quiescent current **[1 mark]**
Class-AB	***slightly more than half*** a cycle of the input *signal* **[2 marks]**	Power conversion efficiency in between class-A and class-B **[2 marks]**	**biased** *at a small quiescent current* I_Q **[1 mark]**

(b) Consider the emitter follower of the **class-A** output stage shown in **Figure 4**. The circuit parameters are: V^+ **= 7.5 V,** V^- **= -7.5 V**, and R_L **= 2 kΩ**. Assume all transistors are matched with $V_{BE}(on)$ **= 0.7 V** and $V_{CE}(sat)$ **= 0.5 V**. Neglect base currents in your calculations.

i) Find the value of R_1 that gives the maximum possible output range. [10 marks]

ii) **Sketch the output current waveform (i_{C1})** for one complete input cycle. [5 marks]

iii) **Calculate the power conversion efficiency**, η, for this output stage. [10 marks]

Answer for Question 3(b)

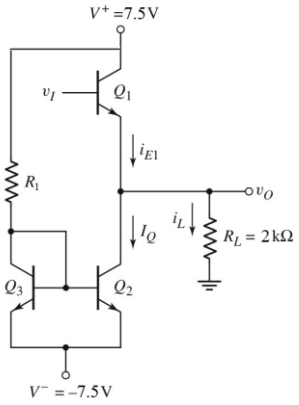


Figure 4

(i)

$$-i_{L\max} = -v_{O\max} / R_L \qquad [1]$$

$$-v_{O\max} = V^- + V_{CE1(sat)} = -7.5 + 0.5 = -7V \qquad [2]$$

$$-i_{L\max} = \frac{7}{2k} = 3.5mA = |I| \qquad [2]$$

$$R = \frac{V^+ - V_{BE2} - V^-}{I} = \frac{7.5 - 0.7 - (-7.5)}{3.5m} = 4.086k\Omega \qquad [2]$$

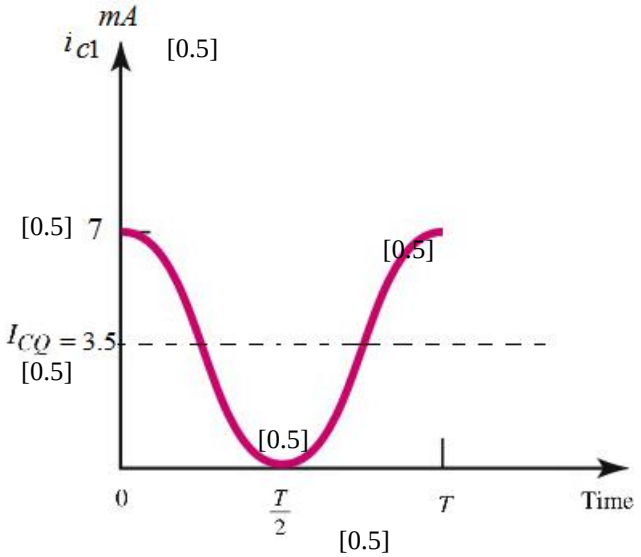
(ii)

$$v_{o(\max)} = V^+ - V_{CE2(sat)} = 7.5 - 0.5 = 7V \qquad [1.5]$$

$$i_{L(\max)} = v_{o(\max)} / R_L = 3.5mA \qquad [1.5]$$

$$i_{C1\min} = I + i_{L\min} = 3.5m + (-3.5m) = 0 \qquad [1]$$

$$i_{C1\max} = I + i_{L\max} = 3.5m + 3.5m = 7mA \qquad [1]$$



(iii)

$$\overline{P}_L = \frac{1}{2}\frac{V_p^2}{R_L} = \frac{1}{2}\frac{7^2}{2k} = 12.25mW \qquad [1.5]$$

$$\overline{P}_S = \overline{P}_S^+ + \overline{P}_S^- = (V^+ - V^-)(I) + (0 - V^-) \cong 3(7.5)(3.5m) = 78.75mW \qquad [2]$$

$$\eta = \frac{\overline{P_S}}{\overline{P_L}} = \frac{12.25}{78.75} = 0.1556 \qquad [1.5]$$