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Student ID Number:
Section:
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UNIVERSITI TENAGA NASIONAL

College of Engineering

Department of Electronics and Communication Engineering

Test 2

SEMESTER 1, ACADEMIC YEAR 2016/2017

Subject Code	:	**EEEB273**
Course Title	:	**Electronics Analysis & Design II**
Date	:	**19 August 2016**
Time Allowed	:	**1½ hours**

Instructions to the candidates:

1. Write your Name, Student ID number, and Section number. Indicate your Lecturer.
2. Write all your answers **using pen**. **DO NOT USE PENCIL** except for the diagram.
3. **ANSWER ALL QUESTIONS.**
4. **WRITE YOUR ANSWER ON THIS QUESTION PAPER.**
5. For all calculations, use V_T **= 26 mV** when necessary.

NOTE: DO NOT OPEN THE QUESTION PAPER UNTIL INSTRUCTED TO DO SO.

☺ **GOOD LUCK!** ☺

Question No.	1	2	3	Total
Marks				

BASIC FORMULA

BJT

$$i_C = I_S e^{v_{BE}/V_T} \text{; npn}$$

$$i_C = I_S e^{v_{EB}/V_T} \text{; pnp}$$

$$i_C = \alpha i_E = \beta i_B$$

$$i_E = i_B + i_C$$

$$\alpha = \frac{\beta}{\beta + 1}$$

;Small signal

$$\beta = g_m r_\pi$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

MOSFET

;N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n [v_{GS} - V_{TN}]^2$$

$$K_n = \frac{k_n'}{2} \cdot \frac{W}{L}$$

;P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p [v_{SG} + V_{TP}]^2$$

$$K_p = \frac{k_p'}{2} \cdot \frac{W}{L}$$

;Small signal

$$g_m = 2\sqrt{K_? I_{DQ}}$$

$$r_o \cong \frac{1}{\lambda I_{DQ}}$$

Question 1 **[30 marks]**

A differential amplifier is shown in **Figure 1.** The circuit parameters are given as V^+ **= 10 V**, V^- **= −10 V**, and I_Q **= 1.5 mA**. The **NMOS** transistor parameters are V_{TN} **= 0.4 V**, k'_n **= 100** μ**A/V**^{2}, λ_n = **0.025 V**$^{-1}$, $(W/L)_{1,2}$ **= 5** and $(W/L)_8$ **= 20**. The **PMOS** transistor parameters are V_{TP} **= −0.4 V**, k'_p **= 40** μ**A/V**^{2}, λ_p = **0.04 V**$^{-1}$ and $(W/L)_{3,4}$ **= 10**.

i. Determine the **range of the output voltage,** v_o**,** for the differential amplifier. [15 marks]

ii. Define **common mode rejection ratio**, **CMRR**. How can the circuit in **Figure 1** be **redesigned** to **improve** its CMRR? Explain what will happen to the **range of the output voltage** calculated in part i) if the circuit is redesigned. [5 marks]

iii. Find the **output resistance**, R_o, of the differential amplifier. [10 marks]

Answer for Question 1

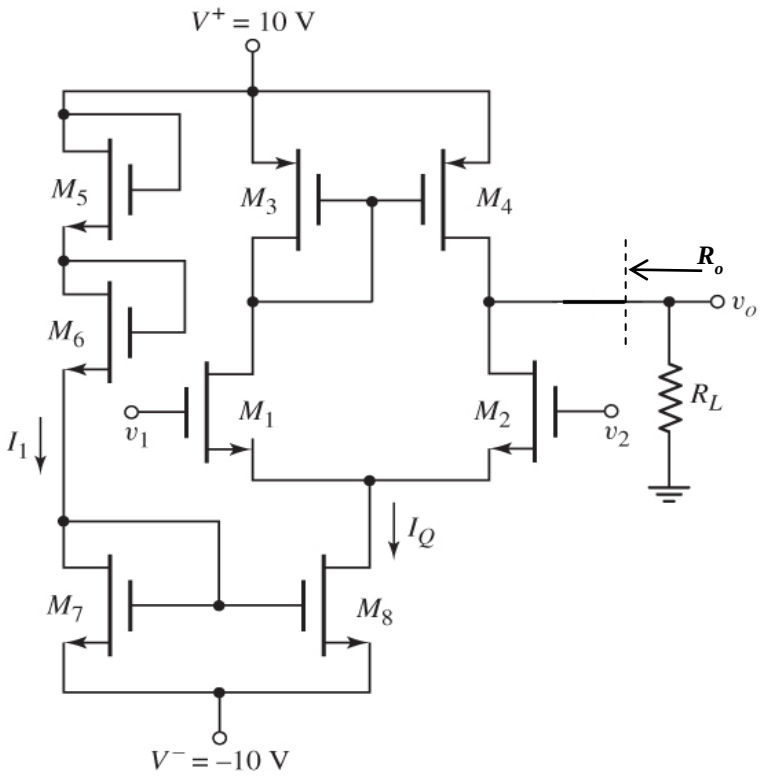

Figure 1

Answer for Question 1 (continue)

Question 2 **[30 marks]**

(a) The circuit in **Figure 2** has a pair of npn bipolar transistors as input devices and three-pnp-bipolar- transistor circuit connected as an active load. The differential amplifier circuit is biased with a constant current source $\boldsymbol{I_Q = 0.2\ mA}$ that has and output resistance $\boldsymbol{R_{OCS} = 50\ M\Omega}$. The transistor parameters are: $\boldsymbol{\beta = 100}$, $\boldsymbol{V_{A1} = V_{A2} = 100\ V}$, $\boldsymbol{V_{A3} = V_{A4} = 60\ V}$, and $\boldsymbol{V_{A5} = \infty}$.

i. **Calculate the open-circuit** differential-mode voltage gain $\boldsymbol{A_d}$. [12 marks]

ii. **Determine** $\boldsymbol{R_L}$ such that the differential-mode voltage gain is reduced to **80%** of its open-circuit value. [8 marks]

Answer for Question 2(a)

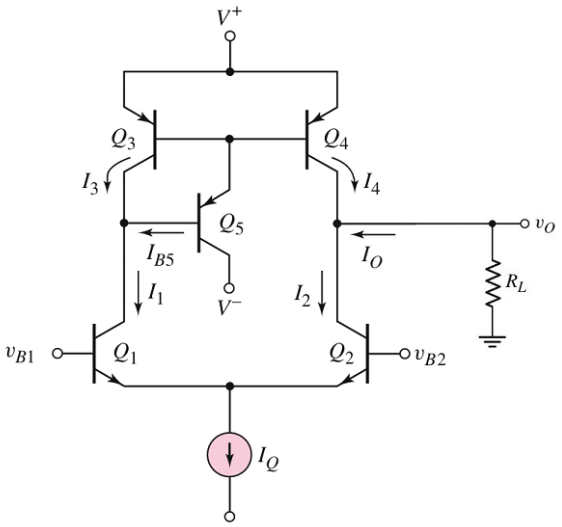

Figure 2

(b) Refer to **Figure 3**. It is given that $\boldsymbol{I_Q = I_{R4} = I_{R6} = 0.4\ mA}$, and $\boldsymbol{I_{R7} = 2\ mA}$. Neglect base currents and assume $\boldsymbol{V_{BE}(on) = 0.7\ V}$ for all transistors except Q_8 and Q_9 in the Widlar circuit. From small-signal analysis, $\boldsymbol{R_{i2} = 1.3M\ \Omega}$. **Calculate the overall gain of the circuit, $A_d = v_O/v_d$.** State any assumptions. Assume $\boldsymbol{\beta = 100}$ and $\boldsymbol{V_A = \infty}$. It is given that the gain of the Darlington Pair can be calculated using:

$$A_{V2} = \left(\frac{I_{R4}}{2V_T}\right)\left(R_5 \parallel R_{i3}\right)$$

[10 marks]

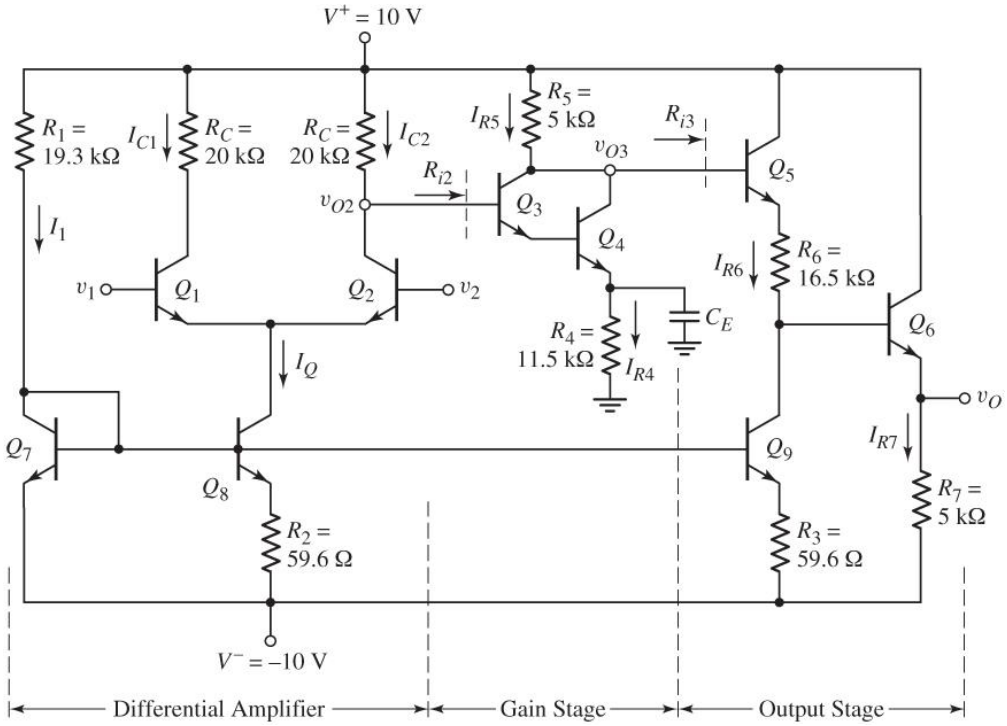

Figure 3

Answer for Question 2(b)

Question 3 **[40 marks]**

(a) **Compare and contrast** the output stage classes (namely **class-A**, **class-B**, and **class-AB**). You might consider the **keywords**: percent (%) of time the output transistors are conducting; the power conversion efficiency; quiescent bias current; power dissipation. [15 marks]

Answer for Question 3(a)

(b) Consider the emitter follower of the **class-A** output stage shown in **Figure 4**. The circuit parameters are: V^+ **= 7.5 V,** V^- **= -7.5 V**, and R_L **= 2 kΩ**. Assume all transistors are matched with $V_{BE}(on)$ **= 0.7 V** and $V_{CE}(sat)$ **= 0.5 V**. Neglect base currents in your calculations.

i) Find the value of R_1 that gives the maximum possible output range. [10 marks]

ii) **Sketch the output current waveform (**i_{C1}**)** for one complete input cycle. [5 marks]

iii) **Calculate the power conversion efficiency,** η, for this output stage. [10 marks]

Answer for Question 3(b)

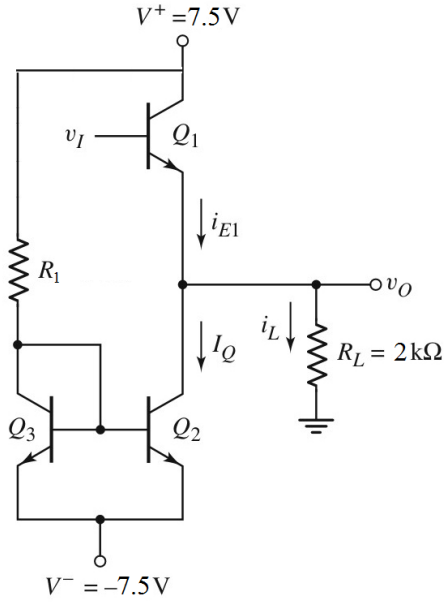

Figure 4