COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 2 2016 / 2017

PROGRAMME	: **Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	: **EEEB273**
SUBJECT	: **ELECTRONIC ANALYSIS AND DESIGN II**
DATE	: **January/February 2017**
TIME	: **3 hours**

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **FIVE (5)** questions in **NINE (9)** pages.
2. Answer **ALL** questions.
3. Write **ALL** answers in the answer booklet provided. **Use pen** to write your answer.
4. Write answer to different question on **a new page**.
5. **Show clearly all calculations, complete with proper Unit for every parameter.**

THIS QUESTION PAPER CONSISTS OF NINE* (9) *PRINTED PAGES INCLUDING THIS COVER PAGE.

Question 1 [20 marks]

Consider a BJT differential amplifier with the circuit shown in **Figure 1**. The transistor parameters are $\boldsymbol{\beta = 100}$, $\boldsymbol{V_A = \infty}$ **for** $\boldsymbol{Q_1}$ **and** $\boldsymbol{Q_2}$, and $\boldsymbol{V_A = 100}$ **V for** $\boldsymbol{Q_3}$ **and** $\boldsymbol{Q_4}$.

At input voltages of $\boldsymbol{v_1 = v_2 = 0, I_{C4} = 200}$ **μA**, and $\boldsymbol{I_1 = 0.5}$ **mA**, output voltage is $\boldsymbol{v_{O2} = 8}$ **V**.

Neglect the base currents.

(a) **Find** the output resistance ($\boldsymbol{R_O}$) of the current source. [8 marks]

(b) **Determine** the value of $\boldsymbol{R_C}$. [4 marks]

(c) **Find** the differential-mode input resistance, $\boldsymbol{R_{id}}$. [4 marks]

(d) **Find** the common-mode input resistance, $\boldsymbol{R_{icm}}$. [4 marks]

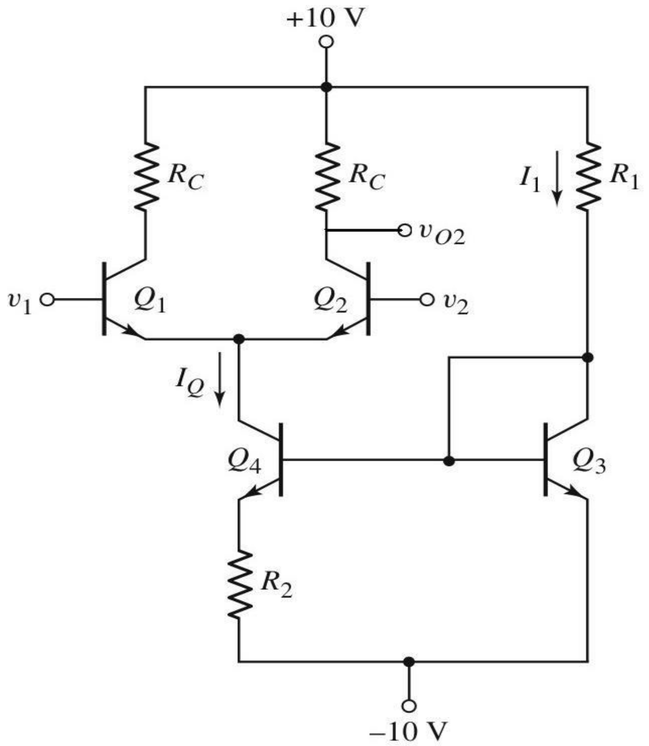


Figure 1

Question 2 [20 marks]

Figure 2 shows a BJT differential amplifier with a bias current, $\boldsymbol{I_Q}$ **= 0.2 mA**. The differential amplifier increases its gain by applying a BJT cascode current source comprising **pnp** transistors as an active load. The circuit parameters are $\boldsymbol{V^+}$ **= 10 V** and $\boldsymbol{V^-}$ **= −10 V**. The transistor parameters are given as $\boldsymbol{\beta}$ **= 80,** $\boldsymbol{V_{BE}}$**(on) = 0.7 V,** $\boldsymbol{V_{AN}}$ **= 100 V, and** $\boldsymbol{V_{AP}}$ **= 120 V.**

(a) **Draw** the differential amplifier circuit with the added cascode current source as the active load. [3 marks]

(b) **Determine** the output resistance, $\boldsymbol{R_{OAL}}$, of the cascode current source. Later, **compare** the output difference for the circuit above should the active load is replaced by a two-transistor current source. [7 marks]

(c) **Find** the differential-mode voltage gain, $\boldsymbol{A_d}$, of the circuit. [6 marks]

(d) **Calculate** the output voltage of the circuit with a $\boldsymbol{v_d}$ **= 10 sin(ω*t*) mV**. [4 marks]

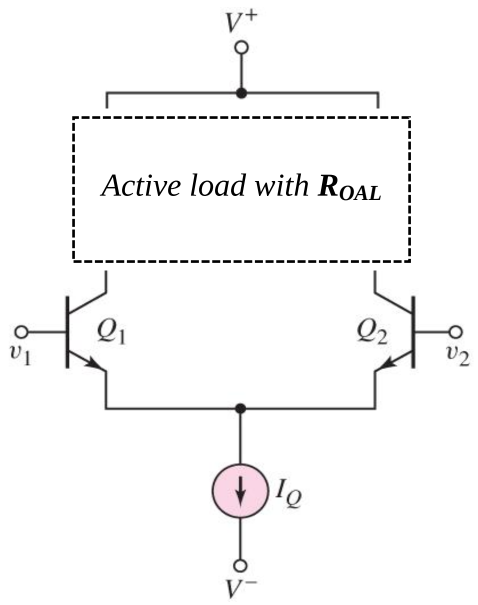


Figure 2

Question 3 [20 marks]

(a) A **class-AB** output stage with BJTs is shown in **Figure 3**. **Reverse saturation current** for every transistor is I_S **= 2×10^{-15} A**. Assume $+V_{CC}$ **= +6 V** and $-V_{CC}$ **= -6 V.** Let R_L **= 1 kΩ** and V_{BB} **= 1.40 V.** For the case of the output voltage v_O **= -4 V:**

(i) **Determine** i_L, i_{Cp}, i_{Cn}, and v_I. [6 marks]

(ii) **Calculate** the power dissipated in transistor Q_n and Q_p. [4 marks]

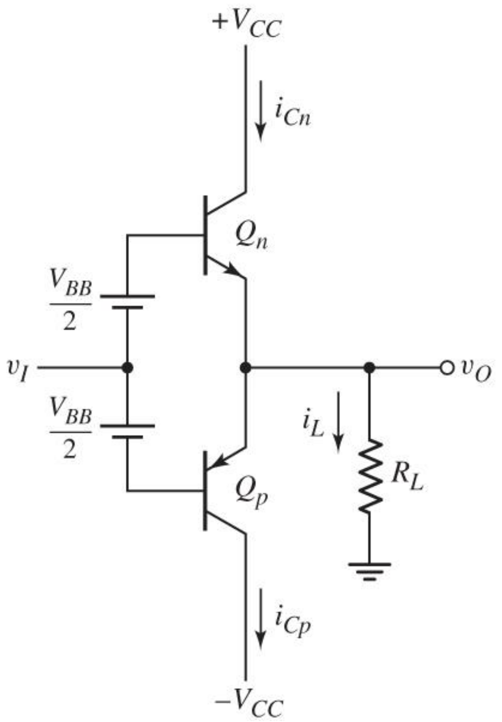


Figure 3

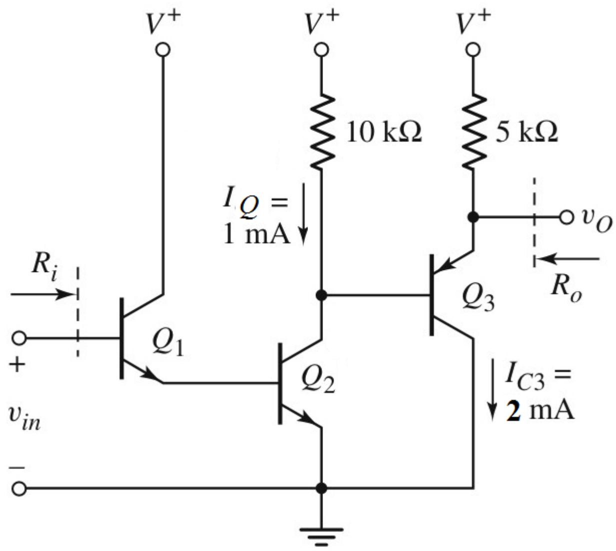


Figure 4

(b) **Figure 4** shows a circuit with the transistor parameters as β **= 120**, and $V_A = \infty$**.** The bias currents in the transistors are indicated on the figure. **Determine** the **input resistance (R_i)** and the **output resistance (R_o)** of the circuit. [10 marks]

Question 4 [20 marks]

(a) Study the input stage and bias circuit of the 741 op-amp in **Figure 5**. The circuit parameters are V^+ **= +15 V**, V^- **= -15 V**, and I_{C9} **= 10 μA**. The transistor parameters are β **= 200,** $V_{BE6} = V_{BE7}$ **= 0.6 V,** and the reverse saturation current $I_S = 10^{-14}$ **A** for each transistor. Ignore the base currents and assume the DC currents in the input stage are **exactly balanced**.

Given that the current flowing through resistor R_5 is **1 mA**.

(i) **Determine** the values of resistor R_4 and R_5. [5 marks]

(ii) **Calculate** values for current I_{C1} and resistance $r_{\pi 6}$. [3 marks]

(iii) **Determine** the DC voltage at the collector of Q_6 (i.e. V_{C6}). [2 marks]

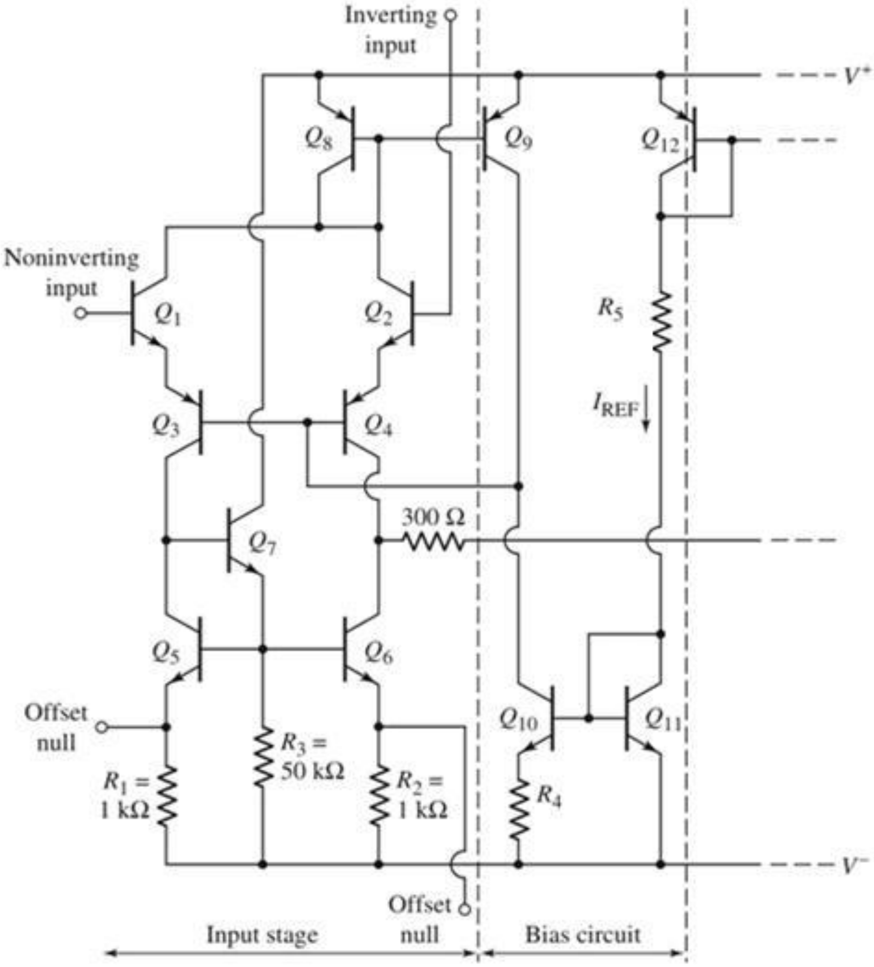


Figure 5

(b) Consider the **MC14573** op-amp in **Figure 6.** Assume transistor parameters of V_{TN} **= 0.5 V**, V_{TP} **= -0.5 V**, K_n **= 125 μA/V²**, K_p **= 100 μA/V²**, λ_n **= 0.01 V⁻¹**, λ_p **= 0.02 V⁻¹** and the circuit parameters of V^+ **= +10 V** and V^- **= -10 V**.

Given that V_{SG5} **= 1.5 V**:

(i) **Find** the DC bias currents I_Q. [4 marks]

(ii) **Determine** the **overall small signal differential-mode voltage gain** for the **MC14573** op-amp in **Figure 6**. Gain for the output stage consists of transistor M_7 and M_8 is given by equation $A_{v2} = g_{m7}(r_{o7} \| r_{o8})$. [6 marks]

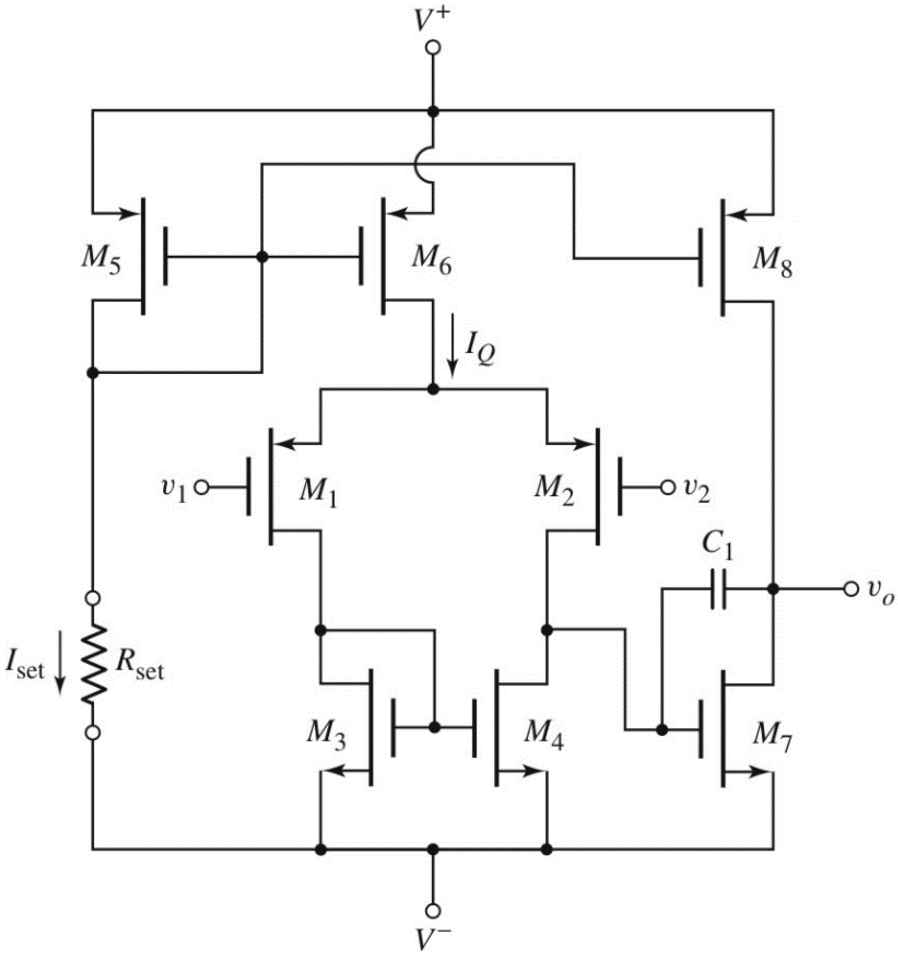


Figure 6

Question 5 [20 marks]

(a) With a **feedback resistor (R_2)** of **250 kΩ**, **design** an amplifier using op-amp in non-inverting configuration with a **closed-loop gain** which can be **varied from 11 to 51 V/V.** The closed-loop gain can be varied using a **potentiometer (R_{1V})** and a **fixed-value resistor (R_{1F})**. **Draw and label clearly** your circuit design. [6 marks]

(b) Consider the two inverting op-amp circuit connected in cascade as shown in **Figure 7**. Let R_1 **= 75 kΩ**, R_2 **= 100 kΩ**, R_3 **= 80 kΩ**, and R_4 **= 200 kΩ**. **Calculate** v_{O1}/v_I and v_O/v_I for the circuit. [4 marks]

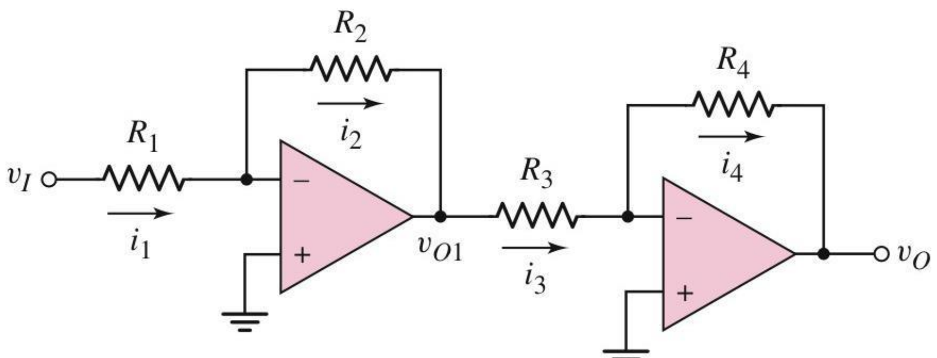


Figure 7

(c) **Figure 8** shows a design for an **instrumentation amplifier** using op-amps. In the design, $\boldsymbol{R_{1POT}}$ is a **100 kΩ potentiometer** (or a variable resistor) used to provide variable resistance so that differential voltage gain ($\boldsymbol{A_v}$) of the instrumentation amplifier can be adjustable. With analysis, it can be shown that output voltage ($\boldsymbol{v_O}$) is given by

$$v_O = \frac{R_4}{R_3}\left(1 + \frac{2R_2}{R_1 + R_{1POT}}\right)(v_{I2} - v_{I1})$$

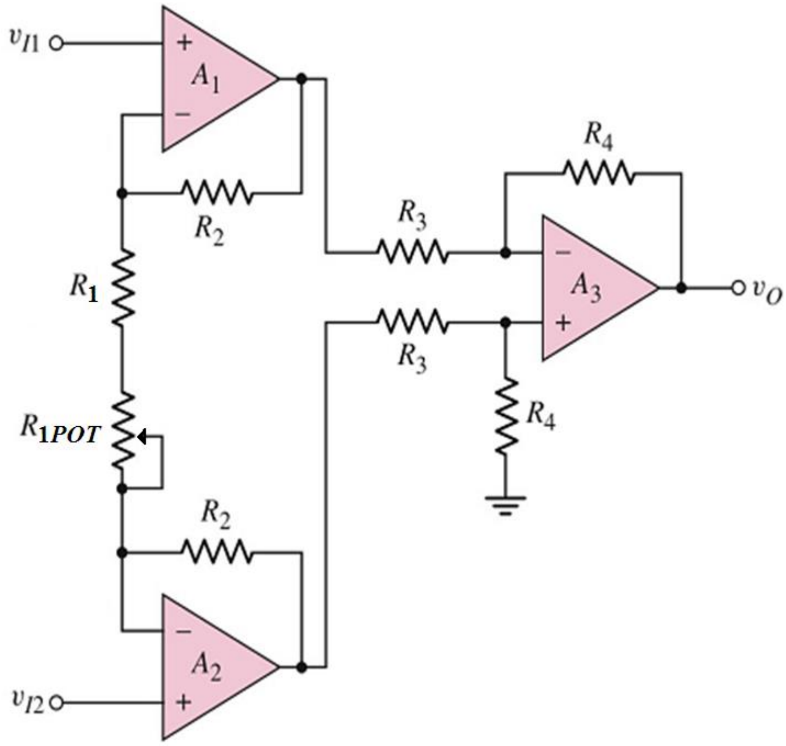


Figure 8

(i) With $\boldsymbol{R_3}$ = $\boldsymbol{R_4}$ = **100 kΩ**, **design an instrumentation amplifier** using the circuit as shown in the **Figure 8** to realize a differential voltage gain ($\boldsymbol{A_v}$) adjustable from **10 to 100.** (Hints: $\boldsymbol{A_v}$ is smallest when $\boldsymbol{R_{1POT}}$ is at maximum value, and vice versa. You are required to determine the value of $\boldsymbol{R_1}$ and $\boldsymbol{R_2}$ in the circuit). [7 marks]

(ii) **Calculate** $\boldsymbol{A_v}$ and $\boldsymbol{v_O}$ when $\boldsymbol{v_{I1}}$ **= 1.45 V,** $\boldsymbol{v_{I2}}$ **= 1.13 V**, $\boldsymbol{R_4}$ = **2** $\boldsymbol{R_3}$, $\boldsymbol{R_{1POT}}$ is set at **40 kΩ**, and the values of $\boldsymbol{R_1}$ and $\boldsymbol{R_2}$ are found in step (i) above. [3 marks]

-END OF QUESTION PAPER-

APPENDIX:

A) BASIC FORMULA FOR TRANSISTOR

BJT

$$i_C = I_S e^{v_{BE}/V_T} \quad ;\text{NPN}$$

$$i_C = I_S e^{v_{EB}/V_T} \quad ;\text{PNP}$$

$$i_C = \beta i_B = \frac{\beta}{\beta+1} i_E$$

$$i_E = i_B + i_C$$

;Small signal

$$\beta = g_m r_\pi$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

$$V_T = 26\,\text{mV}$$

MOSFET

;N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n [v_{GS} - V_{TN}]^2$$

$$K_n = \frac{\mu_n C_{ox} W}{2L} = \frac{k_n'}{2} \cdot \frac{W}{L}$$

;P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p [v_{SG} + V_{TP}]^2$$

$$K_p = \frac{\mu_p C_{ox} W}{2L} = \frac{k_p'}{2} \cdot \frac{W}{L}$$

;Small signal

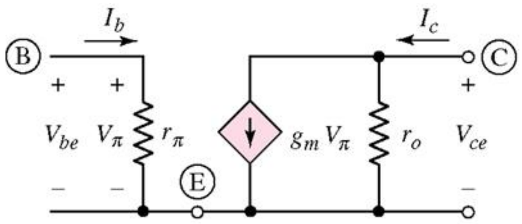
$$g_m = 2\sqrt{K_n I_{DQ}} \quad ;\text{N – MOSFET}$$

$$g_m = 2\sqrt{K_p I_{DQ}} \quad ;\text{P – MOSFET}$$

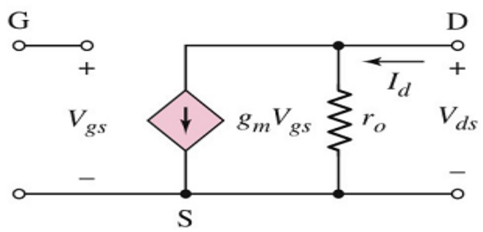
$$r_o \cong \frac{1}{\lambda I_{DQ}}$$

B) HYBRID-π EQUIVALENT CIRCUITS

BJT



MOSFET



C) QUADRATIC FORMULA

$$Ax^2 + Bx + C = 0 \quad \rightarrow \quad x = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$