UNIVERSITI TENAGA NASIONAL

COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 1 2017 / 2018

PROGRAMME	**: Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	**: EEEB273**
SUBJECT	**: ELECTRONIC ANALYSIS AND DESIGN II**
DATE	**: September 2017**
TIME	**: 3 hours**

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **FIVE** (5) questions in **NINE** (9) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided. **Use pen** to write your answer.
4. Write answer to different question on **a new page**.

THIS QUESTION PAPER CONSISTS OF NINE* (9) *PRINTED PAGES INCLUDING THIS COVER PAGE.

Question 1 [20 marks]

Figure 1 is NMOS current source circuit with the transistor M_2 sourcing a bias current to the load circuit.

(a) Draw the **PMOS version** of the current source. **[5 marks]**

(b) Using the **PMOS current source circuit** drawn in **Question 1(a)**, assume that the circuit is biased at $V^+ = 5$ **V** and $V^- = -5$ **V**. The transistors parameters are $V_{TP} = -0.5$ **V**, $k'_p = 50\ \mu A/V^2$, $(W/L)_1 = (W/L)_2 = 15$, $(W/L)_3 = 3$, and $\lambda = 0$. Calculate I_{REF}, I_O and V_{SD2}**(sat)**. **[15 marks]**

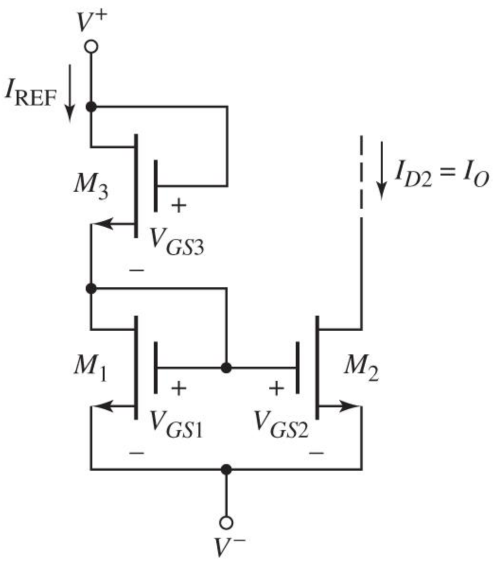


Figure 1

<u>Question 2 [20 marks]</u>

For a **MOSFET differential amplifier** shown in **Figure 2** the circuit parameters are: $\boldsymbol{V^+ = 3}$ **V** and $\boldsymbol{V^- = -3}$ **V**. Transistor parameters for **N-MOSFET** are: $\boldsymbol{V_{TN} = 0.5}$ **V**, $\boldsymbol{k'_n = 100\ \mu A/V^2}$ and $\boldsymbol{\lambda_n = 0.02\ V^{-1}}$; and the transistor parameters for **P-MOSFET** are: $\boldsymbol{V_{TP} = -0.5}$ **V**, $\boldsymbol{k'_p = 40\ \mu A/V^2}$ and $\boldsymbol{\lambda_p = 0.03\ V^{-1}}$. The transistor aspect ratios are: $\boldsymbol{(W/L)_1 = 20, (W/L)_2 = 80}$ and for the other transistors, $\boldsymbol{(W/L)_{3\text{-}10} = 10}$. It is given that I_{REF} = 0.5mA.

(a) Calculate the differential gain A_d. **[6 marks]**

(b) The biasing constant current source I_Q is a **cascode current source**. Calculate the **output resistance**, R_o of the current source. **[4 marks]**

(c) It is given that the common-mode rejection ratio (CMRR) of the differential amplifier is **71dB**. By how much should the output resistance, R_o of the cascode current source should decrease or increase such that the **CMRR increases to 80dB**? Calculate the new value of the output resistance.

[10 marks]

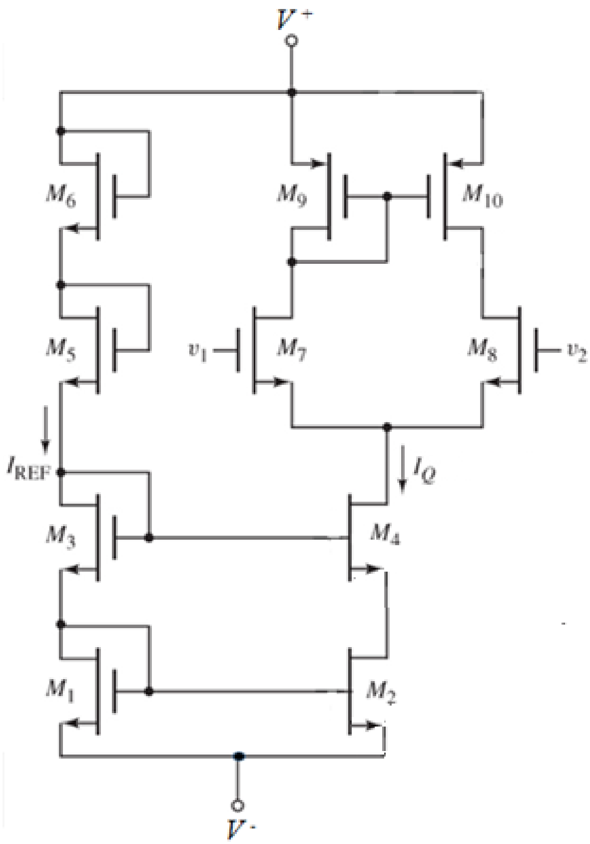


Figure 2

Question 3 [20 marks]

The transistor parameters for the circuit in **Figure 3** are: $\boldsymbol{\beta}$ **= 200,** $\boldsymbol{V_{BE}}$**(on) = 0.7 V**, and $\boldsymbol{V_A}$ **= 80 V**. For $\boldsymbol{Q_1}$ and $\boldsymbol{Q_2}$, $V_A = \infty$**.** The diff-amp has a common-mode voltage gain of $\boldsymbol{A_{cm1} = -0.0749}$. It is given that $\boldsymbol{I_{C3} = 1.886}$ **mA** and $\boldsymbol{I_{C5} = 1.003}$ **mA**.

(a) Calculate the differential-mode input resistance ($\boldsymbol{R_{id}}$) and common-mode input resistance ($\boldsymbol{R_{icm}}$). **[7 marks]**

(b) Determine the differential-mode voltage gain $\boldsymbol{A_d = v_{O3}/v_d}$ and the common-mode voltage gain $\boldsymbol{A_{cm} = v_{O3}/v_{cm}}$. **[10 marks]**

(c) If $A_{cm} = 0$, determine the **output voltage** $\boldsymbol{v_{O3}}$ if $\boldsymbol{v_1 = 2.015 \sin \omega t}$ **mV** and $\boldsymbol{v_2 = 1.985 \sin \omega t}$ **mV**. **[3 marks]**

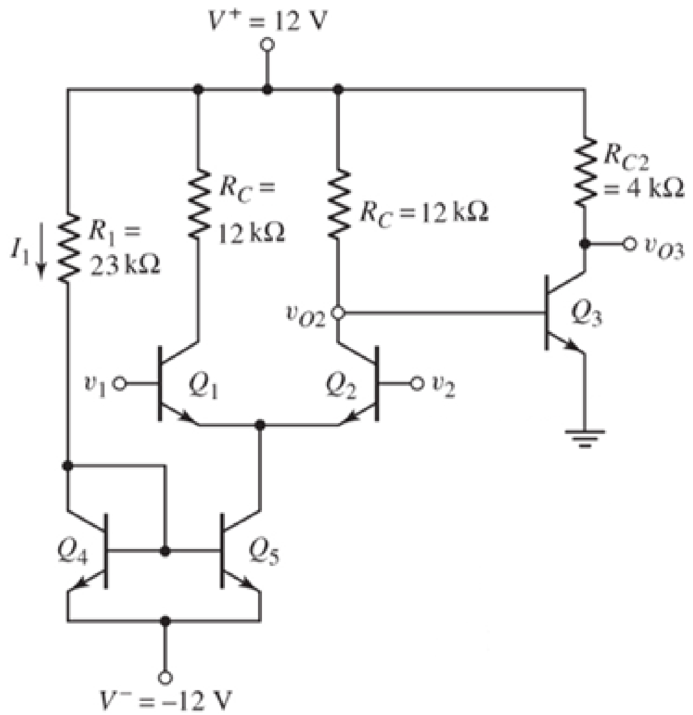


Figure 3

Question 4 [25 marks]

(a) Refer to the output stage circuits shown in **Figure 4(a)** and **Figure 4(b)**.

(i) **Identify** the output stage circuits shown in the **Figure 4(a)** and **Figure 4(b).** Then, **describe** clearly the differences between the output stages shown in the **Figure 4(a)** and **Figure 4(b)** in terms of advantage(s) and/or disadvantage(s) of the designs.

[5 marks]

(ii) For the output stage shown in **Figure 4(b)**, assume that $V_{CC} = 10$ V, $V_{BB} = 1.35$ V, and $R_L = 1$ kΩ. Transistor Q_n and Q_p have $I_S = 4\times10^{-15}$ A. Given that output voltage $v_O = -8$ V, **calculate** the currents i_L, i_{Cn}, and i_{Cp}, the input voltage v_I, and the power dissipation in the transistors Q_n and Q_p. **[10 marks]**

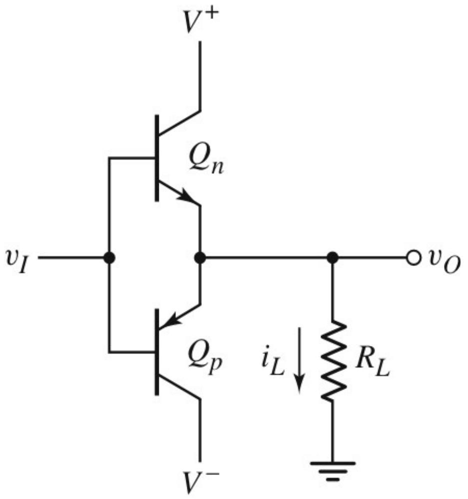


Figure 4(a)

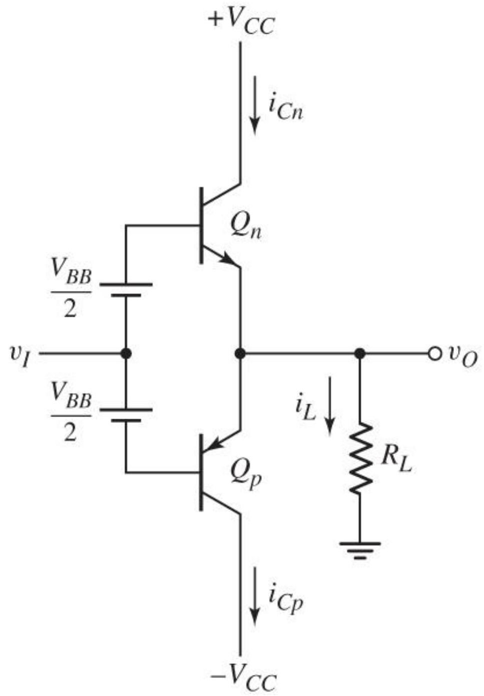


Figure 4(b)

(b) The 741 op-amp is shown in **Figure 5.** The minimum recommended supply voltages are $\boldsymbol{V^{+} = 5}$ **V** and $\boldsymbol{V^{-} = -5}$ **V**. Assume that $\boldsymbol{V_{BE(on)} = V_{EB(on)} = 0.65}$ **V**, $\boldsymbol{\beta_n = 200}$, and $\boldsymbol{\beta_p = 60}$. Calculate I_{C16} if $R_8 = 0$. What is the function of resistor R_8 in the gain stage?

[10 marks]

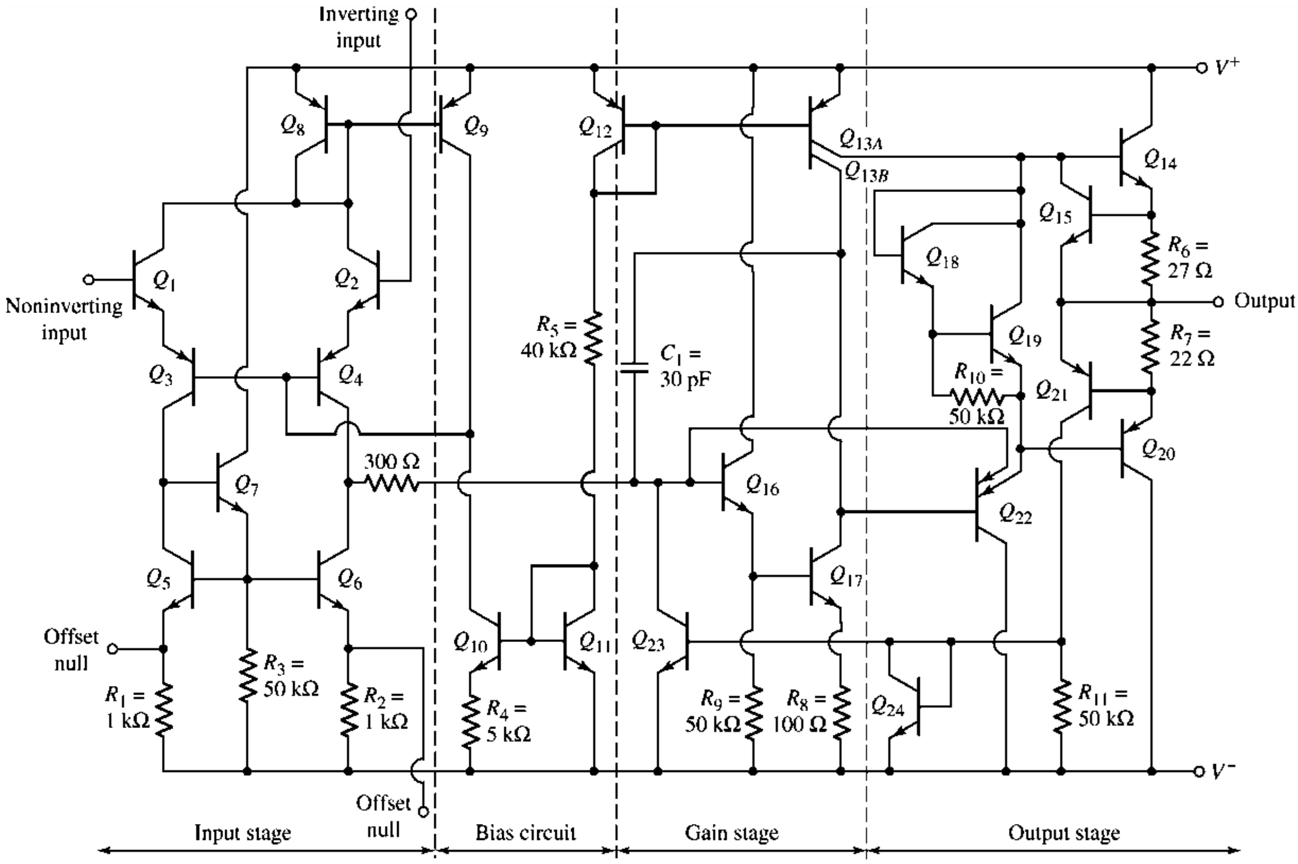


Figure 5

Question 5 [15 marks]

(a) Consider **two (2)** ideal op-amp circuits connected in cascade as shown in **Figure 6**. Given that $\boldsymbol{R_1}$ **= 50 kΩ**, $\boldsymbol{R_2}$ **= 100 kΩ**, $\boldsymbol{R_3}$ **= 80 kΩ**, and $\boldsymbol{R_4}$ **= 75 kΩ**. **Calculate voltage gain** $\boldsymbol{v_O/v_I}$ of the overall circuit. **[5 marks]**

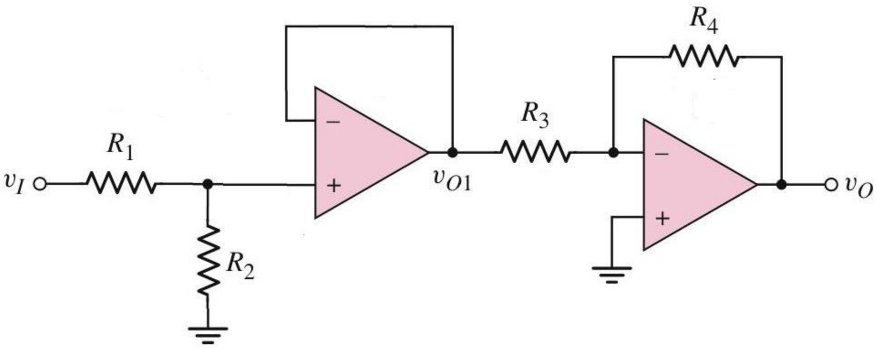


Figure 6

(b) **Figure 7** <u>in the following page</u> shows a design for an **instrumentation amplifier** using op-amps. The instrumentation amplifier has **adjustable differential voltage gain** ($\boldsymbol{A_v}$). In the design, $\boldsymbol{R_{1POT}}$ is a **potentiometer** (or a variable resistor) used **to provide variable resistance** so that differential voltage gain of the instrumentation amplifier can be adjustable. With analysis, it can be shown that output voltage ($\boldsymbol{v_O}$) for the **difference amplifier** constructed using op-amp $\boldsymbol{A_3}$, resistors $\boldsymbol{R_3}$, and resistors $\boldsymbol{R_4}$ is

$$v_O = \frac{R_4}{R_3}\left(v_{O2} - v_{O1}\right)$$

(i) **Study Figure 7 carefully**. Using same labels for all resistors, voltages and currents given in the **Figure 7**, **show** that the output voltage (v_O) of the **instrumentation amplifier with adjustable differential voltage gain** is

[7 marks]

$$v_O = \frac{R_4}{R_3}\left(1 + \frac{2R_2}{R_{1f} + R_{1POT}}\right)(v_{I2} - v_{I1})$$

(ii) For the circuit in **Figure 7,** given that $R_4 = 2.5\ R_3$, $R_2 = 495\ \text{k}\Omega$, $R_{1f} = 15\ \text{k}\Omega$, R_{1POT} is set at **40 kΩ**, $v_{I1} = 0.090$ **V,** and $v_{I2} = 0.115$ **V**. **Calculate** adjustable differential voltage gain (A_v) and the output voltage (v_O) of the circuit.

[3 marks]

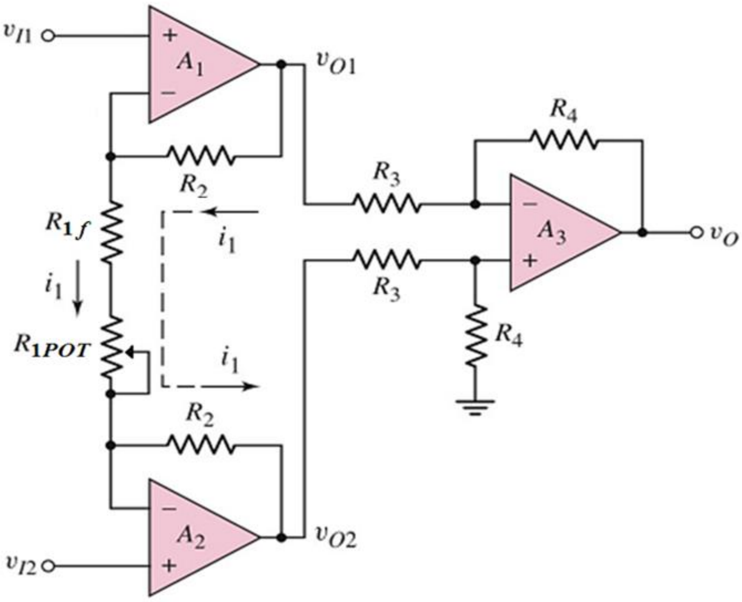


Figure 7

-END OF QUESTION PAPER-

APPENDIX:

A) BASIC FORMULA FOR TRANSISTOR

BJT

$i_C = I_S e^{v_{BE}/V_T}$; NPN

$i_C = I_S e^{v_{EB}/V_T}$; PNP

$i_C = \beta i_B = \dfrac{\beta}{\beta+1} i_E$

$i_E = i_B + i_C$

; Small signal

$\beta = g_m r_\pi$

$g_m = \dfrac{I_{CQ}}{V_T}$

$r_\pi = \dfrac{\beta V_T}{I_{CQ}}$

$r_o = \dfrac{V_A}{I_{CQ}}$

$V_T = 26\,\text{mV}$

MOSFET

; N – MOSFET

$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$

$i_D = K_n [v_{GS} - V_{TN}]^2$

$K_n = \dfrac{\mu_n C_{ox} W}{2L} = \dfrac{k_n^{'}}{2} \cdot \dfrac{W}{L}$

; P – MOSFET

$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$

$i_D = K_p [v_{SG} + V_{TP}]^2$

$K_p = \dfrac{\mu_p C_{ox} W}{2L} = \dfrac{k_p^{'}}{2} \cdot \dfrac{W}{L}$

; Small signal

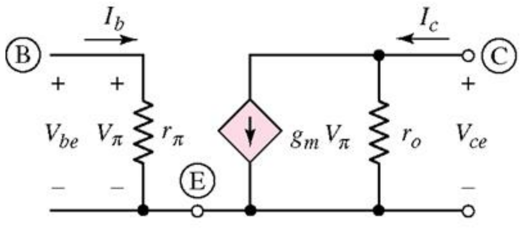
$g_m = 2\sqrt{K_n I_{DQ}}$; N – MOSFET

$g_m = 2\sqrt{K_p I_{DQ}}$; P – MOSFET

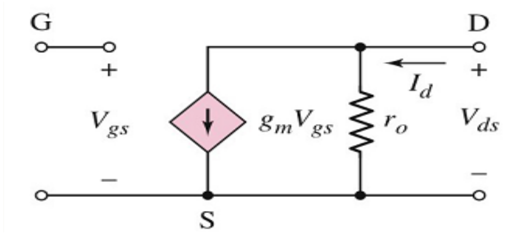
$r_o \cong \dfrac{1}{\lambda I_{DQ}}$

B) HYBRID-π EQUIVALENT CIRCUITS

BJT



MOSFET



C) QUADRATIC FORMULA

$$Ax^2 + Bx + C = 0 \quad \rightarrow \quad x = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$