Name:

Student ID Number:

Section Number: 01/02/03/04/05/06 A/B

Lecturer: Dr Azni Wati/ Dr Fazrena Azlee/ Dr Jehana Ermy/ Dr Jamaludin

Table Number:

UNIVERSITI TENAGA NASIONAL

College of Engineering

Department of Electronics and Communication Engineering

Test 2

SEMESTER 1, ACADEMIC YEAR 2017/2018

Subject Code	:	**EEEB273**
Course Title	:	**Electronics Analysis & Design II**
Date	:	**19 August 2017**
Time Allowed	:	**2 hours**

Instructions to the candidates:

1. Write your Name and Student ID Number. Indicate your Section Number and Lecturer's Name. Write also your Table Number.
2. **Write all your answers using pen**. **DO NOT USE PENCIL** except for the diagram.
3. **ANSWER ALL QUESTIONS. Show clearly** all your calculations. Every value **must** be written with its correct Unit.
4. **WRITE YOUR ANSWER ON THIS QUESTION PAPER.**

NOTE: DO NOT OPEN THE QUESTION PAPER UNTIL INSTRUCTED TO DO SO.

☺ **GOOD LUCK!** ☺

Question Number	Q1	Q2	Q3	Q4	Total
Marks					

APPENDIX

A) BASIC FORMULA FOR TRANSISTOR

BJT

$$i_C = I_S e^{v_{BE}/V_T} \quad ;\text{NPN}$$

$$i_C = I_S e^{v_{EB}/V_T} \quad ;\text{PNP}$$

$$i_C = \beta i_B = \frac{\beta}{\beta+1} i_E$$

$$i_E = i_B + i_C$$

;Small signal

$$\beta = g_m r_\pi$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

$$V_T = 26\,\text{mV}$$

MOSFET

$$;\text{N}-\text{MOSFET}$$

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n[v_{GS} - V_{TN}]^2$$

$$K_n = \frac{\mu_n C_{ox} W}{2L} = \frac{k_n'}{2} \cdot \frac{W}{L}$$

$$;\text{P}-\text{MOSFET}$$

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p[v_{SG} + V_{TP}]^2$$

$$K_p = \frac{\mu_p C_{ox} W}{2L} = \frac{k_p'}{2} \cdot \frac{W}{L}$$

;Small signal

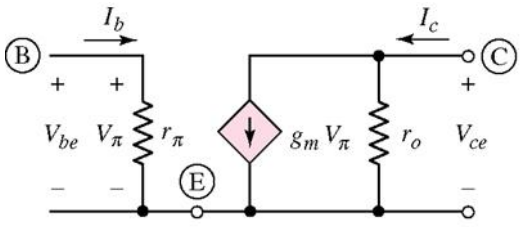
$$g_m = 2\sqrt{K_n I_{DQ}} \quad ;\text{N}-\text{MOSFET}$$

$$g_m = 2\sqrt{K_p I_{DQ}} \quad ;\text{P}-\text{MOSFET}$$

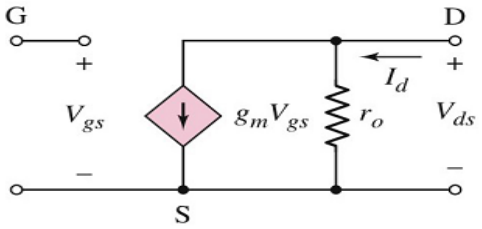
$$r_o \cong \frac{1}{\lambda I_{DQ}}$$

B) HYBRID-π EQUIVALENT CIRCUITS

BJT



MOSFET



C) QUADRATIC FORMULA

$$Ax^2 + Bx + C = 0 \quad \rightarrow \quad x = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$

QUESTION 1 [20 marks]

The differential amplifier in **Figure 1** has a pair of transistors forming an active load. A two-transistor current source is added to bias a constant current source of **0.25 mA**. (Note: I_Q **= 0.25 mA)**. The transistor parameters are β **= 100**, V_{BE} **(on) =** V_{EB}**(on) = 0.7 V**, V_{AN} **= 120 V, and** V_{AP} **= 100 V**.

(i) Draw a complete circuit for **Figure 1** with the active load and the bias circuit. **[5 marks]**

(ii) Determine the differential-mode voltage gain, $A_d = v_O/v_d$. **[10 marks]**

(iii) Calculate the differential-mode voltage gain if the load resistance, R_L, is 150 kΩ. **[5 marks]**

Answers for Question 1

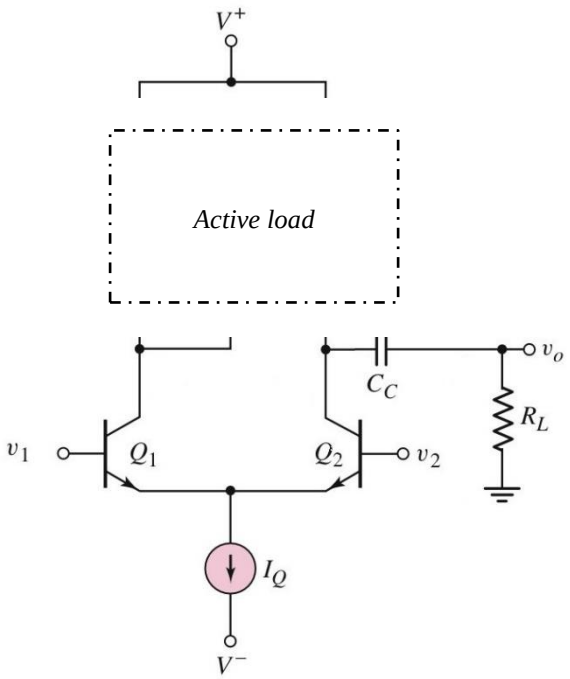


Figure 1

Answers for Question 1 (continued)

QUESTION 2 [35 marks]

The MOSFET differential amplifier shown in Figure 2 below is connected to supply voltages of V^+ = +5V and V^- = -5V. The value of R_{set} is 15 kΩ. Transistor parameters for **N-MOSFET** are: V_{TN} **= 2 V**, k_n**' = 40** μ**A/V**^{2} and λ_n **= 0.01 V**$^{-1}$; and the transistor parameters for **P-MOSFET** are: V_{TP} **= -2 V**, k_p**' = 20** μ**A/V**^{2} and λ_p **= 0.02 V**$^{-1}$. The transistor aspect ratios are $(W/L)_{A,B}$=20 , $(W/L)_{C,D}$=15 and $(W/L)_{E,F}$=10.

(a) Calculate the values of I_{set}, I_Q, V_{SGA} and V_{SGC}. [12 marks]

(b) Determine the gain of the differential amplifier. [8 marks]

(c) Another amplifier is connected at the output of the differential amplifier as a second gain stage, to form a multistage amplifier circuit. If the second gain stage has input impedance R_{in2} of 200MΩ and gain A_{V2} = 80 V/V, calculate the overall gain of the multistage circuit. [5 marks]

(d) The biasing current source circuit generating I_Q for the differential amplifier is now changed to a Wilson current source.

i) Sketch the circuit in Figure 2 with its new biasing current source circuit. [5 marks]

ii) Discuss the advantage and disadvantage of using the Wilson current source over the two-transistor current source for biasing the differential amplifier circuit. [5 marks]

Answers for Question 2

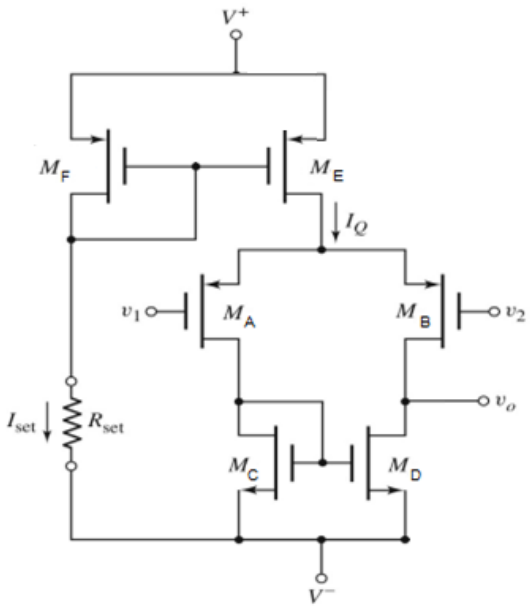


Figure 2

Answers for Question 2 (Continued)

QUESTION 3 [20 marks]

Consider the **Class- A** amplifier circuit shown in Figure 3. Assume all transistors are matched with V_{BE} (on) = 0.7 V, V_{CE} (sat) = 0.38 V, and is very large β is very large. Determine the following:

(i) The range of the maximum symmetrical output voltage swing. [4 marks]

(ii) The required bias current I_Q for Class-A operation. [2 marks]

(iii) Maximum and minimum amplifier current ($i_{E1(max)}$ and $i_{E1(min)}$). [4 marks]

(iv) Maximum and minimum input voltage ($v_{I(max)}$ and $v_{I(min)}$). [3 marks]

(v) Power conversion efficiency of the amplifier, η. [7 marks]

Answers for Question 3

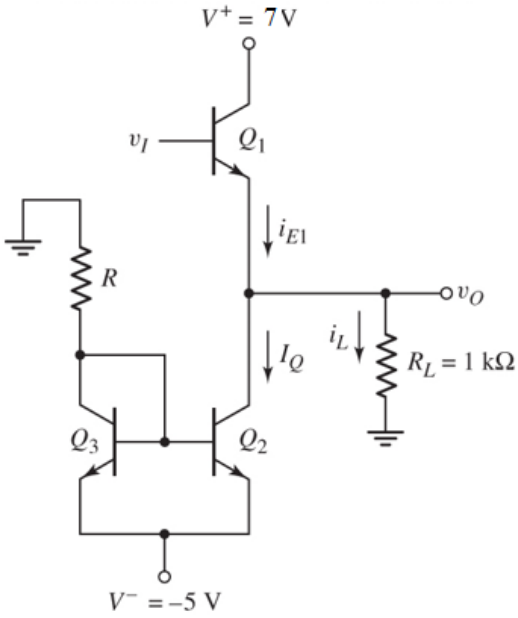


Figure 3

Answers for Question 3 (Continued)

QUESTION 4 [25 marks]

Consider the circuit shown in **Figure 4**. Study the **Figure 4** thoroughly and ***notice that biasing for the amplifiers in the circuit is provided by two-transistor current mirrors***.

The circuit parameters for the **Figure 4** are $I_{C7} = I_{C11} = 0.2$ **mA**, $I_{C8} = 1.3$ **mA**, and $R_2 = 12$ **kΩ**. Assume $\beta = 100$ for all transistors and the **Early voltage** for Q_{11} is **100 V**.

Using small-signal analysis, the small-signal voltage gain (A_v) for the **Darlington Pair** in the gain stage can be found using the following formula:

$$A_v = \frac{\beta(1+\beta)R_{L7}}{R_i}$$

Calculate the value of I_{C6} and the value of small-signal voltage gain (A_v) for the Darlington Pair in the gain stage. [25 marks]

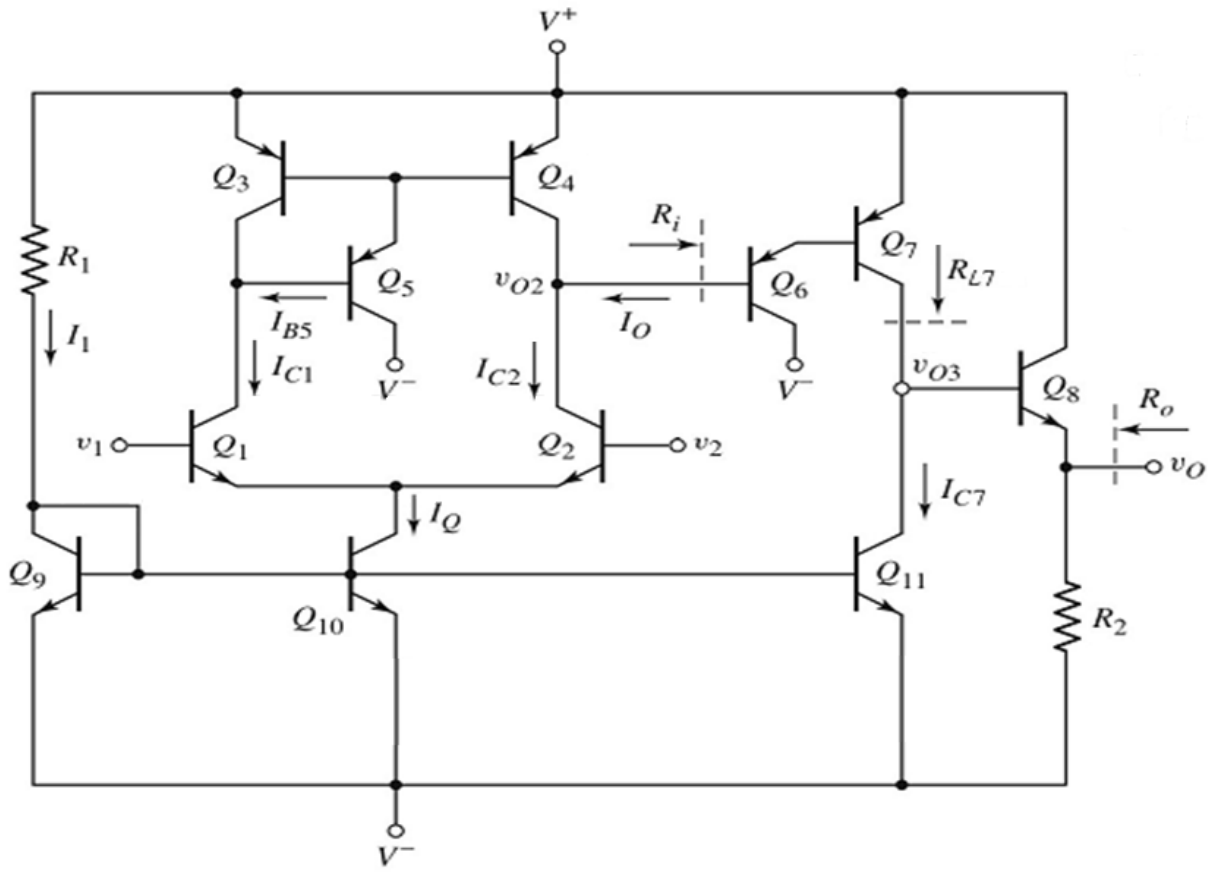


Figure 4

Answers for Question 4