COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 2 2017 / 2018

PROGRAMME	: **Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	: **EEEB273**
SUBJECT	: **ELECTRONIC ANALYSIS AND DESIGN II**
DATE	: **January/February 2018**
TIME	: **3 hours**

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **FIVE** (5) questions in **NINE** (9) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided. **Use pen** to write your answer.
4. Write answer to different question on **a new page**.

THIS QUESTION PAPER CONSISTS OF NINE* (9) *PRINTED PAGES INCLUDING THIS COVER PAGE.

Question 1 [20 marks]

(a) **Draw** the npn BJT **two-transistor** and **Widlar** current sources with clear details of the transistors Q_1 and Q_2 placements. **[10 marks]**

(b) **Show** that $I_O R_E = V_T \ln\left(\frac{I_{REF}}{I_O}\right)$ for the BJT **Widlar** current source. **[5 marks]**

(c) **Design** the BJT **Widlar** current source from your drawing in part (a) such that currents I_{REF} **= 3 mA** and I_O **= 50 μA**. The circuit parameters are V^+ **= 10 V** and V^- **= –10 V**. The transistors are matched with V_{BE} **= 0.7 V** at **1 mA**. Neglect the base current.

[5 marks]

Question 2 [20 marks]

(a) The basic differential pair biased by a three-transistor current source is shown in **Figure 1**. Assume $\beta = 200$ and $V_{BE}(on) = 0.7$ V for **all** BJTs in the circuit. For $R_1 = 10$ kΩ and $R_C = 12.8$ kΩ, **find** the differential voltage gain (*Ad*) of the differential amplifier taken as **one-sided output**. **[10 marks]**

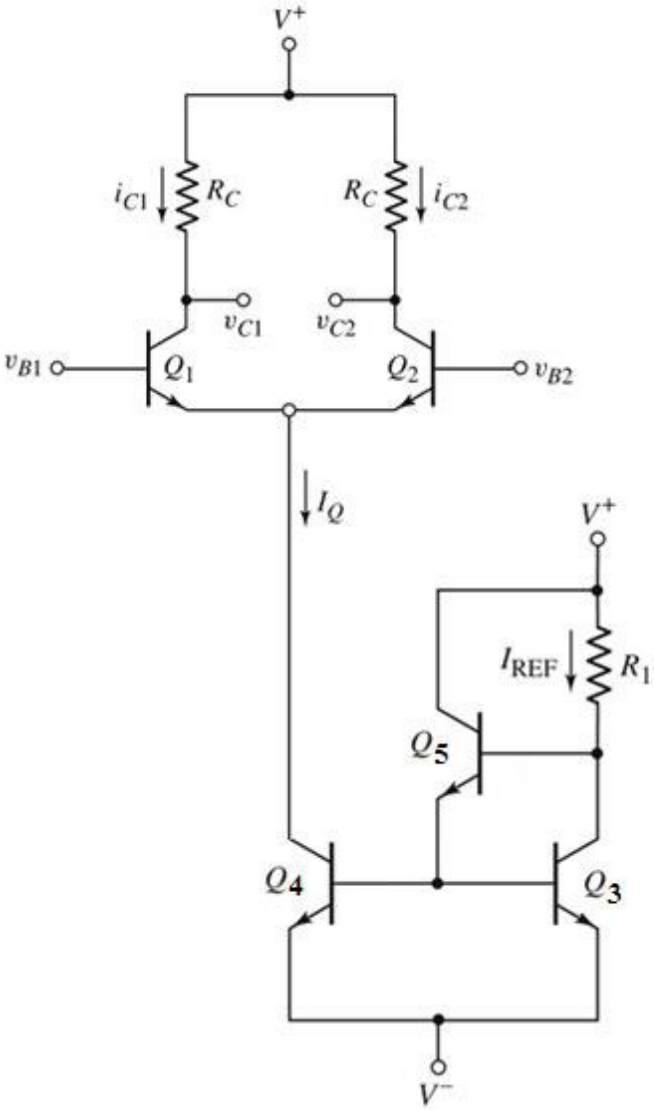


Figure 1

(b) **Figure 2** shows a differential amplifier with **PNP three-transistor** current mirror connected as an active load. The circuit are connected to $V^+ = 3$ **V,** $V^- = -3$ **V**, and $I_Q = 0.5$ **mA.** The transistors parameters are $\beta = 120$, $V_{A1} = V_{A2} = 120$ **V**, $V_{A3} = V_{A4} = 80$ **V**, and $V_{A5} = \infty$.

(i) **Determine** the open-circuit differential-mode voltage gain (A_d). **[5 marks]**

(ii) **What** is the output resistance (R_O) of the differential amplifier? **[2 marks]**

(iii) **Find** the value of load resistance R_L that reduces the differential-mode gain to **75 percent** of the open-circuit value. **[3 marks]**

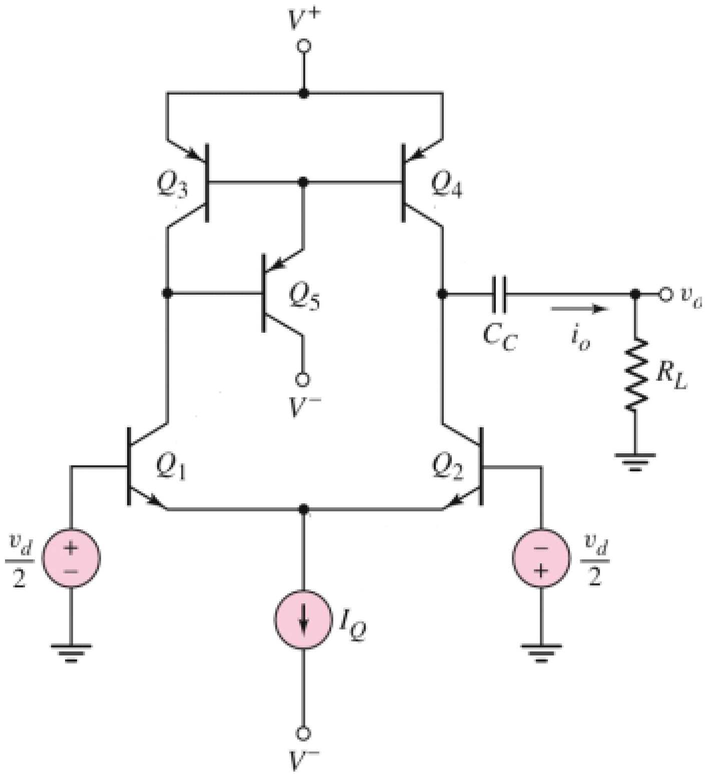


Figure 2

Question 3 [20 marks]

Consider the multi stage bipolar circuit in **Figure 3**. The transistors parameters are: $\boldsymbol{V_{BE}}$**(on) = 0.7 V,** $\boldsymbol{\beta}$ **= 150** and $V_A = \infty$. When there is no input, $\boldsymbol{v_O}$ = **-0.1316 V.**

(a) **Determine** the transistor quiescent currents: $\boldsymbol{I_{C2}}$**,** $\boldsymbol{I_{C3}}$**,** $\boldsymbol{I_{C4}}$**,** $\boldsymbol{I_{C6}}$**,** and $\boldsymbol{I_{C8}}$. **[10 marks]**

(b) Assume $\boldsymbol{R_{i3}}$ is very large compared to $\boldsymbol{R_5}$, calculate the **overall differential mode voltage gain (**$\boldsymbol{v_O/v_d}$**)** of the circuit in **Figure 3**. **[10 marks]**

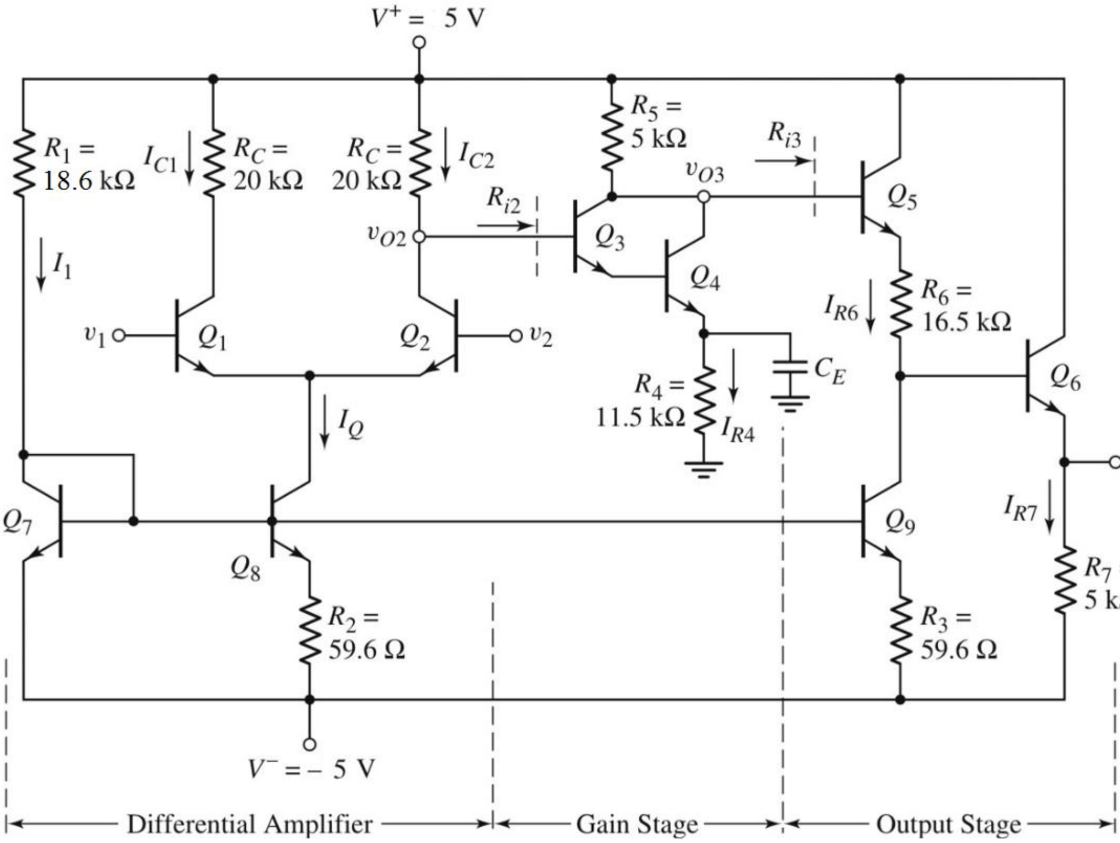


Figure 3

Question 4 [20 marks]

(a) An **idealized class B output stage** is to deliver **10 Watts** of average power to a load for a symmetrical input sine wave. The maximum output voltage required should be **80%** of the power supply voltage V_{CC}. Given that the power supply voltage is **24 V** and the average current in the circuit is $I = V_p / (\pi R_L)$, where R_L is the load. **Calculate** the value of the output stage's **power conversion efficiency** η. **[10 marks]**

(b) Consider the **MC14573** op-amp in **Figure 4.** Assume transistor parameters for **N-MOSFET** are V_{TN} **= 0.5 V**, K_n **= 100 μA/V^2** and λ_n **= 0.01 V^{-1}**; and transistor parameters for **P-MOSFET** are V_{TP} **= -0.5 V**, K_p **= 125 μA/V^2,** and λ_p **= 0.02 V^{-1}**.

Given that V_{SG5} **= 1.5 V:**

(i) **Find** the **quiescent bias currents** for all transistors in the **Figure 4**. **[4 marks]**

(ii) **Determine** the **overall small signal differential-mode voltage gain** for the **MC14573** op-amp in the **Figure 4**. Gain for the output stage consists of transistor M_7 and M_8 is given by equation $A_{v2} = -g_{m7}(r_{o7} \| r_{o8})$ **[6 marks]**

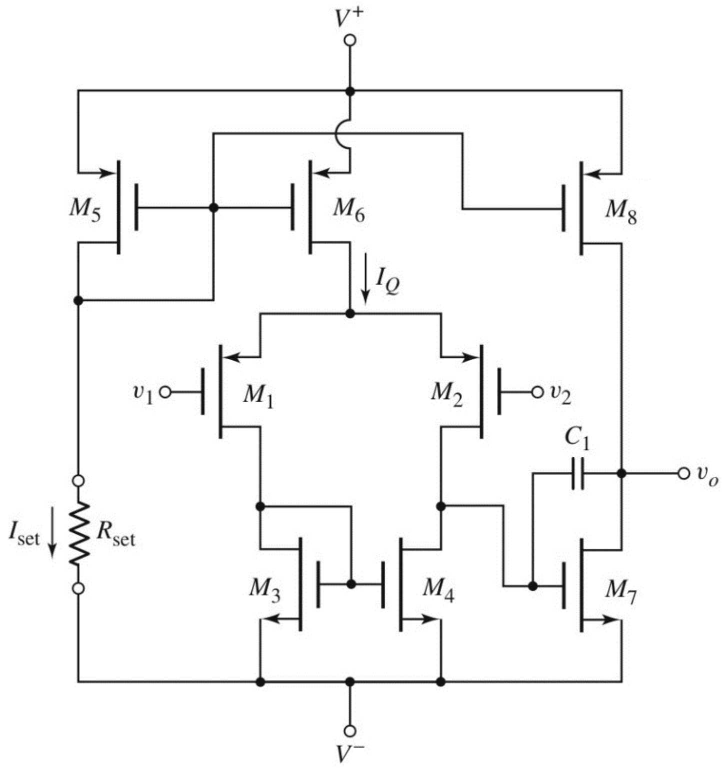


Figure 4

<u>Question 5 [20 marks]</u>

(a) An **ideal** inverting op-amp with adjustable **closed-loop voltage gain** is shown in **Figure 5**. **Calculate** its **<u>absolute</u>** minimum A_v and maximum A_v values when R_1 = **20 kΩ,** potentiometer R_{1V} **= 0 to 30 kΩ,** R_2 = **30 kΩ,** and potentiometer R_{2V} **= 0 to 40 kΩ.**

[10 marks]

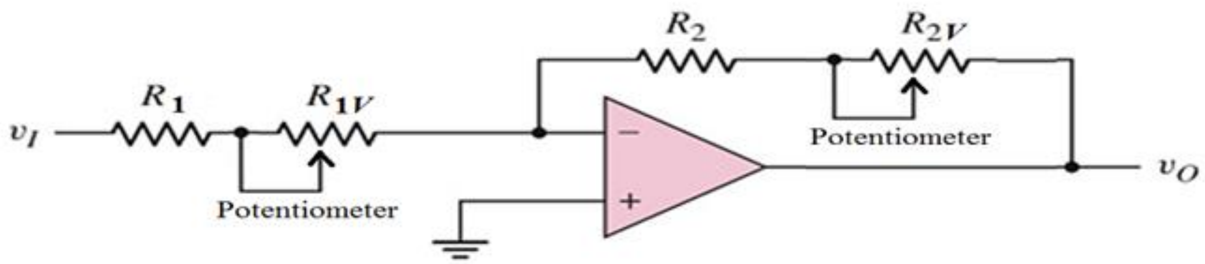


Figure 5

(b) For a **generalized summing op-amp** shown in **Figure 6** the **total output voltage (v_O)** is the **sum of the individual terms**, or

$$v_O = -\frac{R_F}{R_1} v_{I1} - \frac{R_F}{R_2} v_{I2} + \left(1 + \frac{R_F}{R_N}\right)\left(\frac{R_P}{R_A} v_{I3} + \frac{R_P}{R_B} v_{I4}\right)$$

where $R_N = R_1 \| R_2$

$R_P = R_A \| R_B \| R_C$

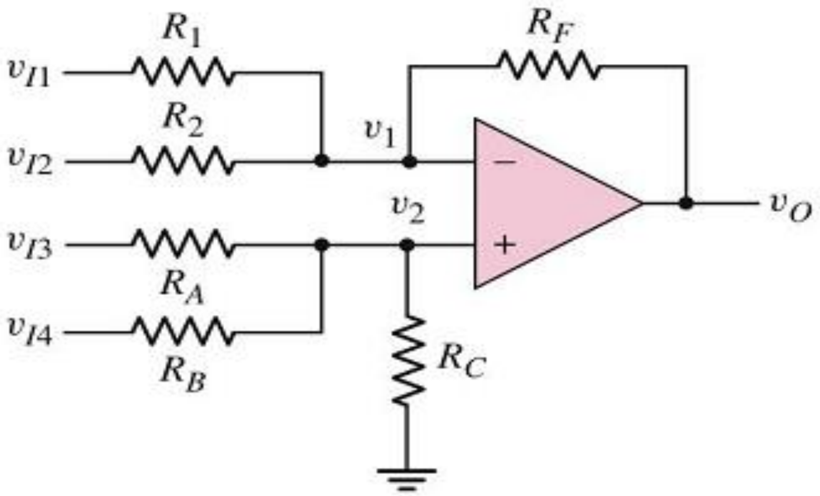


Figure 6

The summing op-amp similar to **Figure 6** is designed to produce the output of

$$v_O = -10v_{I1} - 5v_{I2} + 3v_{I3} + 5v_{I4}$$

Given that $\boldsymbol{R_1}$ = **50 kΩ** and $\boldsymbol{R_A}$ = **240 kΩ, calculate** the value of $\boldsymbol{R_2}$**,** $\boldsymbol{R_B}$**,** $\boldsymbol{R_C}$**,** and $\boldsymbol{R_F}$**.**

[10 marks]

-END OF QUESTION PAPER-

APPENDIX:

A) BASIC FORMULA FOR TRANSISTOR

BJT

$$i_C = I_S e^{v_{BE}/V_T} \quad ;\text{NPN}$$

$$i_C = I_S e^{v_{EB}/V_T} \quad ;\text{PNP}$$

$$i_C = \beta i_B = \frac{\beta}{\beta+1} i_E$$

$$i_E = i_B + i_C$$

;Small signal

$$\beta = g_m r_\pi$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

$$V_T = 26\,\text{mV}$$

MOSFET

;N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n[v_{GS} - V_{TN}]^2$$

$$K_n = \frac{\mu_n C_{ox} W}{2L} = \frac{k_n^{'}}{2} \cdot \frac{W}{L}$$

;P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p[v_{SG} + V_{TP}]^2$$

$$K_p = \frac{\mu_p C_{ox} W}{2L} = \frac{k_p^{'}}{2} \cdot \frac{W}{L}$$

;Small signal

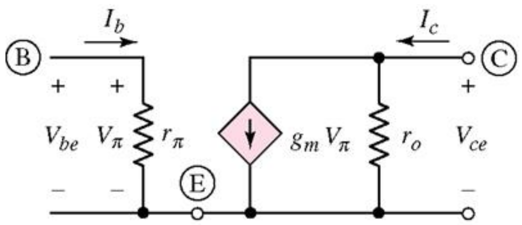
$$g_m = 2\sqrt{K_n I_{DQ}} \quad ;\text{N – MOSFET}$$

$$g_m = 2\sqrt{K_p I_{DQ}} \quad ;\text{P – MOSFET}$$

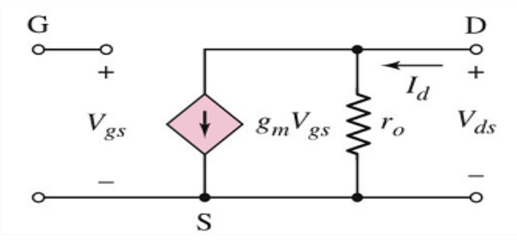
$$r_o \cong \frac{1}{\lambda I_{DQ}}$$

B) HYBRID-π EQUIVALENT CIRCUITS

BJT



MOSFET



C) QUADRATIC FORMULA

$$Ax^2 + Bx + C = 0 \quad \rightarrow \quad x = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$