Name:
Student ID Number:
Section Number: 01/02/03/04 A/B
Lecturer: Dr Jamaludin/ Dr Azni Wati/ Dr Jehana Ermy/ Prof Md Zaini
Table Number:

UNIVERSITI TENAGA NASIONAL

College of Engineering

Department of Electronics and Communication Engineering

Test 2

SEMESTER 2, ACADEMIC YEAR 2017/2018

Subject Code	:	**EEEB273**
Course Title	:	**Electronics Analysis & Design II**
Date	:	**30 December 2017**
Time Allowed	:	**2 hours**

Instructions to the candidates:

1. Write your Name and Student ID Number. Indicate your Section Number and Lecturer's Name. Write also your Table Number.
2. **Write all your answers using pen**. **DO NOT USE PENCIL** except for the diagram.
3. **ANSWER ALL QUESTIONS. Show clearly** all your calculations. Every value **must** be written with its correct Unit.
4. **WRITE ALL YOUR ANSWERS ON THIS QUESTION PAPER.**

NOTE: DO NOT OPEN THE QUESTION PAPER UNTIL INSTRUCTED TO DO SO.

☺ **GOOD LUCK!** ☺

Question Number	Q1a	Q1b-c	Q2a-d	Q2e	Q3	Q4a	Q4b	Total
Marks								

QUESTION 1 [20 marks]

A BJT differential amplifier shown in **Figure 1** is biased by a constant current source with I_Q = **0.23 mA**. The differential amplifier is to be redesigned with an active load. The active load to be used is a **BJT Wilson current source** using ***pnp* transistors**.

The transistor parameters are β **= 120,** V_{BE}**(on) =** V_{EB}**(on) = 0.7 V,** V_{AN} **= 100 V**, and V_{AP} **= 120 V.**

(a) **Draw** the new differential amplifier circuit added with the active load. **Label** the circuit correctly and clearly with appropriate symbols and numbering for transistors used in circuit. **[4 marks]**

(b) **Calculate** the differential-mode voltage gain, (A_d), of the new circuit. **[12 marks]**

(c) **Calculate** the differential-mode voltage gain, (A_d), of the differential amplifier circuit if the active load is changed to a **three-transistor current source**. Give your comment about values of A_d for the differential amplifier circuit using **Wilson current source** and **three-transistor current source** active loads. **[4 marks]**

Answers for Question 1

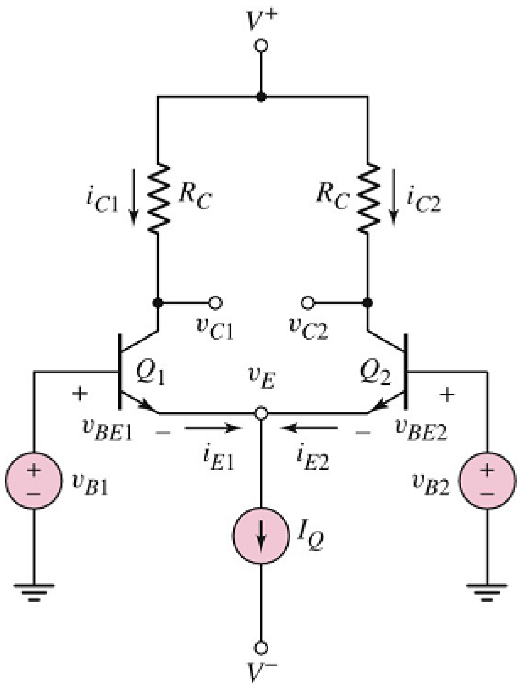

Figure 1

Answers for Question 1 (continued)

QUESTION 2 [35 marks]

Figure 2 shows a differential amplifier circuit with active loads and biased by a current source using **MOSFET**. Transistors M_1 and M_2 are driven into saturation with V_{DS}(sat)**= 1.12 V**. The active load transistors (M_3 and M_4) are matched with parameters $K_p = 0.1\ mA/V^2$, $V_{TP} = -2\ V$, and $\lambda_p = 0.02\ V^{-1}$. Transistors M_5, M_6 and M_7 are **identical**. All the **NMOS transistors** have the same $K_n = 0.2\ mA/V^2$, $V_{TN} = 2\ V$, and $\lambda_n = 0.015\ V^{-1}$.

(a) **Determine** I_1, I_Q, and I_{D1} when $v_1 = v_2 = 0$ V. **[6 marks]**

(b) **Determine** the **one-sided differential mode voltage gain** (A_d) for the differential amplifier if $R_L = 100\ k\Omega$. **[9 marks]**

(c) It is required that the **CMRR** of the circuit to be **60 dB**. **What** is the **common mode voltage gain** (A_{cm})? **[3 marks]**

(d) **Suggest 2 ways** to improve the **CMRR** for the circuit in the **Figure 2**. **[2 marks]**

(e) The MOSFET differential amplifier with active load in the **Figure 2** is replaced with the MOSFET differential amplifier with **Cascode active load**. **Draw** and label clearly all the transistors used in the new circuit. **[15 marks]**

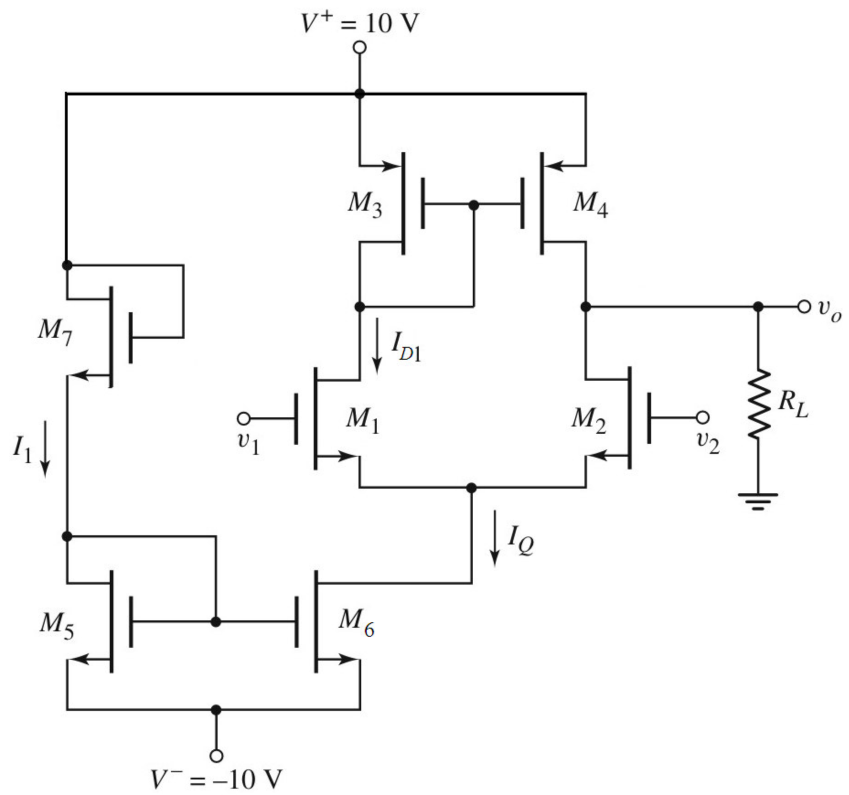

Figure 2

Answers for Question 2

Extra page for Answers – Indicate question number(s)

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QUESTION 3 [20 marks]

Consider the circuit shown in **Figure 3**. Study the **Figure 1** thoroughly. With supply voltage **±10V** and circuit parameters $\boldsymbol{R_1}$ **= 19.3 kΩ,** $\boldsymbol{R_2}$ **=** $\boldsymbol{R_3}$ **= 0.1 kΩ,** and $\boldsymbol{R_4}$ **= 5 kΩ** it can be calculated that the value of $\boldsymbol{I_Q}$ is **0.307 mA**.

Assume the quiescent values $\boldsymbol{I_{C7} = I_Q}$; $\boldsymbol{I_{C1} = I_{E1} = I_{C2} = I_{E2}}$; $\boldsymbol{V_{BE}}$**(on) = 0.7 V**, $\boldsymbol{\beta = 120}$, **Early voltage** is **100** for $\boldsymbol{Q_7}$ and $\boldsymbol{Q_{11}}$**;** and $\boldsymbol{v_O = 0}$ when $\boldsymbol{v_1 = v_2 = 0}$.

$\boldsymbol{R_i}$ is the input resistance of the Darlington Pair while $\boldsymbol{R_{L7}}$ is the effective resistance connected between collector of $\boldsymbol{Q_7}$ and signal ground. **Calculate** the small signal **voltage gain of the Darlington Pair (**$\boldsymbol{A_{v2}}$**)** by using the following relationship: **[20 marks]**

$$A_{v2} = \frac{V_{o3}}{V_{b6}} = \frac{\beta(1+\beta)(r_{o7} \parallel R_{L7})}{R_i}$$

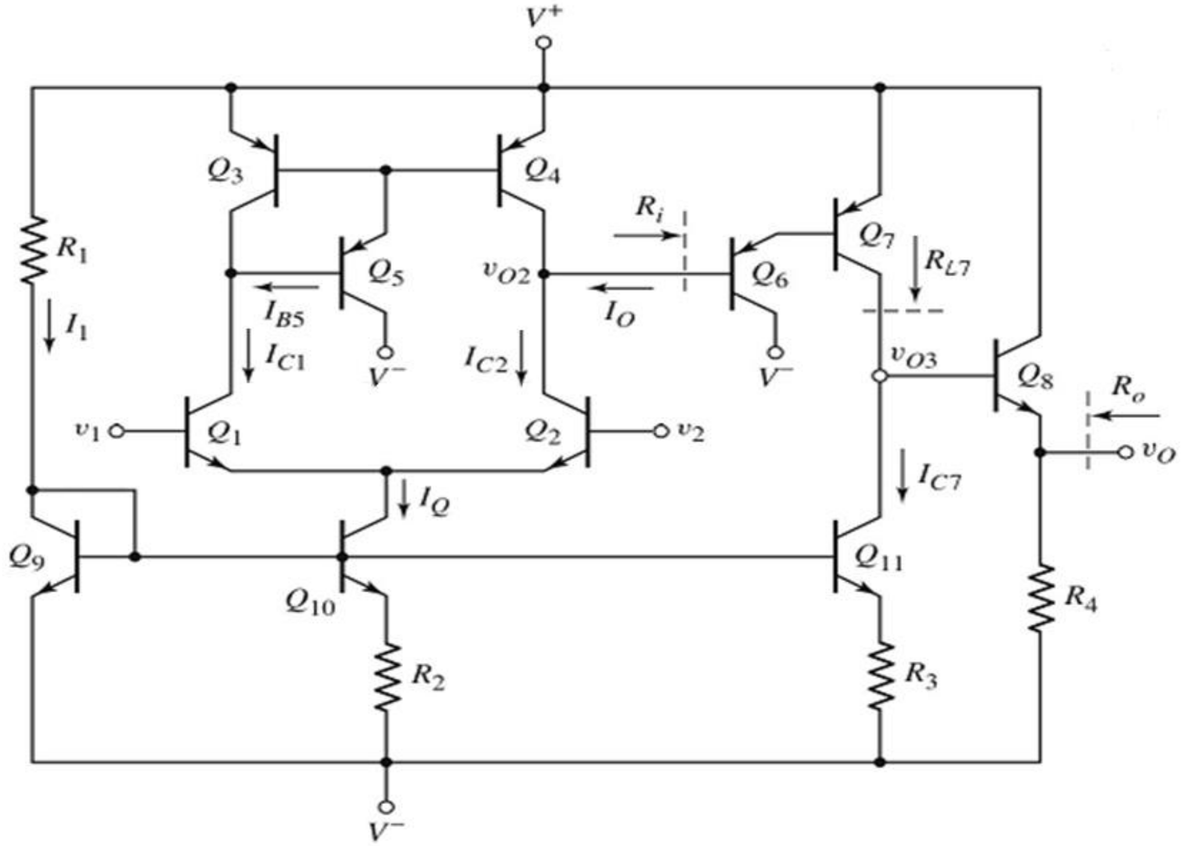


Figure 3

Answers for Question 3

Answers for Question 3 (Continued)

QUESTION 4 [25 marks]

(a) **Draw** a **class-A output stage** constructed using **npn** emitter follower with load R_L and biased by a three-transistor current sinking current source. The overall circuit is connected to supply voltages of $V^+ = +5$ V and $V^- = -5$ V. **[5 marks]**

(b) A **class-AB** output stage with BJTs is shown in **Figure 4**. **Reverse saturation current** for every transistor is $I_S = 2\times10^{-15}$ **A**. Assume $+V_{CC} = +6$ **V** and $-V_{CC} = -6$ **V.** Let $R_L = 1$ **kΩ** and $V_{BB} = 1.40$ **V.** For the case of the output voltage $v_O = -4$ **V:**

(i) **Determine** i_L, i_{Cp}, i_{Cn}, and v_I. **[12 marks]**

(ii) **Calculate** the power dissipated in transistor Q_n and Q_p. **[8 marks]**

Answers for Question 4

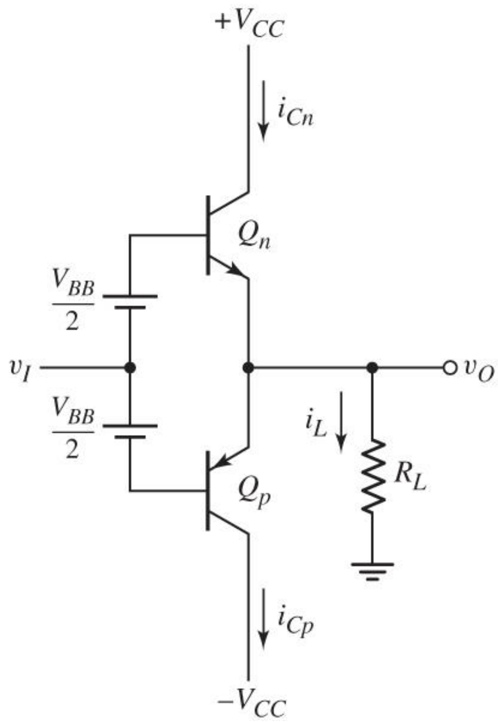


Figure 4

Answers for Question 4 (Continued)

APPENDIX

A) BASIC FORMULA FOR TRANSISTOR

BJT

$$i_C = I_S e^{v_{BE}/V_T} \quad ;\text{NPN}$$

$$i_C = I_S e^{v_{EB}/V_T} \quad ;\text{PNP}$$

$$i_C = \beta i_B = \frac{\beta}{\beta+1} i_E$$

$$i_E = i_B + i_C$$

;Small signal

$$\beta = g_m r_\pi$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

$$V_T = 26\,\text{mV}$$

MOSFET

;N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n[v_{GS} - V_{TN}]^2$$

$$K_n = \frac{\mu_n C_{ox} W}{2L} = \frac{k_n'}{2} \cdot \frac{W}{L}$$

;P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p[v_{SG} + V_{TP}]^2$$

$$K_p = \frac{\mu_p C_{ox} W}{2L} = \frac{k_p'}{2} \cdot \frac{W}{L}$$

;Small signal

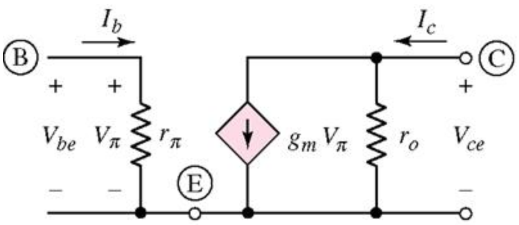
$$g_m = 2\sqrt{K_n I_{DQ}} \quad ;\text{N – MOSFET}$$

$$g_m = 2\sqrt{K_p I_{DQ}} \quad ;\text{P – MOSFET}$$

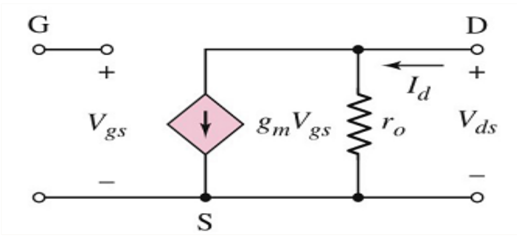
$$r_o \cong \frac{1}{\lambda I_{DQ}}$$

B) HYBRID-π EQUIVALENT CIRCUITS

BJT



MOSFET



C) QUADRATIC FORMULA

$$Ax^2 + Bx + C = 0 \quad \rightarrow \quad x = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$