COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 1 2018 / 2019

PROGRAMME	**: Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	**: EEEB273**
SUBJECT	**: ELECTRONIC ANALYSIS AND DESIGN II**
DATE	**: September 2018**
DURATION	**: 3 hours**

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **FIVE** (5) questions in **NINE** (9) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided. **Use pen** to write your answer.
4. Write answer to different question on **a new page**.

THIS QUESTION PAPER CONSISTS OF NINE* (9) *PRINTED PAGES INCLUDING THIS COVER PAGE.

Question 1 [20 marks]

You are one of the selected candidates to attend an interview carried out at Motorola Semiconductor as Product Engineer. As part of the interview you are given the following task:

> **Design** a BJT Current Source that utilized 4 transistors arranged in cascode mode. All transistors in the circuit are matched. The transistor parameters are: $\boldsymbol{\beta}$ **= 150,** $\boldsymbol{V_A}$ **= 100 V,** and $\boldsymbol{V_{BE}}$**(on) = 0.7 V**. The power supplies: $\boldsymbol{V^+}$ **= 5 V**, $\boldsymbol{V^-}$ **= -5V**. Resistor $\boldsymbol{R_1}$ **= 6 kΩ.**

Determine the followings:

(a) **Draw** the circuit for the current source. **[4 marks]**

(b) **Derive** the relationship between $\boldsymbol{I_O}$ and $\boldsymbol{I_{REF}}$. **[5 marks]**

(c) Based on given value of $\boldsymbol{\beta}$, use approximate value of $\boldsymbol{I_O}$ to **estimate** the output resistance, $\boldsymbol{R_O}$, of the current source. **[7 marks]**

(d) **Find** $\boldsymbol{g_{m4}}$ and $\boldsymbol{r_{\pi 4}}$. **[4 marks]**

Question 2 [20 marks]

(a) The differential amplifier in **Figure 1** has transistor parameters as β **= 100** and V_{BE}**(on) = 0.7 V**. The Early voltage is $V_A = \infty$ for Q_1 and Q_2, and is V_A **= 50 V** for Q_3 and Q_4.

(i) Design the circuit such that I_3 **= 400 μA** and $V_{CE1} = V_{CE2}$ **= 10 V**. **[5 marks]**

(ii) Determine A_d and $CMRR_{dB}$ for a one-sided output at v_{O2}. A_{cm} is given as **−0.113 V/V.** **[5 marks]**

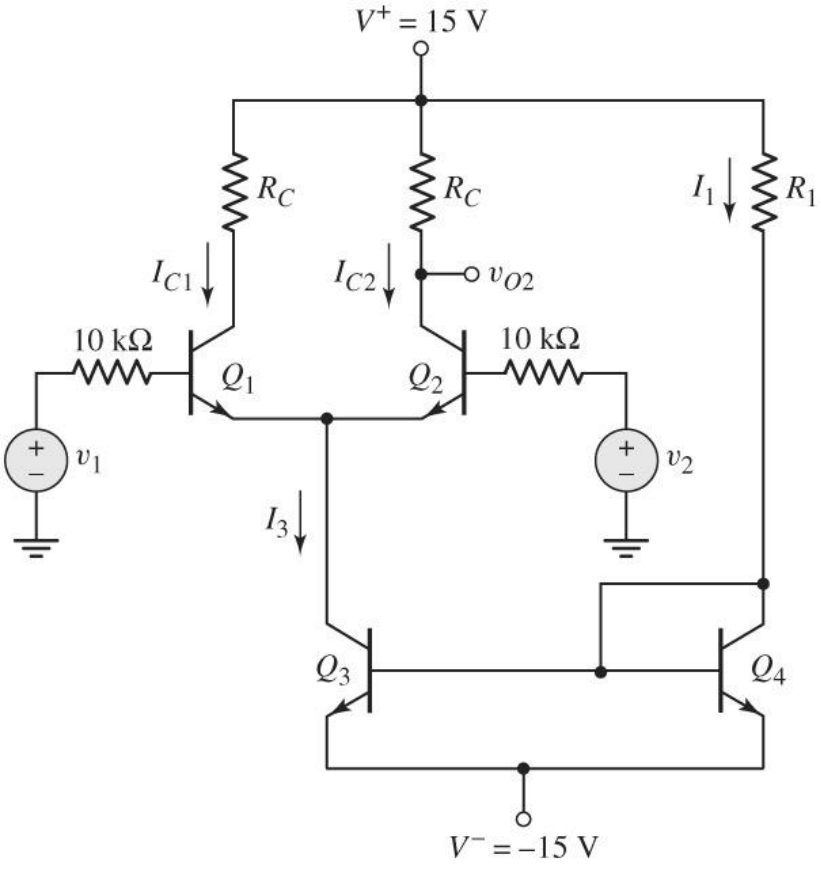

Figure 1

(b) The differential amplifier in **Figure 2** is biased at I_Q **= 0.5 mA.** The transistor parameters are shown in **Table 1**.

Table 1: MOSFET parameters

N-MOSFET transistor	P-MOSFET transistor
K_n **= 0.25 mA/V^2**	K_p **= 0.25 mA/V^2**
V_{TN} **= 0.4 V**	V_{TP} **= −0.4 V**
λ_n **= 0.02 V^{-1}**	λ_p **= 0.02 V^{-1}**

(i) **Draw** an improved diff-amp for the circuit in **Figure 2**. Use **Table 1** for the transistors specification. **[4 marks]**

(ii) **Calculate** the minimum power supply voltages if the common input voltages are to be in the range of $\pm$ **3 V**. Assume symmetrical supply voltages. **[6 marks]**

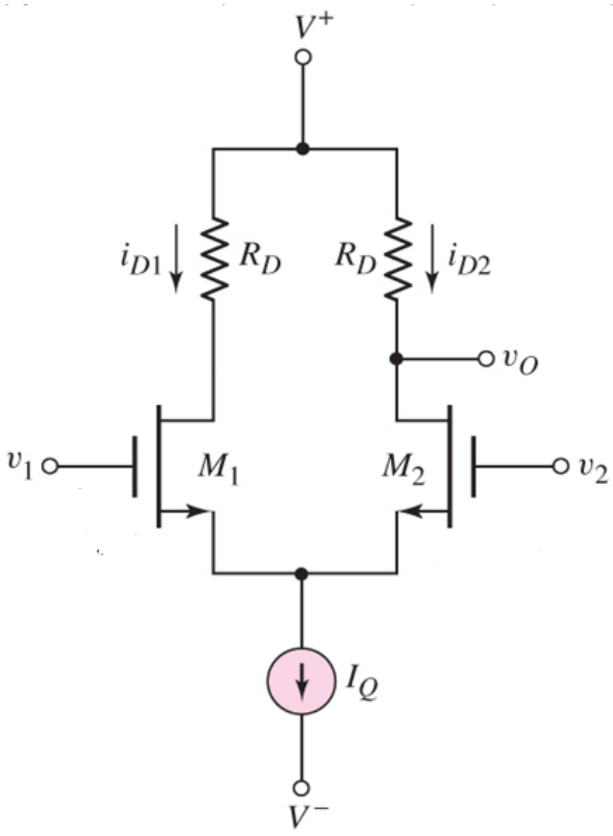

Figure 2

Question 3 [20 marks]

A simple bipolar op-amp is designed as shown in **Figure 3**. *Note that biasing for amplifiers in the circuit is provided by* ***two-transistor current mirrors***. Study the **Figure 3** carefully. Neglect base currents. Assume parameters for all transistors are V_{BE}**(on) = 0.7 V**, β **= 200,** and $V_A = \infty$.

(a) Referring to **Figure 3 calculate** DC values for I_1, I_Q, I_{C2}, v_{O2}, and v_{O3}. **[10 marks]**

(b) With small-signal analysis, values for A_{d1}, $r_{\pi 3}$, and A_{v2} can be found using the following **Equations (3.1) to (3.3),** assuming that $R_{i3} >> R_5$. **Calculate** A_{d1}, A_{v2}, and the total overall small-signal voltage gain, A_d for the bipolar op-amp. **[10 marks]**

$$A_{d1} = \frac{V_{o2}}{v_d} = \frac{g_{m2}}{2}(R_C || R_{i2}) \qquad (3.1)$$

$$r_{\pi 3} \cong \beta r_{\pi 4} \qquad (3.2)$$

$$A_{v2} \cong \frac{I_{R4}}{2V_T}(R_5) \qquad (3.3)$$

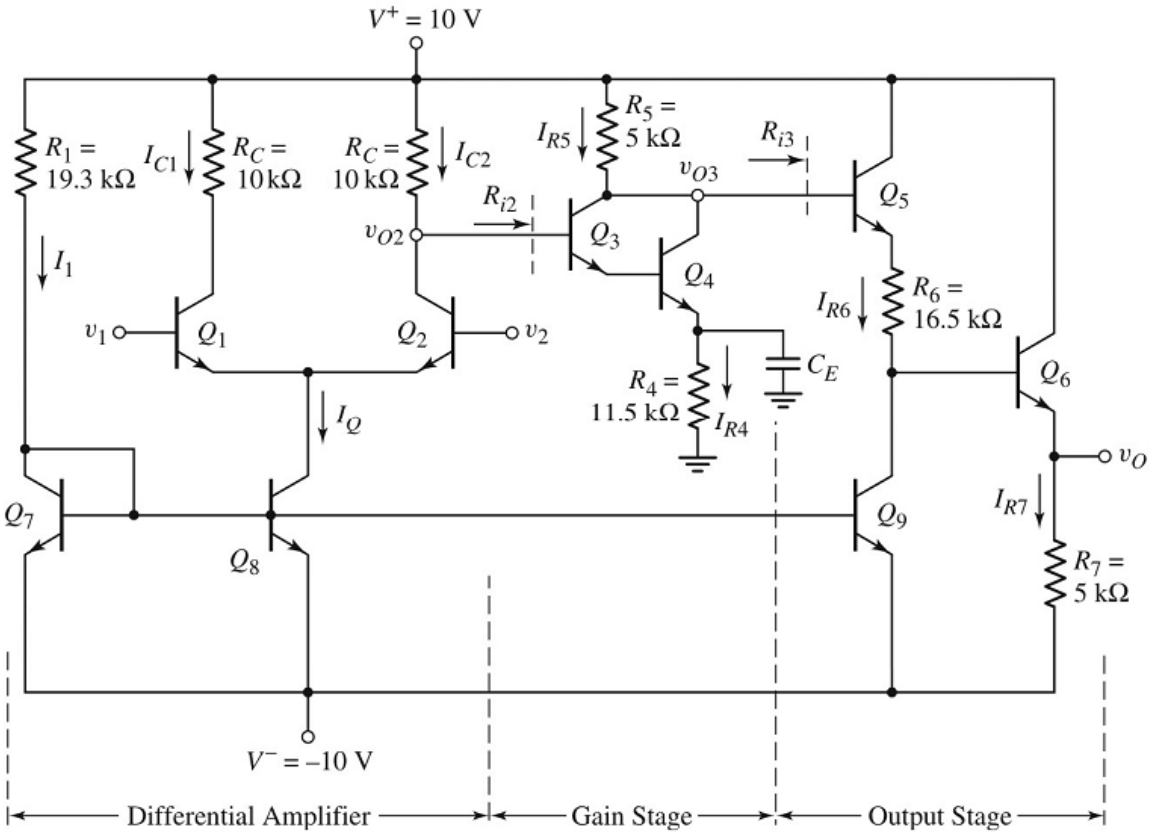

Figure 3

Question 4 [20 marks]

(a) **Figure 4a** and **Figure 4b** show two different designs of output stages.

(i) **Identify** class of the output stages in the **Figure 4a** and **Figure 4b**. **[2 marks]**

(ii) For the output stage circuit in the **Figure 4a** assume the B-E cut-in voltage (i.e. V_{BE} V_{EB}) of **0.6 V** such that v_O remains zero for the interval **-0.6 V** $\leq v_I \leq$ **0.6 V**. **Sketch** the voltage transfer characteristic of the circuit. **Indicate** when Q_n is conducting and when it is not conducting. **[3 marks]**

(iii) For the output stage circuit in the **Figure 4b**, the circuit parameters are V_{CC} **= 12 V**, R_L **= 100 Ω**, and V_{BB} **= 1.2 V**. Q_n and Q_p are matched with I_S **= 4x10^{-13} A** and β **>> 1.** For input voltage v_I **= 0**, **calculate** the quiescent collector currents, i_{Cn} and i_{Cp}. **What** is the maximum amplitude of the output voltage (v_O) and the corresponding maximum power that can be delivered to the load? **[5 marks]**

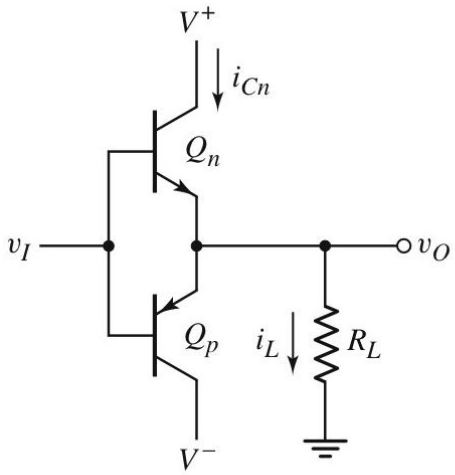

Figure 4a

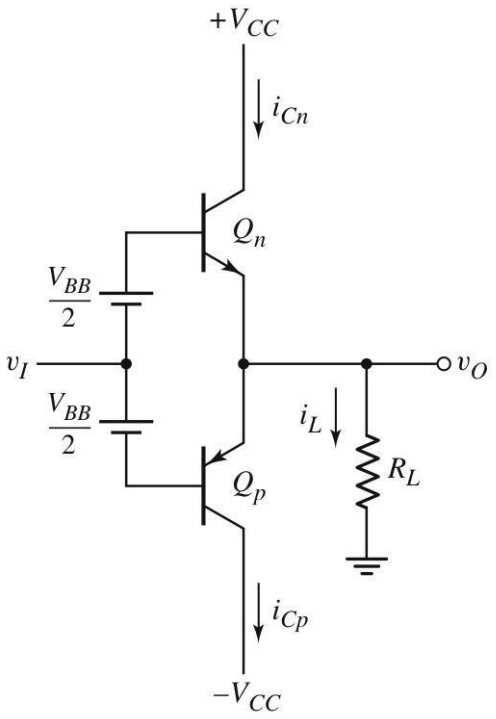

Figure 4b

(b) The **741 op-amp** is shown in **Figure 5.** Assume that V_{BE}**(on) =** V_{EB}**(on) = 0.7 V**, β_n **= 200**, β_p **= 60,** V_{AN} **= 200 V,** and V_{AP} **= 100 V**. The area of transistor Q_{13B} is 75% of transistor Q_{12}. It is given that I_{REF} **=** I_{C12} **= 0.3mA**. Calculate the **small signal input resistance** of the **Gain stage** (i.e. into the base of Q_{16}). **[10 marks]**

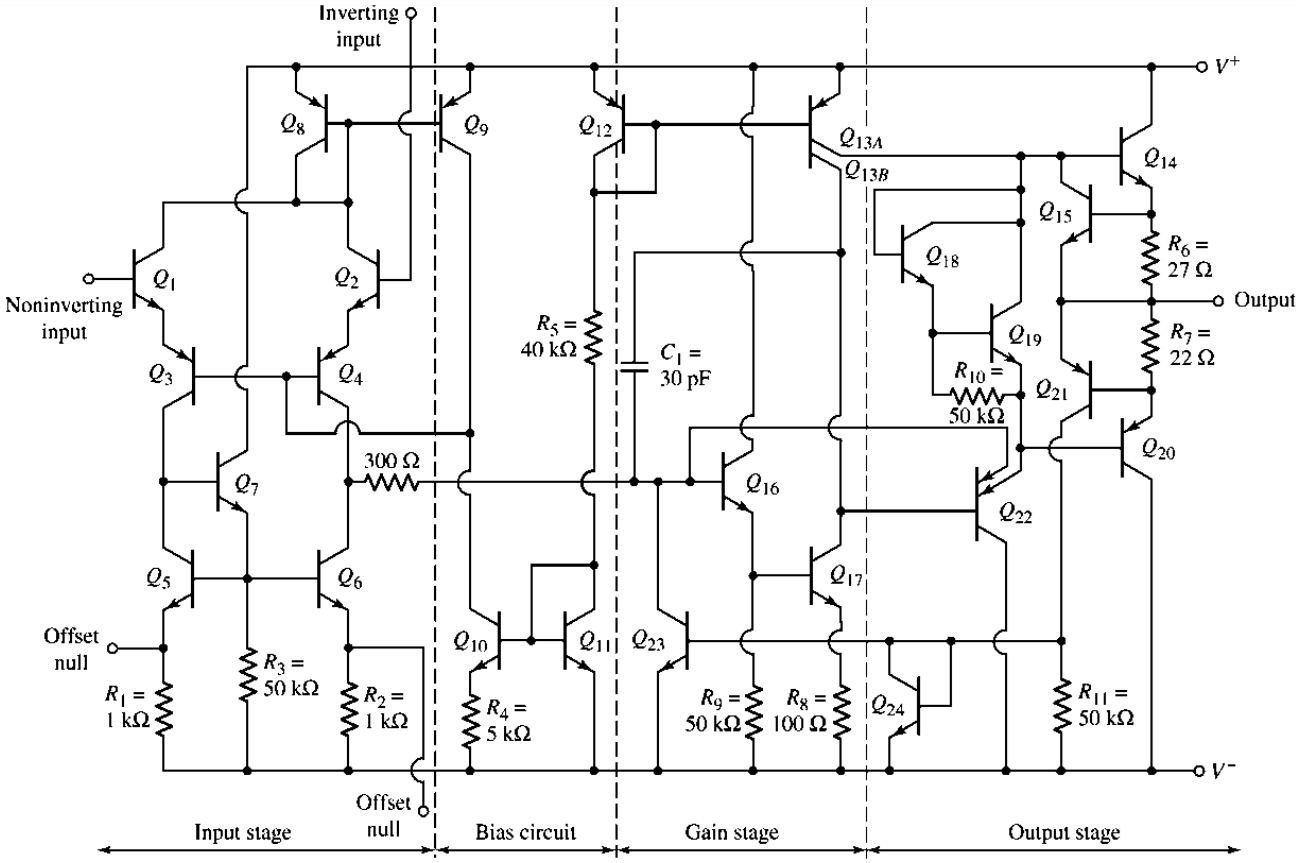

Figure 5

Question 5 [20 marks]

(a) Using **feedback resistor of 20 kΩ**, draw the following circuits using **inverting op-amp configuration:**

(i) An **inverting amplifier** with a **closed-loop gain of -10**. **[3 marks]**

(ii) **A voltage follower**. **[5 marks]**

(b) A general output equation for a **difference amplifier** shown in **Figure 6** is:

$$v_o = A_d v_d + A_{cm} v_{cm}$$

For the difference amplifier in the **Figure 6**, the circuit parameters are $\boldsymbol{R_1}$ **= 20 kΩ**, $\boldsymbol{R_2}$ **= 80 kΩ**, $\boldsymbol{R_3}$ **= 20 kΩ**, and $\boldsymbol{R_4}$ **= 85 kΩ** and the output voltage ($\boldsymbol{v_O}$) equation is as follows:

$$v_o = \left[1 + \frac{R_2}{R_1}\right]\left[\frac{R_4/R_3}{1 + R_4/R_3}\right] v_{I2} - \frac{R_2}{R_1} v_{I1}$$

where $v_{I1} = v_{cm} + \frac{v_d}{2}$ and $v_{I2} = v_{cm} - \frac{v_d}{2}$

Calculate **the differential-mode gain ($\boldsymbol{A_d}$)**, **common-mode gain ($\boldsymbol{A_{cm}}$)**, and **the common-mode rejection ratio (*CMRR*) in dB** for the circuit. **[12 marks]**

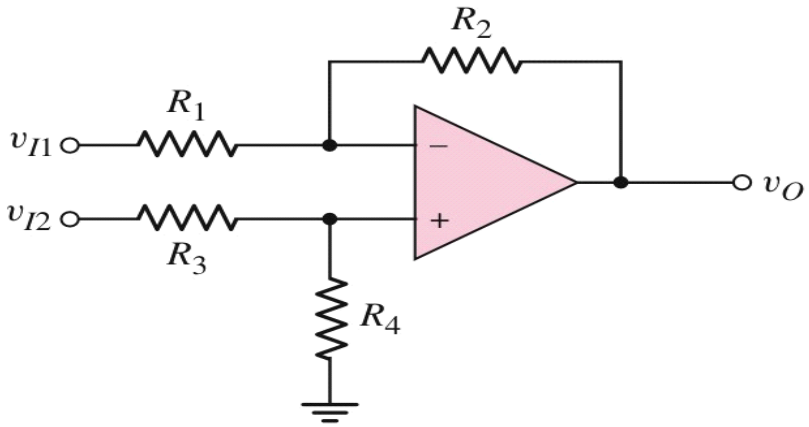

Figure 6

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APPENDIX:

A) BASIC FORMULA FOR TRANSISTOR

BJT

$$i_C = I_S e^{v_{BE}/V_T} \quad ;\text{NPN}$$

$$i_C = I_S e^{v_{EB}/V_T} \quad ;\text{PNP}$$

$$i_C = \beta i_B = \frac{\beta}{\beta+1} i_E$$

$$i_E = i_B + i_C$$

;Small signal

$$\beta = g_m r_\pi$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

$$V_T = 26\,\text{mV}$$

MOSFET

$$;\text{N}-\text{MOSFET}$$

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n[v_{GS} - V_{TN}]^2$$

$$K_n = \frac{\mu_n C_{ox} W}{2L} = \frac{k_n'}{2} \cdot \frac{W}{L}$$

$$;\text{P}-\text{MOSFET}$$

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p[v_{SG} + V_{TP}]^2$$

$$K_p = \frac{\mu_p C_{ox} W}{2L} = \frac{k_p'}{2} \cdot \frac{W}{L}$$

;Small signal

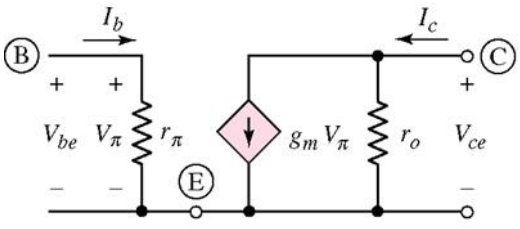
$$g_m = 2\sqrt{K_n I_{DQ}} \quad ;\text{N}-\text{MOSFET}$$

$$g_m = 2\sqrt{K_p I_{DQ}} \quad ;\text{P}-\text{MOSFET}$$

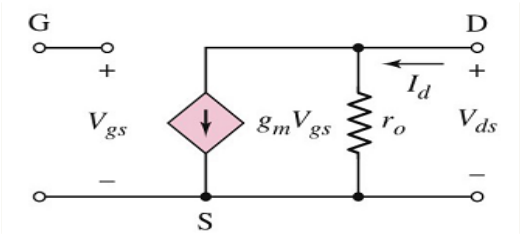
$$r_o \cong \frac{1}{\lambda I_{DQ}}$$

B) HYBRID-π EQUIVALENT CIRCUITS

BJT



MOSFET



C) QUADRATIC FORMULA

$$Ax^2 + Bx + C = 0 \qquad \rightarrow \quad x = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$