Name:
Student ID Number:
Section Number: 01/02/03/04 A/B
Lecturer: Dr Jamaludin/ Dr Fazrena Azlee/ Dr Jehana Ermy/ Prof Md Zaini
Table Number:

UNIVERSITI TENAGA NASIONAL

The National Energy University

College of Engineering

Department of Electronics and Communication Engineering

Test 2

SEMESTER 1, ACADEMIC YEAR 2018/2019

Subject Code	:	**EEEB273**
Course Title	:	**Electronics Analysis & Design II**
Date	:	**11 August 2018**
Duration	:	**2 hours**

Instructions to the candidates:

1. Write your **Name** and **Student ID Number**. Indicate your **Section Number** and **Lecturer**'s Name. Write also your **Table Number**.
2. **Write all your answers using pen**. **DO NOT USE PENCIL** except for the diagram.
3. **ANSWER ALL QUESTIONS. Show clearly** all your calculations. Every value **must** be written with its correct Unit.
4. **WRITE YOUR ANSWER ON THIS QUESTION PAPER.**

NOTE: DO NOT OPEN THE QUESTION PAPER UNTIL INSTRUCTED TO DO SO.

☺ **GOOD LUCK!** ☺

Question Number	Q1a	Q1bc	Q2a	Q2b	Q3a	Q3b	Q4a	Q4b	Total
Marks									

BASIC FORMULA FOR TRANSISTOR

BJT

$i_C = I_S e^{v_{BE}/V_T}$; npn

$i_C = I_S e^{v_{EB}/V_T}$; pnp

$i_C = \alpha i_E = \beta i_B$

$i_E = i_B + i_C$

$\alpha = \dfrac{\beta}{\beta + 1}$

; Small signal

$\beta = g_m r_\pi$

$g_m = \dfrac{I_{CQ}}{V_T}$

$r_\pi = \dfrac{\beta V_T}{I_{CQ}}$

$r_o = \dfrac{V_A}{I_{CQ}}$

$V_T = 26\,\text{mV}$

MOSFET

; N – MOSFET

$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$

$i_D = K_n[v_{GS} - V_{TN}]^2$

$K_n = \dfrac{k_n'}{2} \cdot \dfrac{W}{L}$

; P – MOSFET

$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$

$i_D = K_p[v_{SG} + V_{TP}]^2$

$K_p = \dfrac{k_p'}{2} \cdot \dfrac{W}{L}$

; Small signal

$g_m = 2\sqrt{K_n I_{DQ}}$; N - MOSFET

$g_m = 2\sqrt{K_p I_{DQ}}$; P - MOSFET

$r_o \cong \dfrac{1}{\lambda I_{DQ}}$

Quadratic formula :

$$Ax^2 + Bx + C = 0 \quad \rightarrow \quad x = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$

This is extra page for answers. Please indicate question number clearly.

QUESTION 1 [20 marks]

The differential amplifier with active load shown in **Figure 1** has a pair of **pnp bipolar differential amplifier** as input devices and a pair of **npn bipolar connected as an active load**. The circuit bias is $\boldsymbol{I_Q}$ = **0.15 mA**, and the transistor parameters are $\boldsymbol{\beta}$ **= 100**, and $\boldsymbol{V_A}$ **= 100 V**.

(a) **Draw** the active load circuit to complete the circuit in **Figure 1**. [6 marks]

(b) **Find** the open-circuit differential-mode voltage gain, $\boldsymbol{A_d}$. [8 marks]

(c) **Calculate** the value of a load resistance $\boldsymbol{R_L}$ connected to the output $\boldsymbol{v_O}$ if the differential mode voltage gain $\boldsymbol{A_d}$ is to be reduced to **524 V/V**. [6 marks]

Answers for Question 1

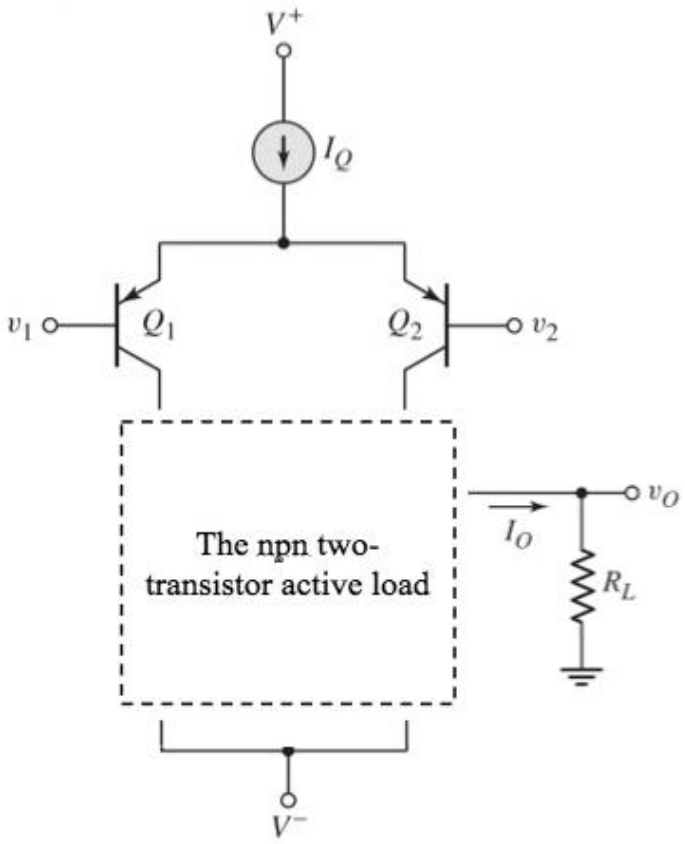

Figure 1

Answers for Question 1 (Continued)

QUESTION 2 [35 marks]

(a) **Draw** a **PMOS** differential amplifier, M_1 and M_2, with an active load of two-transistor current source, M_3 and M_4. **Label** them clearly with $V^+ = 10$ **V** and $V- = -10$ **V**.

[15 marks]

(b) Consider the drawn figure in **part (a)**. The transistors parameters are $V_{TN} = 1$ **V**, $K_n = 90$ **μA/V²**, $\lambda_n = 0.02$ **V⁻¹**, $V_{TP} = -1$ **V**, $K_p = 60$ **A/V²**, $\lambda_p = 0.01$ **V⁻¹**, and $I_Q = 0.4$ **mA**. Assume that the differential amplifier transistors M_1 and M_2, and active load transistors M_3 and M_4 are identical.

(i) **Calculate** the output resistance, R_O, of the differential amplifier. [5 marks]

(ii) **Determine** the differential-mode gain, A_d. [5 marks]

(iii) **Find** the output voltage, v_O, if the differential input voltage is $v_d = 20 \sin(\omega t)$ **V**. [5 marks]

(iv) **What will happen** to the differential amplifier gain if the active load is changed to **cascode** current source? [5 marks]

Answers for Question 2

Answers for Question 2 (Continued)

QUESTION 3 [20 marks]

Consider a **multistage amplifier** shown in **Figure 2**. ***Take note that one PNP two-transistor current source is used as active load for a differential amplifier***. ***Two other NPN two-transistor current sources are used to bias the differential amplifier and a Darlington Pair respectively.***

Given values of V^+ **= 10 V,** $V-$ **= −10 V,** I_Q = **0.307 mA,** and R_2 **= 5 kΩ**. Assume β **= 120** for all transistors; **Early voltage** (V_A) for Q_7 and Q_{11} is **100 V**; saturation current (I_S) for Q_7 and Q_{11} is higher than other transistors; $I_{C7} = I_{C11}$; and output voltage v_O **= 0** when inputs $v_1 = v_2$ **= 0**.

(a) **Show** that $I_O = I_Q / \beta$ when the DC currents in the differential amplifier are **balanced (i.e.** $I_O = I_{B3} + I_{B4}$**)** by assuming that base currents for transistors in the differential amplifier and I_O are small. Then **determine** the value of I_O in the **Figure 2**.

[5 marks]

(b) In the **Figure 2** also, R_i is the input resistance of the **Darlington Pair** and R_{L7} is the effective resistance connected between collector of Q_7 and signal ground. **Calculate** the small signal **voltage gain of the Darlington Pair (**A_{v2}**)** by using the following relationship

$$A_{v2} = \frac{v_{O3}}{v_{O2}} = \frac{\beta(1+\beta)(r_{o7} || R_{L7})}{R_i}$$ [15 marks]

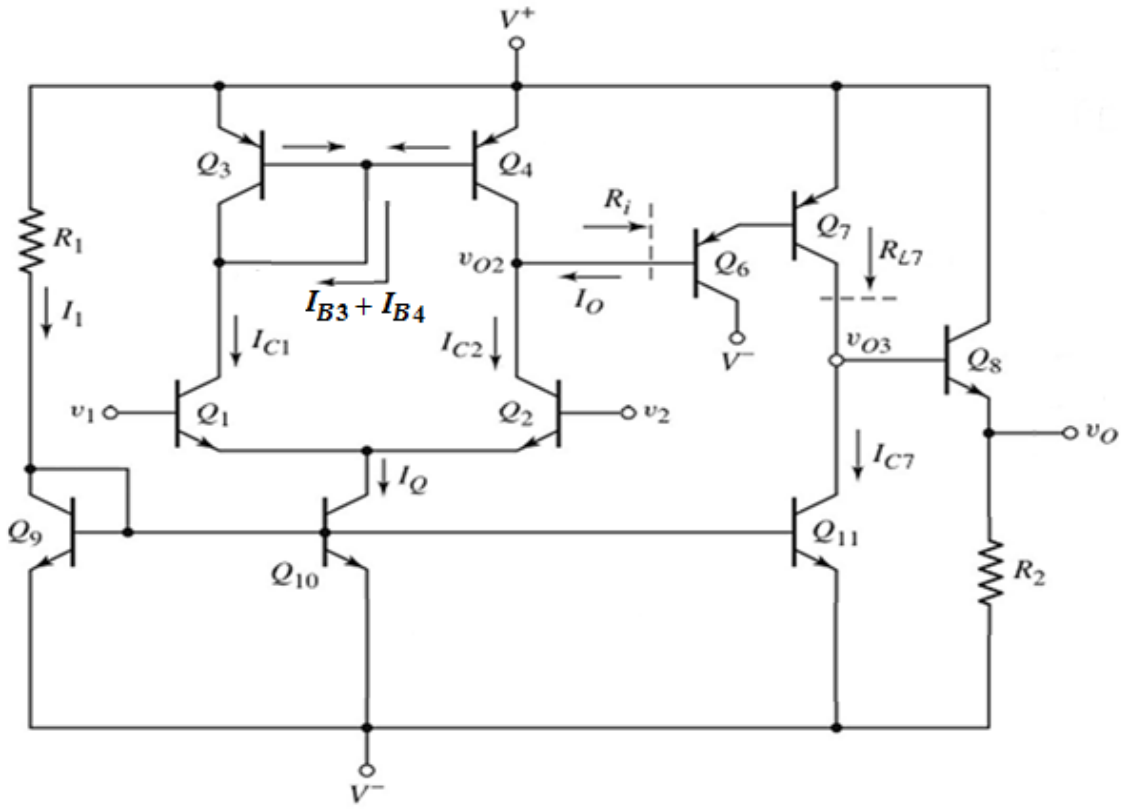

Figure 2

Answers for Question 3

QUESTION 4 [25 marks]

(a) Briefly **explain** the **classification** of the output stage of **Class-A**, **Class-B** and **Class-AB** by **sketching** the waveform of the relevant transistor current, i_c. [5 marks]

(b) A **Class-A** output stage circuit using BJTs is shown in **Figure 3**. For the circuit, V_{CC} **= 10 V**, V_{bias} **= 2 V**, and R_L **= 1 kΩ.** Assume all the transistors are matched with V_{BE}**(on) = 0.65 V**, V_{CE}**(sat) = 0.3 V**, and $V_A = \infty$**. Neglect the base currents**.

(i) **Calculate** the value of I_Q to allow the largest possible output voltage swing. What is the value of resistor R? [10 marks]

(ii) **Calculate** the power conversion efficiency (η) of this circuit. [7 marks]

(iii) **Calculate** the power dissipation in the **emitter follower transistor** Q_1 when output voltage V_O **= 5 V.** [3 marks]

Answers for Question 4

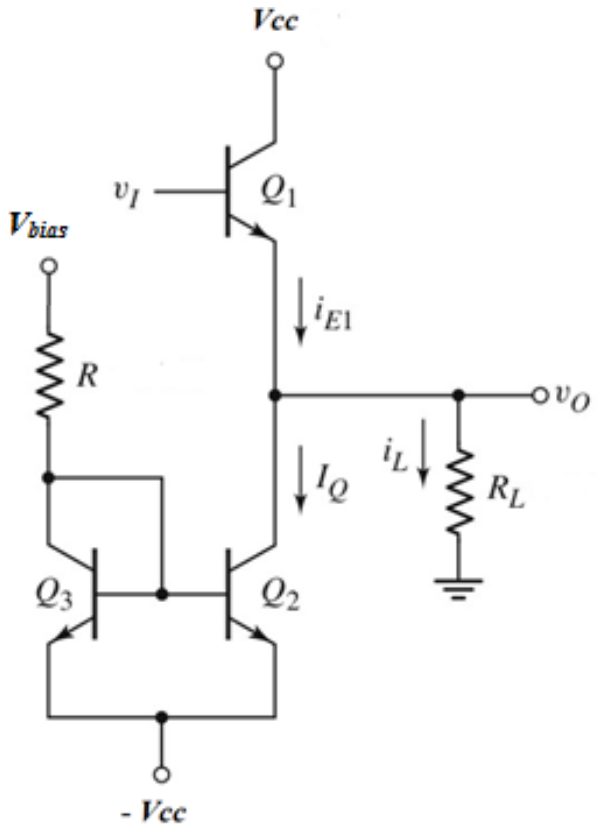

Figure 3

Answers for Question 4 (Continued)

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