COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 2 2018 / 2019

PROGRAMME	: **Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	: **EEEB273/EEEB2014**
SUBJECT	: **ELECTRONIC ANALYSIS AND DESIGN II**
DATE	: **January/February 2019**
TIME	: **3 hours**

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **FIVE** (5) questions in **TEN** (10) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided. **Use pen** to write your answer.
4. Write answer to different question on **a new page**.

THIS QUESTION PAPER CONSISTS OF TEN* (10) *PRINTED PAGES INCLUDING THIS COVER PAGE.

<u>Question 1 [20 marks]</u>

(a) An **npn** current source is shown in **Figure 1**. The transistor parameters are $\boldsymbol{\beta}$ **= 200,** $\boldsymbol{V_{BE}}$**(on) = 0.7 V,** and $\boldsymbol{V_A}$ **= 250 V**. The required **output current** is **20** μ**A** and the **reference current** is **0.5 mA**. **Calculate** the percentage change in output current $\boldsymbol{I_O}$ when $\boldsymbol{V_{C2}}$ changes from **0.9 to 5 V**. **[8 marks]**

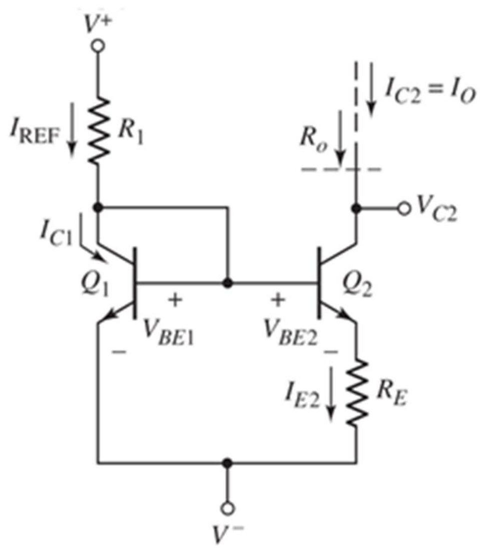


Figure 1

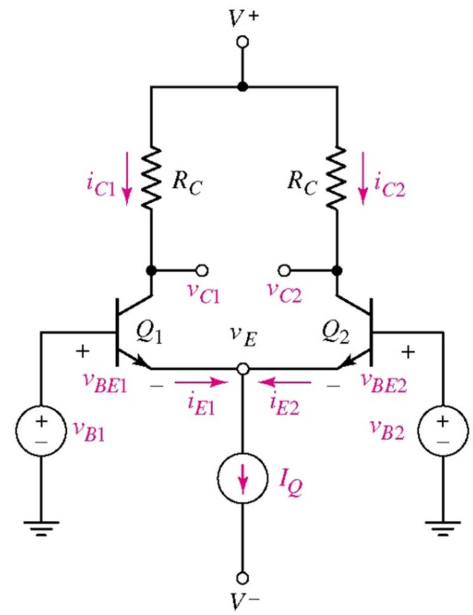


Figure 2

(b) A **BJT differential amplifier** with passive load is shown in **Figure 2**. The power supplies are V^+ **= 5 V** and V^- **= -5 V**. **Draw** a **pnp** version of the circuit. **[4 marks]**

(c) For the **pnp** differential amplifier drawn in **part (b)**, the value of $\boldsymbol{I_Q}$ = **0.5 mA**. It is required that when $\boldsymbol{v_{B1}} = \boldsymbol{v_{B2}}$ **= 0 V**, the voltage $\boldsymbol{V_{EC1}} = \boldsymbol{V_{EB}}$**(on) = 0.7 V**. Let $\boldsymbol{\beta}$ **= 200** and $\boldsymbol{V_A} = \infty$ and **neglect the base currents**. **Calculate** the maximum value of load resistance $\boldsymbol{R_C}$ for this condition and the one-sided differential gain, $\boldsymbol{A_d}$. **[8 marks]**

Question 2 [20 marks]

Figure 3 shows an **N-MOSFET differential amplifier** with passive load. The differential amplifier is biased by an **N-MOSFET current source** constructed by using M_3, M_4, and M_5 that produces the bias current I_Q = **0.20 mA**. Study the **Figure 3** carefully. The overall circuit is powered by V^+ **= 5 V** and V^- **= –5 V**, with R_D **= 40 kΩ**. ***Take note that different values of parameters for MOSFET transistors are used in part (a) and part (c) of this*** **Question 2.**

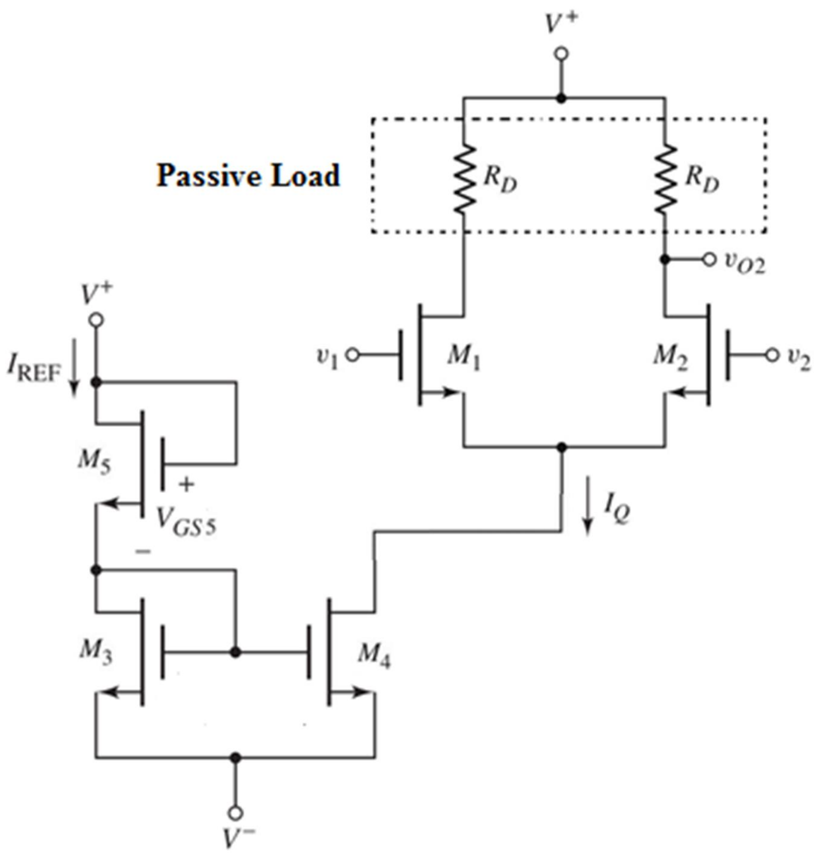


Figure 3

(a) For the **N-MOSFET current source** bias circuit in the **Figure 3** the transistors parameters are V_{TN} **= 0.5 V**, k'_n **= 50** μ**A/V**^{2}, $(W/L)_3$ = $(W/L)_4$ **= 15**, $(W/L)_5$ **= 3**, and λ_n **= 0**. **Calculate** the value of V_{GS5}. **[5 marks]**

(b) The differential amplifier with passive load shown in **Figure 3** is to be redesigned to increase its differential-mode voltage gain (A_d) by replacing its passive load (R_D) with an active load constructed using a **P-MOSFET Cascode current source**. **Draw the new**

circuit for the differential amplifier incorporating the **active load's full circuit diagram**. Label the new circuit correctly and clearly with appropriate symbols and numbering for the **P-MOSFET** transistors used in the new circuit starts from M_7. You are **NOT** required to draw the **N-MOSFET** current source that biased the differential amplifier in the **Figure 3**. **[5 marks]**

(c) For the differential amplifier circuit in the **Figure 3** and the new circuit with **P-MOSFET** active load in **part (b)**, assume that **N-MOSFET** and **P-MOSFET** devices are available with parameters shown in **Table 1**. For the circuit in **Figure 3**, given R_D **= 40 kΩ**. **Determine** how much the **differential-mode voltage gain** (A_d) of the differential amplifier had increased when the active load is used to replace the passive load in the differential amplifier in **Figure 3.** **[10 marks]**

Table 1: MOSFET parameters

N-MOSFET transistor	**P-MOSFET** transistor
K_n = 0.4 mA/V^2	K_p = 0.2 mA/V^2
V_{TN} = 0.5 V	V_{TP} = −1 V
λ_n = 0.02 V^{-1}	λ_p = 0.02 V^{-1}

Question 3 [20 marks]

(a) For circuit in **Figure 4**, given that $\boldsymbol{I_{C2} = 1.2}$ **mA**, $\boldsymbol{I_{C3} = 5}$ **mA**, $\boldsymbol{R_1 = 50}$ **kΩ**, and $\boldsymbol{R_2 = 5}$ **kΩ. Determine** the **input resistance** (**R_i**) and **output resistance** (**R_o**) of the circuit. Let the transistor parameters β = **60** and $V_A = \infty$. **[10 marks]**

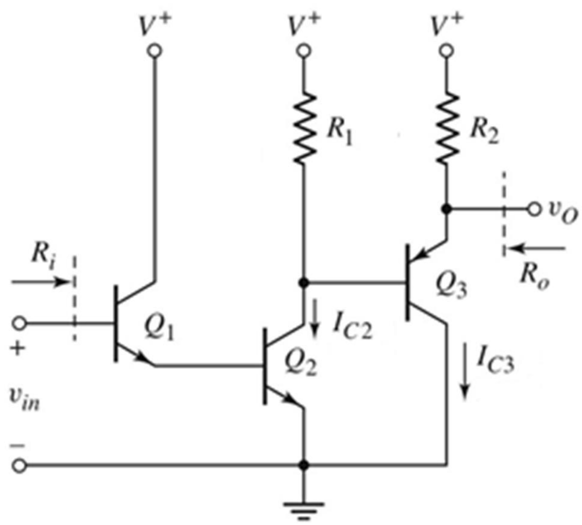


Figure 4

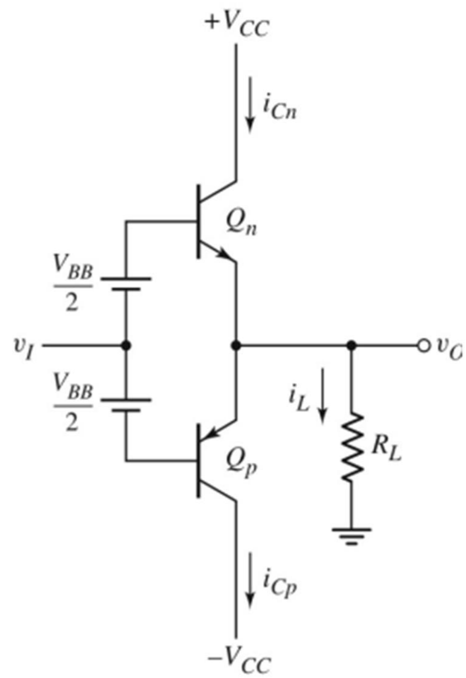


Figure 5

(b) **Compare and contrast** the Class-A with Class-B, Class-B with Class-AB, and Class-A with Class-AB output stages, **respectively**. **[2 marks]**

(c) For the **Class-AB** output stage given in **Figure 5**, V_{CC} **= 10 V**, V_{BB} **= 1.35 V**, R_L **= 100 Ω**, and for the transistors $I_S = 10^{-13}$ **A**. For an output voltage v_O **= 5 V**, **calculate** i_{cn}, i_{cp} and the power dissipated in both Q_n and Q_p transistors. **[8 marks]**

<u>Question 4 [20 marks]</u>

(a) **Consider** the bias circuit portion of the **741 op-amp** in **Figure 6**. Assume that the transistor parameters of $I_S = 5 \times 10^{-16}$ **A.** The bias voltages are given as $\pm$ **15 V**. **Neglect** the base currents.

- **(i)** **Redesign** the bias circuit to obtain $I_{REF} = 0.4$ **mA** and $I_{C10} = 40\ \mu$A. **[4 marks]**
- **(ii)** **Determine** the values of V_{EB12}, V_{BE11}, and V_{BE10}. **[6 marks]**

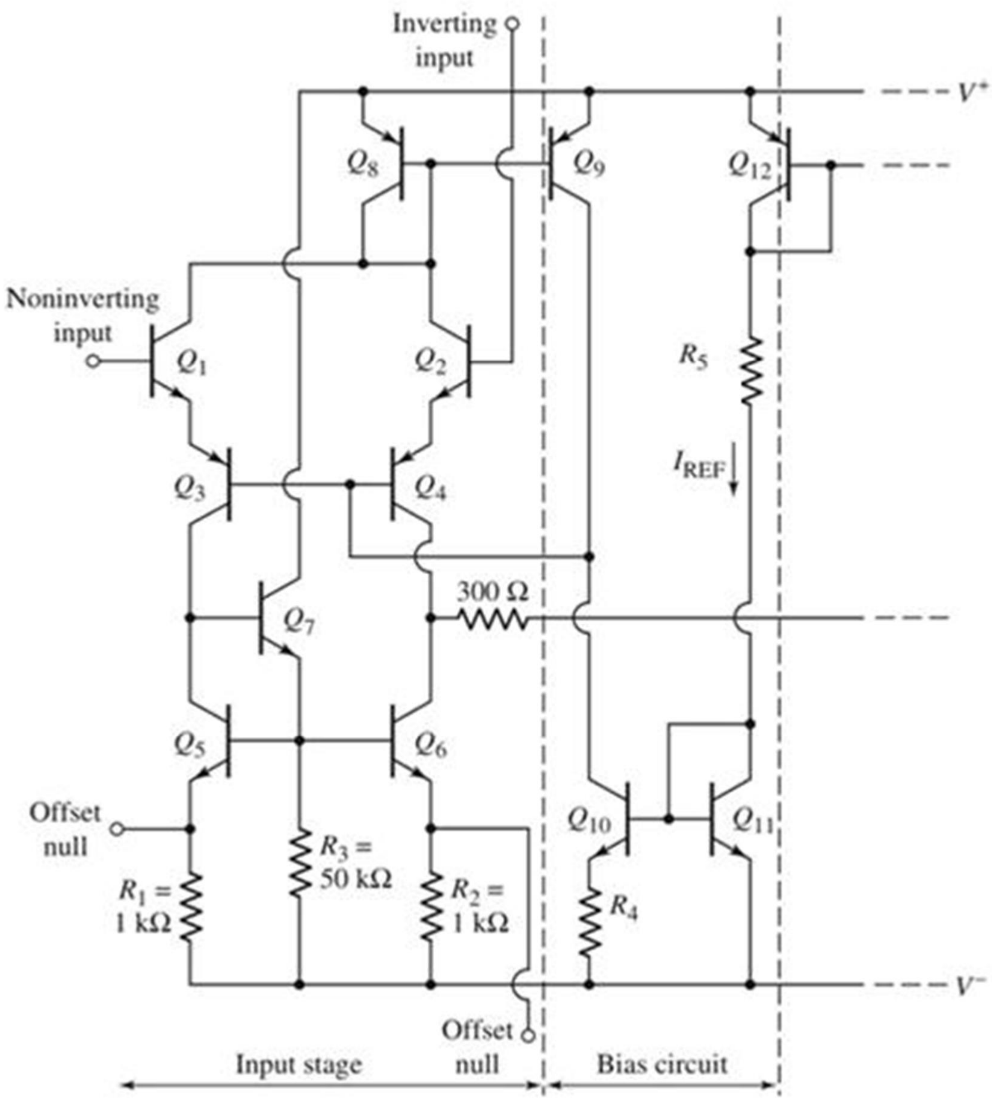


Figure 6

(b) Consider the **MC14573** op-amp in **Figure 7.** Assume transistor parameters of V_{TN} **= 0.5 V**, V_{TP} **= -0.5 V**, K_n **= 125 µA/V²**, K_p **= 100 µA/V²**, λ_n **= 0.01 V⁻¹**, and λ_p **= 0.02 V⁻¹**. Given that bias current for differential amplifier is I_Q **= 0.1 mA**.

Determine the **overall small signal differential-mode voltage gain** for the **MC14573** op-amp in the **Figure 7**. Value for gain of the output stage consists of transistor M_7 and M_8 is given by equation $A_{v2} = g_{m7}(r_{o7} \| r_{o8})$. **[10 marks]**

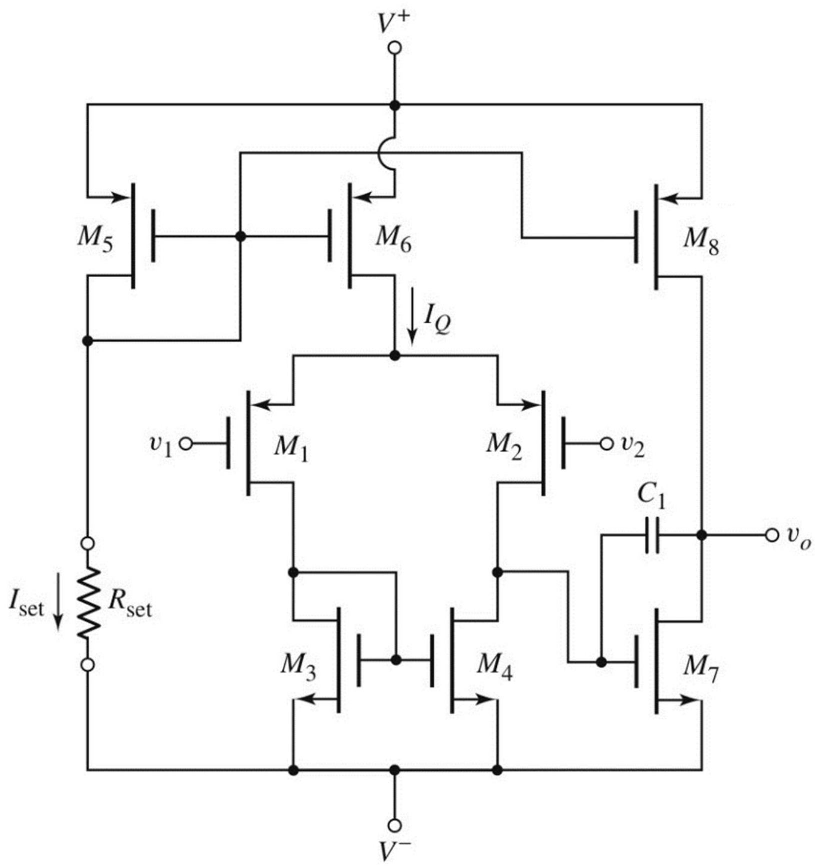


Figure 7

<u>Question 5 [20 marks]</u>

(a) The equivalent circuit of an ideal operational amplifier (**op-amp**) is given in **Figure 8.**

(i) **Explain** why the op-amp input currents are zero. **[1 mark]**

(ii) **Explain** the **'virtual short'** concept for the ideal op-amp. **[3 marks]**

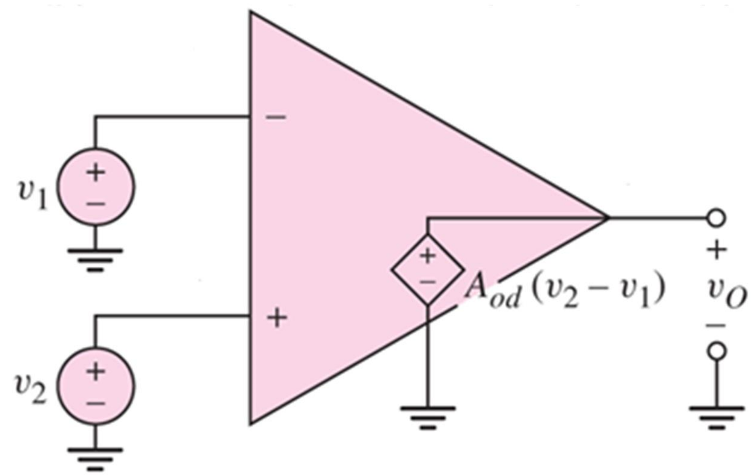


Figure 8

(b) **Figure 9** shows a cascade circuit implemented using ideal op-amps. **Determine** the voltages v_O, v_{O1} and v_{O2}. Given $R = 10\ k\Omega$, $R_1 = 20\ k\Omega$, $R_2 = 30\ k\Omega$, and $v_I = 1\ mV$.

[4 marks]

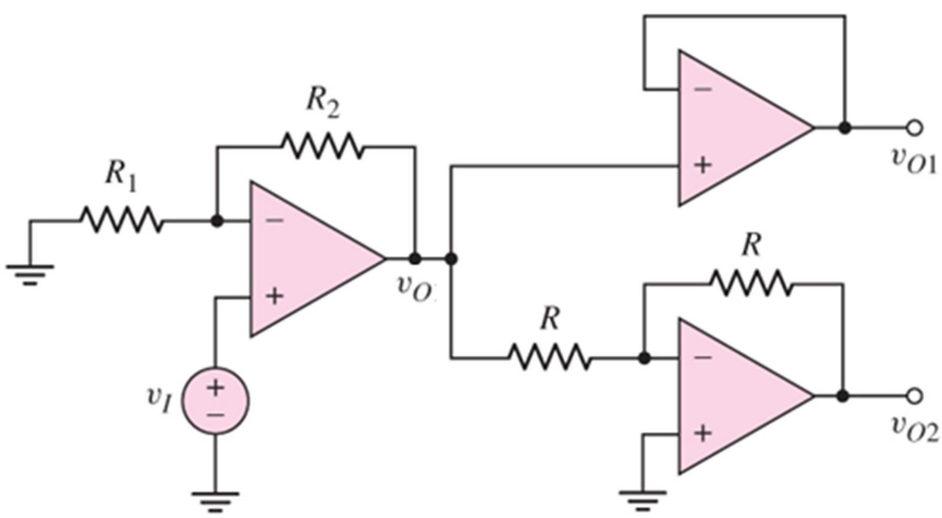


Figure 9

(c) Refer to the **instrumentation amplifier** in **Figure 10**. With proper analysis using ideal operational amplifier characteristics, it can be found that:

$$v_O = \frac{R_4}{R_3}\left(1+\frac{2R_2}{R_1}\right)(v_{I2} - v_{I1})$$

Resistor $\boldsymbol{R_1}$ is such that it consists of a **fixed resistor** $\boldsymbol{R_{1f}}$ **in series with a potentiometer** $\boldsymbol{R_{1v}}$. **Design** the circuit such that the **differential gain varies between 10 to 500 V/V**. Set the difference amplifier gain to **4**. The maximum current in $\boldsymbol{R_1}$ is limited to **10 μA** for a maximum output voltage of **5 V**. What value of potentiometer ($\boldsymbol{R_{1v}}$) is required?

[12 marks]

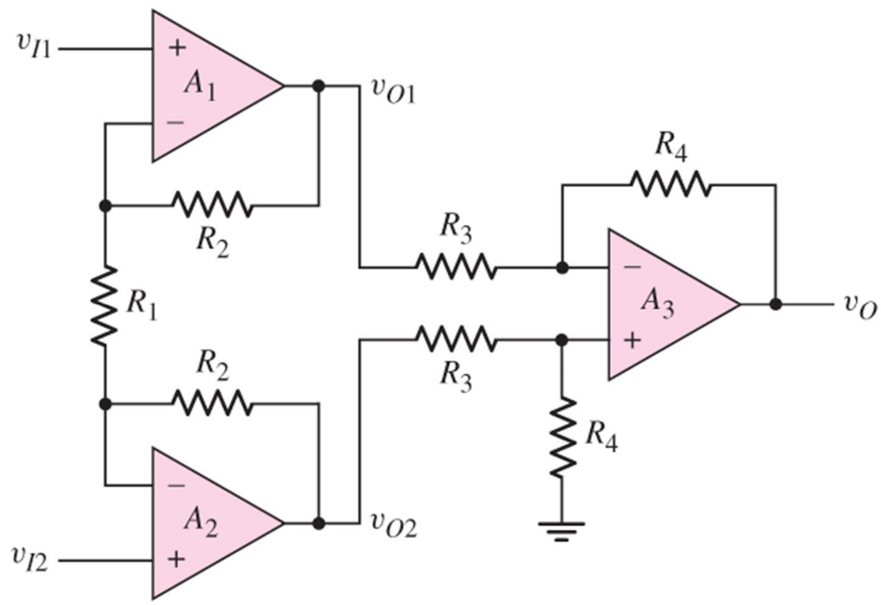


Figure 10

-END OF QUESTION PAPER-

APPENDIX:

A) <u>BASIC FORMULA FOR TRANSISTOR</u>

<u>BJT</u>

$$i_C = I_S e^{v_{BE}/V_T} \quad ;\text{NPN}$$

$$i_C = I_S e^{v_{EB}/V_T} \quad ;\text{PNP}$$

$$i_C = \beta i_B = \frac{\beta}{\beta+1} i_E$$

$$i_E = i_B + i_C$$

;Small signal

$$\beta = g_m r_\pi$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

$$V_T = 26\,\text{mV}$$

<u>MOSFET</u>

;N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n[v_{GS} - V_{TN}]^2$$

$$K_n = \frac{\mu_n C_{ox} W}{2L} = \frac{k_n'}{2} \cdot \frac{W}{L}$$

;P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p[v_{SG} + V_{TP}]^2$$

$$K_p = \frac{\mu_p C_{ox} W}{2L} = \frac{k_p'}{2} \cdot \frac{W}{L}$$

;Small signal

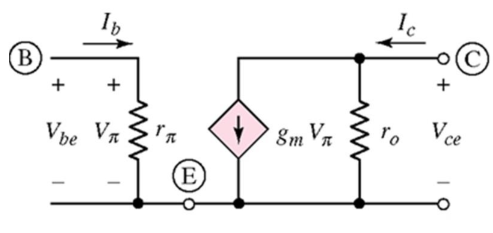
$$g_m = 2\sqrt{K_n I_{DQ}} \quad ;\text{N – MOSFET}$$

$$g_m = 2\sqrt{K_p I_{DQ}} \quad ;\text{P – MOSFET}$$

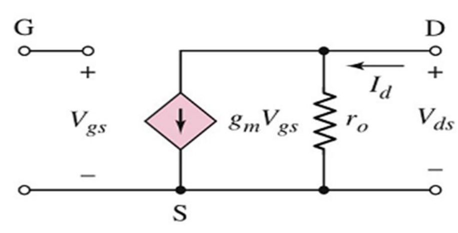
$$r_o \cong \frac{1}{\lambda I_{DQ}}$$

B) <u>HYBRID-´ EQUIVALENT CIRCUITS</u>

<u>BJT</u>



<u>MOSFET</u>



C) <u>QUADRATIC FORMULA</u>

$$Ax^2 + Bx + C = 0 \qquad \rightarrow \qquad x = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$