Name:

Student ID Number:

Section Number: 01/02/03/04 A/B

Lecturer: Dr Jamaludin/ Dr Fazrena Azlee

Table Number:

UNIVERSITI TENAGA NASIONAL

The National Energy University

College of Engineering

Department of Electronics and Communication Engineering

Test 2

SEMESTER 2, ACADEMIC YEAR 2018/2019

Subject Code	:	**EEEB273/EEEB2014**
Course Title	:	**Electronics Analysis & Design II**
Date	:	**5 January 2019**
Duration	:	**2 hours**

Instructions to the candidates:

1. Write your **Name** and **Student ID Number**. Indicate your **Section Number** and **Lecturer's Name**. Write also your **Table Number**.
2. **Write all your answers using pen**. **DO NOT USE PENCIL** except for the diagram.
3. **ANSWER ALL QUESTIONS. Show clearly** all your calculations. Every value **must** be written with its correct Unit.
4. **WRITE YOUR ANSWER ON THIS QUESTION PAPER.**

NOTE: DO NOT OPEN THE QUESTION PAPER UNTIL INSTRUCTED TO DO SO.

☺ GOOD LUCK! ☺

Question Number	Q1 (a)	Q1 (bc)	Q2 (a)	Q2 (bc)	Q3 (ab)	Q4 (a)	Q4 (b)	Total
Marks								
CO	9	3	9	3	5	9	4	

BASIC FORMULA FOR TRANSISTOR

BJT

$$i_C = I_S e^{v_{BE}/V_T}\ ;\text{npn}$$

$$i_C = I_S e^{v_{EB}/V_T}\ ;\text{pnp}$$

$$i_C = \alpha i_E = \beta i_B$$

$$i_E = i_B + i_C$$

$$\alpha = \frac{\beta}{\beta + 1}$$

;Small signal

$$\beta = g_m r_\pi$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

$$V_T = 26\,\text{mV}$$

MOSFET

;N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n[v_{GS} - V_{TN}]^2$$

$$K_n = \frac{k_n'}{2} \cdot \frac{W}{L}$$

;P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p[v_{SG} + V_{TP}]^2$$

$$K_p = \frac{k_p'}{2} \cdot \frac{W}{L}$$

;Small signal

$$g_m = 2\sqrt{K_n I_{DQ}}\ ;\text{N-MOSFET}$$

$$g_m = 2\sqrt{K_p I_{DQ}}\ ;\text{P-MOSFET}$$

$$r_o \cong \frac{1}{\lambda I_{DQ}}$$

Quadratic formula :

$$Ax^2 + Bx + C = 0 \quad \rightarrow \quad x = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$

This is extra page for answers. Please indicate question number clearly.

QUESTION 1 [30 marks]

The circuit in **Figure 1** has a pair of **NPN** transistors as input devices and three **PNP** transistors connected as an active load. The differential amplifier circuit is biased with a constant current source $\boldsymbol{I_Q = 0.24\ mA}$ that has output resistance $\boldsymbol{R_{OCS} = 50\ M\Omega}$.
The transistor parameters are: $\boldsymbol{\beta = 200}$, $\boldsymbol{V_{A1} = V_{A2} = 100\ V}$, $\boldsymbol{V_{A3} = V_{A4} = 60\ V}$, and $\boldsymbol{V_{A5}} = \infty$.

(a) The DC currents in the differential amplifier are **balanced**, that is $\boldsymbol{I_1 = I_2 = I_3 = I_4}$. **Show** that $I_O \cong \frac{I_Q}{\beta(1+\beta)}$ and **calculate** the value of $\boldsymbol{I_O}$. **[10 marks]**

(b) **Determine** $\boldsymbol{R_L}$ such that the differential-mode voltage gain ($\boldsymbol{A_d}$) of the differential amplifier with active load in the **Figure 1** is reduced to **80%** of its **open-circuit differential-mode voltage gain value**. **[15 marks]**

(c) **Design** a better active load circuit that can replace the active load in the **Figure 1**. **Discuss** why your design is better than the circuit in **Figure 1**. **[5 marks]**

Answers for Question 1

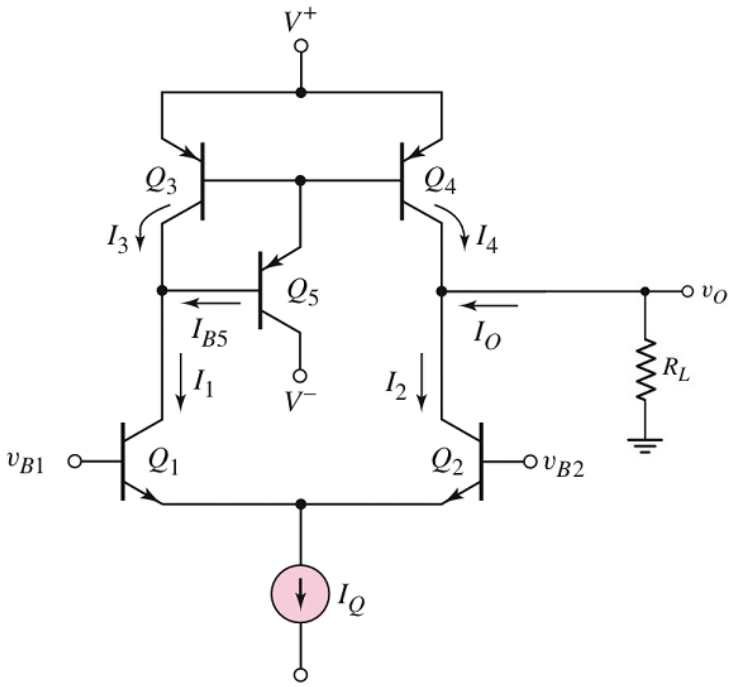

Figure 1

Answers for Question 1 (Continued)

QUESTION 2 [30 marks]

Figure 2 shows a **MOSFET** differential amplifier circuit with active load biased with constant current source I_Q. It is given that $V^+ = 5$ V, $V^- = -5$ V, and $I_Q = 0.3$ mA.

The **N-MOSFET** parameters are: $V_{TN} = 0.8$ V, $k'_n = 200\ \mu A/V^2$ and $\lambda_n = 0.01\ V^{-1}$, while the **P-MOSFET** parameters are: $V_{TP} = -0.7$ V, $k'_p = 80\ \mu A/V^2$ and $\lambda_p = 0.015\ V^{-1}$.

(a) **State** the function of each transistor M_1 to M_6 in the **Figure 2**. **[6 marks]**

(b) **Calculate** the voltages V_{GS1}, V_{SG5} and V_{D1}. **[12 marks]**

(c) **Calculate** the differential gain (A_d) of the circuit if given: $(W/L)_{1\text{-}2} = 10$, $(W/L)_{3\text{-}6} = 30$. **[12 marks]**

Answers for Question 2

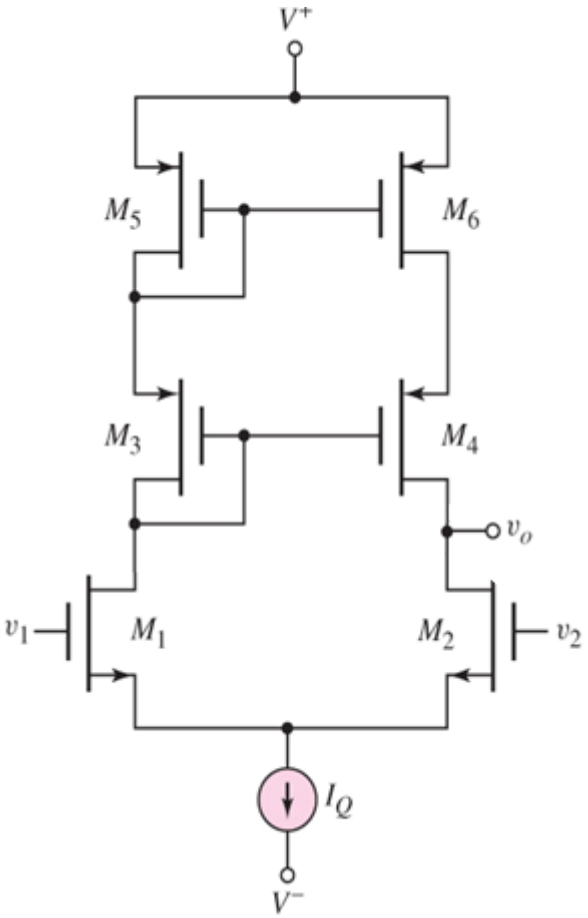

Figure 2

Answers for Question 2 (Continued)

QUESTION 3 [20 marks]

Consider a **multistage amplifier** shown in **Figure 3**. Study the **Figure 3** carefully. The output stage in the circuit is a **Darlington pair** emitter-follower configuration.

Assume β **= 120** for all **NPN** transistors and β **= 90** for all **PNP** transistors. Let V_{A7} **= 60 V for** Q_7**,** V_{A11} **= 120 V for** Q_{11}, and $V_A = \infty$ for all other transistors. Values for resistors are $R_2 = R_3 = 0.2$ **kΩ** and $R_4 = 5$ **kΩ.**

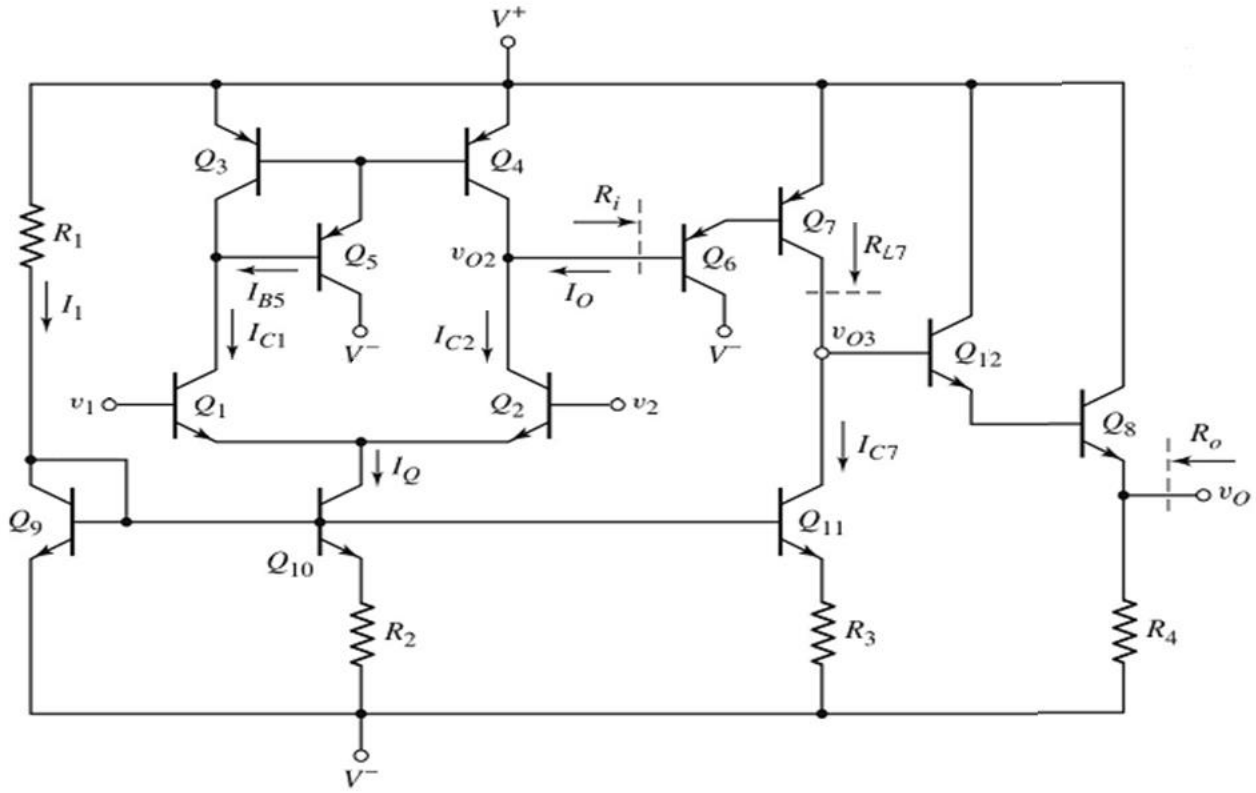

Figure 3

Given that $I_{C7} = I_{C11} = I_Q$ **= 0.3 mA** and I_{C8} **= 1.2 mA**:

(a) **Determine** the effective resistance connected between collector of Q_7 and signal ground **(**i.e. determine R_{L7} shown in the **Figure 3)**. **[13 marks]**

(b) **Determine** output resistance (R_o) of the output stage. **[7 marks]**

Answers for Question 3

Answers for Question 3

QUESTION 4 [20 marks]

(a) **Sketch** the **Class-B** output stage circuit employing **NPN** and **PNP** BJTs of Q_n and Q_p. **Explain** the operation of the **Class-B** circuit. **[5 marks]**

(b) A **Class-A** output stage with BJTs is shown in **Figure 4**. It is given that $V^+ = 5$ V, $V^- = -5$ V, and $R_L = 100\ \Omega$. Assume all the transistors are matched with $I_S = 9\text{x}10^{-15}$ A, $V_{CE}(\text{sat}) = 0.3$ V, and $V_A = \infty$. Neglect the base currents.

(i) **Calculate** the maximum possible output voltage range of the circuit. **[2 marks]**

(ii) **Determine** the **minimum** required biasing current I_Q for Class A operation. **[3 marks]**

(iii) The output voltage range is now limited to $-4\text{V} \le v_O \le +4\text{V}$. **Calculate** the required range of the input voltage v_I. **[10 marks]**

Answers for Question 4

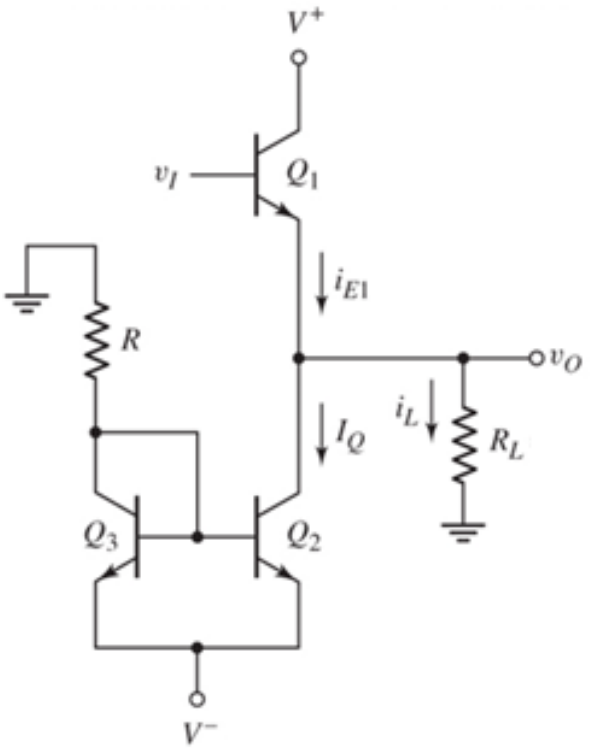

Figure 4

Answers for Question 4 (Continued)

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