The National Energy University

COLLEGE OF ENGINEERING
PUTRAJAYA CAMPUS
FINAL EXAMINATION

SEMESTER 3   2018 / 2019

PROGRAMME	: **Bachelor of Electrical & Electronics Engineering (Honours)** **Bachelor of Electrical Power Engineering (Honours)**
SUBJECT CODE	: **EEEB273**
SUBJECT	: **ELECTRONIC ANALYSIS AND DESIGN II**
DATE	: **April/May 2019**
DURATION	: **3 hours**

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **FIVE** (5) questions in **EIGHT** (8) pages.
2. Answer **ALL** questions.
3. Write **all** answers in the answer booklet provided. **Use pen** to write your answer.
4. Write answer to different question on **a new page**.

THIS QUESTION PAPER CONSISTS OF EIGHT* (8) *PRINTED PAGES INCLUDING THIS COVER PAGE.

<u>Question 1 [20 marks]</u>

(a) **Figure 1** shows a two-transistor **MOSFET** current mirror. The transistor parameters are assumed to be $\boldsymbol{V_{TP} = -0.4}$ **V**, $\boldsymbol{k'_p = 60}$ **μA/V²**, and $\boldsymbol{\lambda = 0}$. The transistor width-to-length ratios are $\boldsymbol{(W/L)_1 = 25}$, $\boldsymbol{(W/L)_2 = 15}$, and $\boldsymbol{(W/L)_3 = 5}$.

Calculate $\boldsymbol{I_O}$, $\boldsymbol{I_{REF}}$, $\boldsymbol{V_{SG1}}$, and $\boldsymbol{V_{SG3}}$. **[10 marks]**

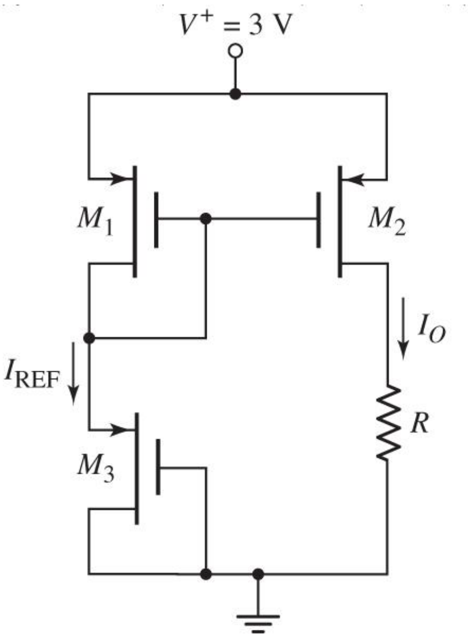


Figure 1

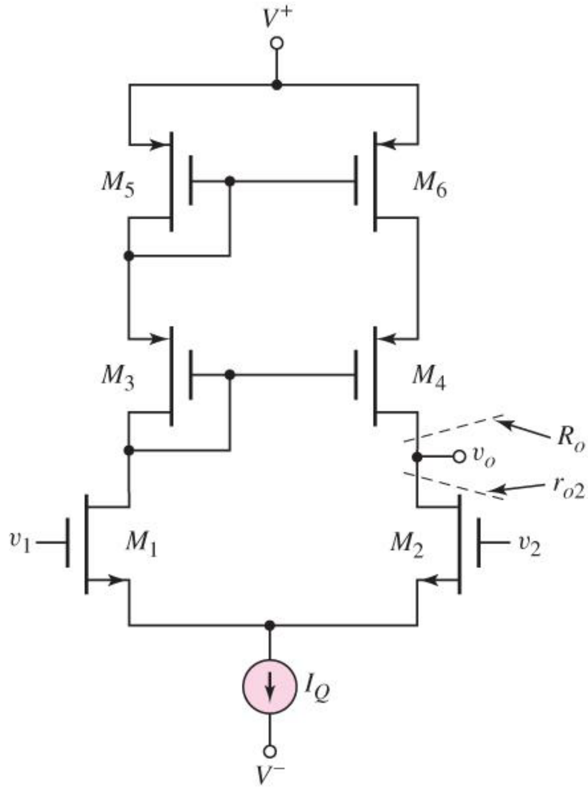


Figure 2

(b) **Figure 2** shows a **MOSFET diff-amp with a Cascode active load**. Assume that **NMOS** devices are available with the following parameters: $\boldsymbol{V_{TN} = 0.5}$ **V**, $\boldsymbol{k'_n = 80}$ **μA/V²**, $\boldsymbol{\lambda_n = 0.02}$ **V⁻¹**, and $\boldsymbol{(W/L)_1 = (W/L)_2 = 10}$. Assume that **PMOS** devices are available with the following parameters: $\boldsymbol{V_{TP} = -1.0}$ **V**, $\boldsymbol{k'_p = 40}$ **μA/V²**, $\boldsymbol{\lambda_p = 0.02}$ **V⁻¹**, and $\boldsymbol{(W/L)_p = 20}$. The circuit parameters are $\boldsymbol{V^+ = 5}$ **V** and $\boldsymbol{V^- = -5}$ **V**. The bias current is $\boldsymbol{I_Q = 0.2}$ **mA**.

(i) **Determine** the output resistance, $\boldsymbol{R_O}$, of the **Cascode** active load. **[6 marks]**

(ii) **Find** the differential-mode voltage gain, $\boldsymbol{A_d}$. **[4 marks]**

Question 2 [20 marks]

(a) **Design** a three-transistor BJT current source using **PNP** transistors so that **its output current** (I_O) is **0.8 mA**. All transistors are matched. The transistor parameters are β **= 50,** V_{EB}**(on) = 0.6 V**, and $V_A = \infty$. The circuit parameters are V^+ **= 7.5 V** and V^- **= -7.5 V**. **Draw** the circuit diagram of your design. **Show clearly all calculations and values in the circuit diagram** as marks are given according to this. **[10 marks]**

(b) A **basic differential pair** is shown in **Figure 3**. It is given that V^+ **= 15 V**, V^- **= -15 V**, resistor R_C **= 5 kΩ**, I_Q **= 2 mA**, and transistor parameters are β **= 100**, voltages V_A **= 100 V**, V_{BE}**(on) = 0.7 V**, and V_{CE}**(sat) = 0.3 V**.

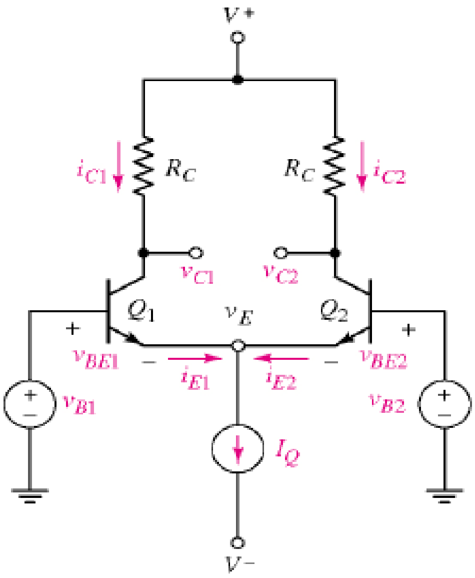


Figure 3

$$A_{cm} = \frac{-g_m R_C}{1+\frac{2(1+\beta)R_o}{r_\pi + R_B}} \quad (2.1)$$

(i) **Calculate** the **one-sided** small-signal differential voltage gain (A_d) of the differential amplifier. **[2 marks]**

(ii) The constant current source of **Figure 3** that is providing the current I_Q is implemented using the **basic two transistor current source**. **Find** the value of A_{cm}, the **common-mode voltage gain** of the differential-amplifier, using **Equation (2.1)** given above near **the Figure 3**. Assume R_B **= 0**. **[2 marks]**

(iii) The differential amplifier shown in **Figure 3** has a **PNP three-transistor current mirror** connected as an **active load**. **Redraw Figure 3** with the new active load. Assume same values of β and V_A for **PNP**. **Determine** the differential mode gain **(**A_d**)** and how much the A_d had changed using the new active load. **[6 marks]**

Question 3 [20 marks]

(a) A simple bipolar op-amp is shown in **Figure 4**. Study the **Figure 4** carefully.

Neglect base currents. Assume parameters for all transistors are V_{BE}**(on) = 0.7 V**, β **= 200,** and $V_A = \infty$. **Bias current** for the differential amplifier can be calculated to be I_Q **= 1.2 mA.** With small-signal analysis, values of gain A_{d1} for the differential amplifier, $r_{\pi 3}$, and gain A_{v2} for the gain stage can be found using the following **Equations (3.1) to (3.3)**.

$$A_{d1} = \frac{V_{o2}}{v_d} = \frac{g_{m2}}{2}(R_C||R_{i2}) \qquad \textbf{(3.1)}$$

$$r_{\pi 3} \cong \beta r_{\pi 4} \qquad \textbf{(3.2)}$$

$$A_{v2} \cong \frac{I_{R4}}{2V_T}(R_5) \qquad \textbf{(3.3)}$$

Calculate the **total overall small-signal voltage gain (**A_d**)** for the bipolar op-amp.

[10 marks]

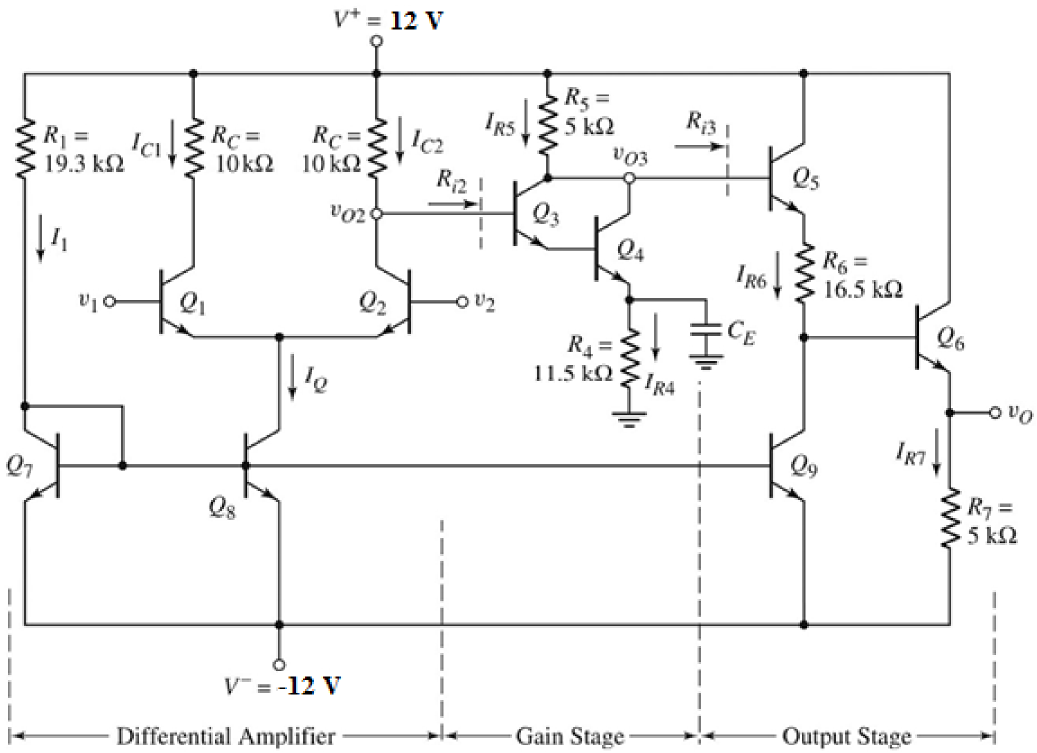


Figure 4

(b) An **idealized Class-B output stage** is to deliver **10 Watts of average power** to a load for a symmetrical input sine wave. The maximum output voltage **(**V_p**)** required should be **80%** of the power supply voltage V_{CC}. Given that the power supply voltage V_{CC} is **24 V** and the average current in the circuit is $I(ave) = V_p / (\pi R_L)$, where R_L is the load. **Calculate** the value of the output stage's **power conversion efficiency (**η**)**. **[10 marks]**

Question 4 [20 marks]

(a) The **741 op-amp** is shown in **Figure 5.** Assume that $V_{BE}(\text{on}) = V_{EB}(\text{on}) = 0.7$ V, $\beta_n = 200$, $\beta_p = 60$, $V_{AN} = 200$ V, and $V_{AP} = 100$ V. The area of transistor Q_{13B} is **75%** of transistor Q_{12}. It is given that $I_{REF} = I_{C12} = 0.4$ mA. **Calculate** the **small signal input resistance** of the **Gain stage** (i.e. equivalent resistance looking into the base of Q_{16}). **[10 marks]**

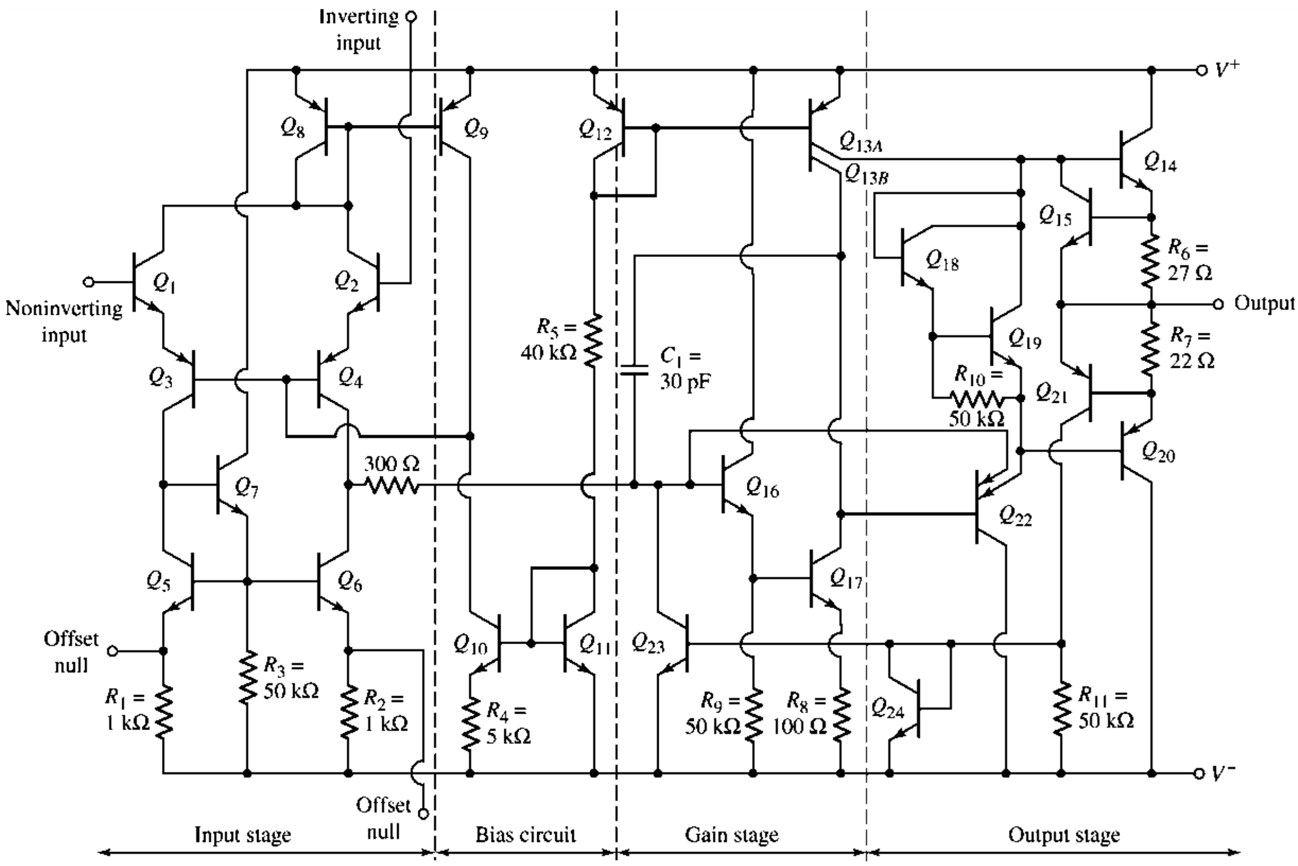


Figure 5

Question 4 (Continue)

(b) Consider the **MC14573** op-amp in **Figure 6.** Assume transistor parameters for **N-MOSFET** are V_{TN} **= 0.5 V**, K_n **= 100 μA/V²** and λ_n **= 0.01 V⁻¹**; and transistor parameters for **P-MOSFET** are V_{TP} **= -0.5 V**, K_p **= 125 μA/V²,** and λ_p **= 0.02 V⁻¹**.

Given that V_{SG5} **= 1.5 V:**

(i) **Find** the **quiescent bias currents** for all transistors in the **Figure 6**. **[4 marks]**

(ii) **Determine** the **overall small signal differential-mode voltage gain** for the **MC14573** op-amp in the **Figure 6**. Gain for the output stage consists of transistor M_7 and M_8 is given by equation $A_{v2} = -g_{m7}(r_{o7}||r_{o8})$. **[6 marks]**

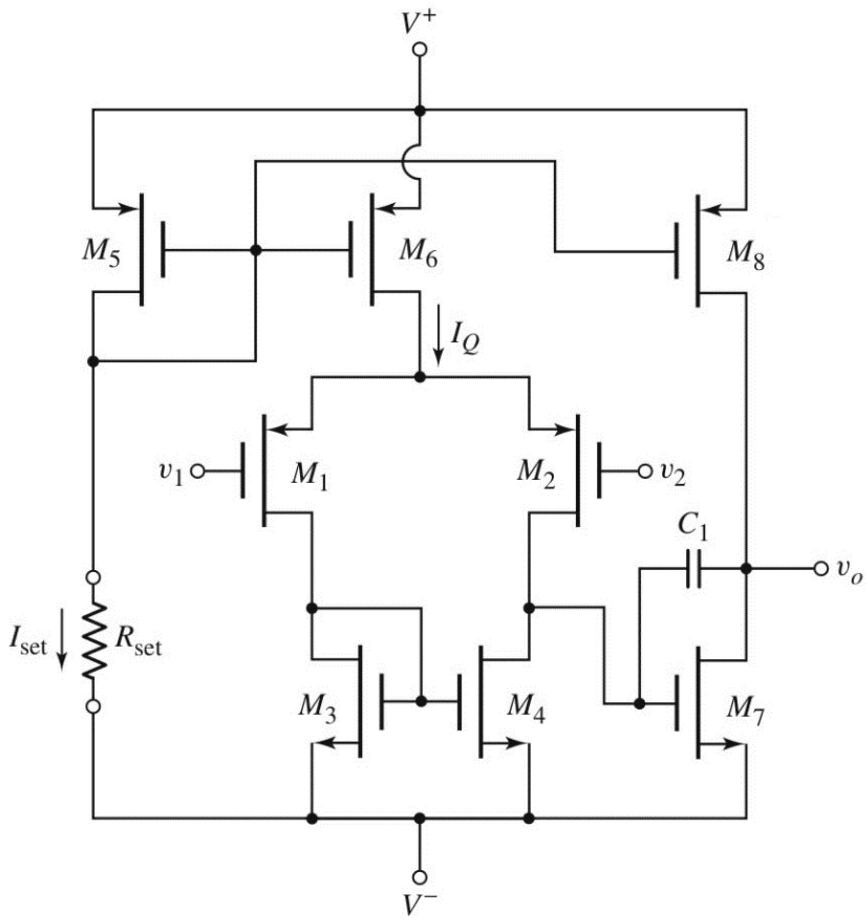


Figure 6

Question 5 [20 marks]

(a) **List two** (2) ideal op-amp characteristics. **[2 marks]**

(b) **Figure 7** shows a **difference amplifier** using ideal op-amps.

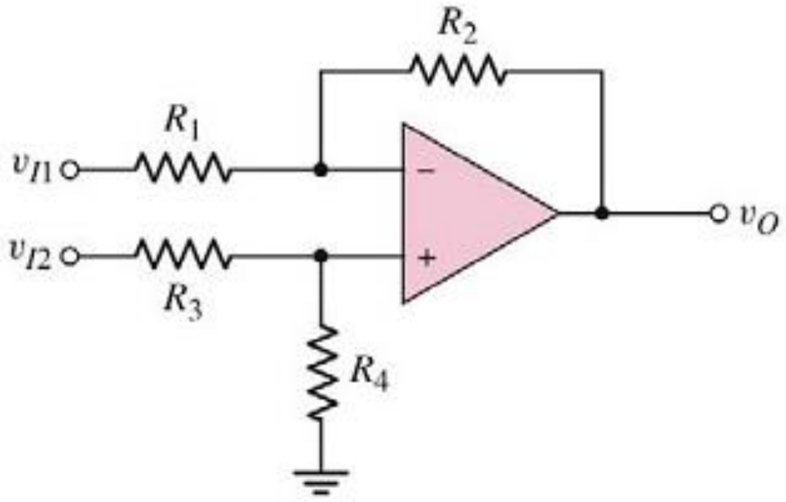


Figure 7

With proper analysis, **show** that **[10 marks]**

$$v_O = \left(1+\frac{R_2}{R_1}\right)\left(\frac{R_4/R_3}{1+R_4/R_3}\right)v_{I2} - \left(\frac{R_2}{R_1}\right)v_{I1}$$

(c) For the difference amplifier in the **Figure 7**, let $\boldsymbol{R_1}$ **= 12 kΩ**, $\boldsymbol{R_2}$ **= 120 kΩ**, $\boldsymbol{R_3}$ **= 40 kΩ**, and $\boldsymbol{R_4}$ **= 440 kΩ**. **Determine** ***CMRR*****(dB)**. **[8 marks]**

-END OF QUESTION PAPER-

APPENDIX:

A) BASIC FORMULA FOR TRANSISTOR

BJT

$$i_C = I_S e^{v_{BE}/V_T} \quad ;\text{NPN}$$

$$i_C = I_S e^{v_{EB}/V_T} \quad ;\text{PNP}$$

$$i_C = \beta i_B = \frac{\beta}{\beta+1} i_E$$

$$i_E = i_B + i_C$$

;Small signal

$$\beta = g_m r_\pi$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$r_o = \frac{V_A}{I_{CQ}}$$

$$V_T = 26\,\text{mV}$$

MOSFET

;N – MOSFET

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

$$i_D = K_n[v_{GS} - V_{TN}]^2$$

$$K_n = \frac{\mu_n C_{ox} W}{2L} = \frac{k_n'}{2} \cdot \frac{W}{L}$$

;P – MOSFET

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

$$i_D = K_p[v_{SG} + V_{TP}]^2$$

$$K_p = \frac{\mu_p C_{ox} W}{2L} = \frac{k_p'}{2} \cdot \frac{W}{L}$$

;Small signal

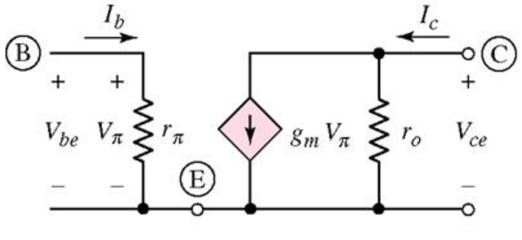
$$g_m = 2\sqrt{K_n I_{DQ}} \quad ;\text{N – MOSFET}$$

$$g_m = 2\sqrt{K_p I_{DQ}} \quad ;\text{P – MOSFET}$$

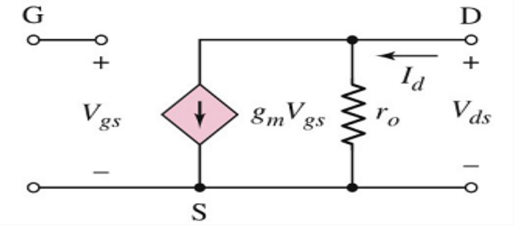
$$r_o \cong \frac{1}{\lambda I_{DQ}}$$

B) HYBRID-π EQUIVALENT CIRCUITS

BJT



MOSFET



C) QUADRATIC FORMULA

$$Ax^2 + Bx + C = 0 \quad \rightarrow \quad x = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$