UNIVERSITI TENAGA NASIONAL

CHAPTER 4
TOP LEVEL VIEW OF COMPUTER FUNCTION AND INTERCONNECTION

CGMB143 COMPUTER SYSTEM

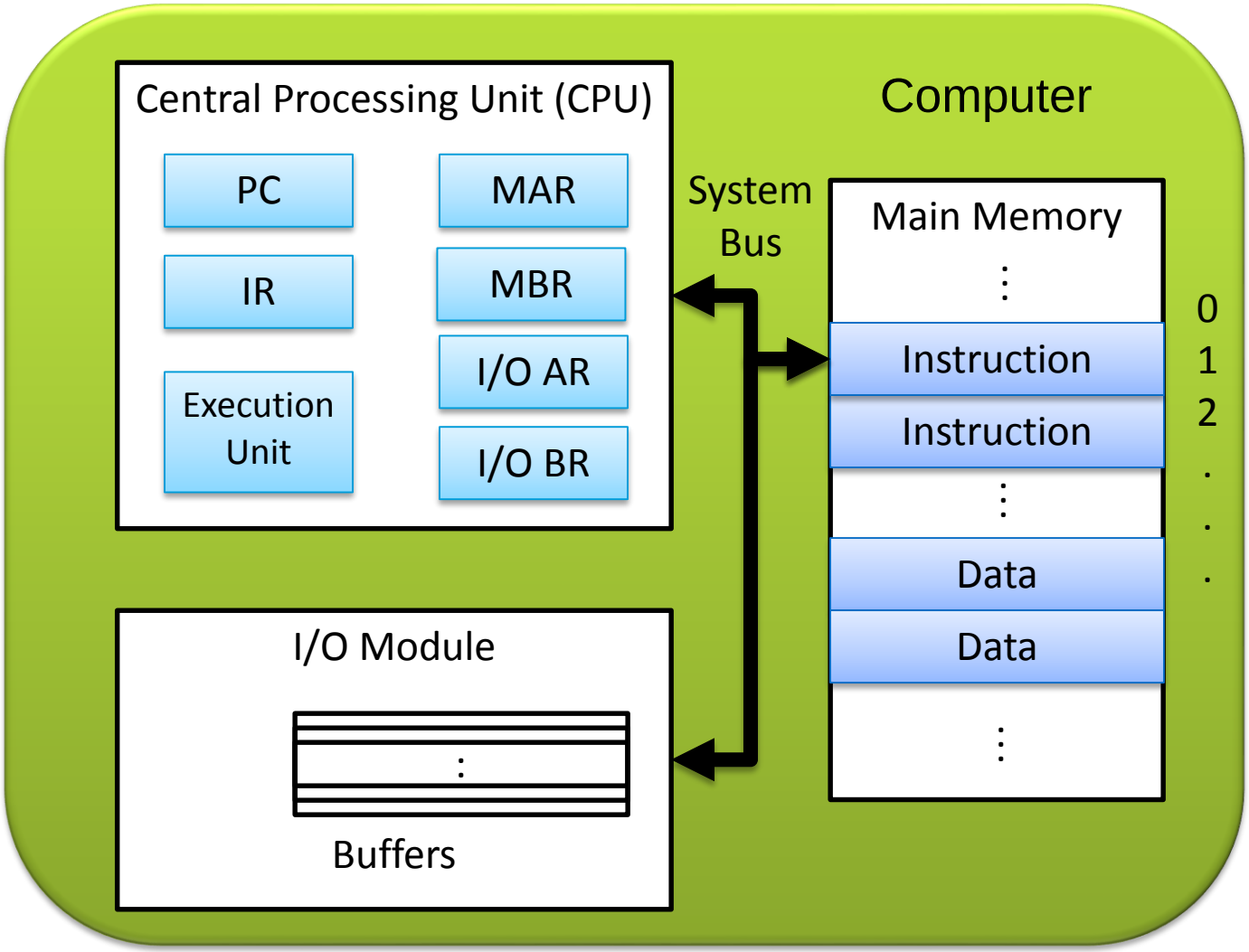
What is a program?

A sequence of steps

arithmetic or logical operation is done

a different set of control signals is needed

Computer Components



PC = Program Counter

IR = Instruction Register

MAR = Memory Address Register

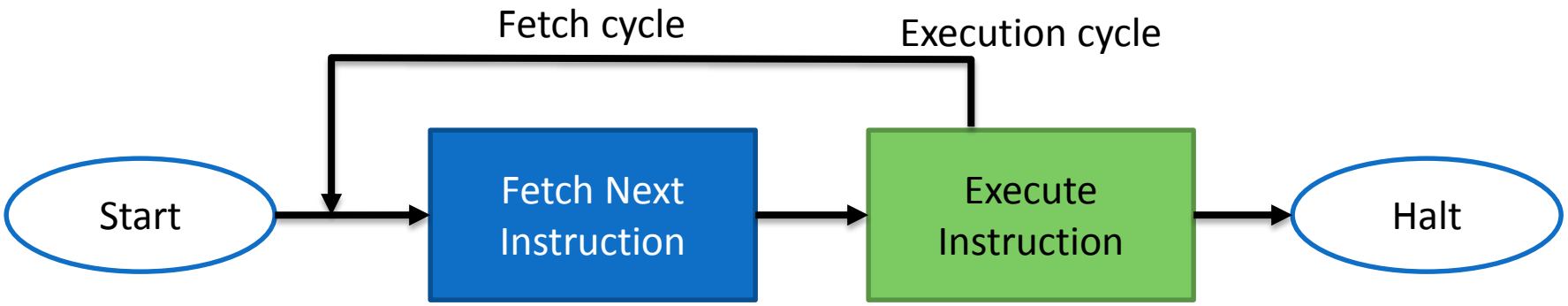
MBR = Memory Buffer Register

I/O AR = Input/Output Address Register

I/O BR = Input/Output Buffer Register

Instruction Cycle

- Two steps
  - Fetch cycle
  - Execute cycle



Fetch Cycle

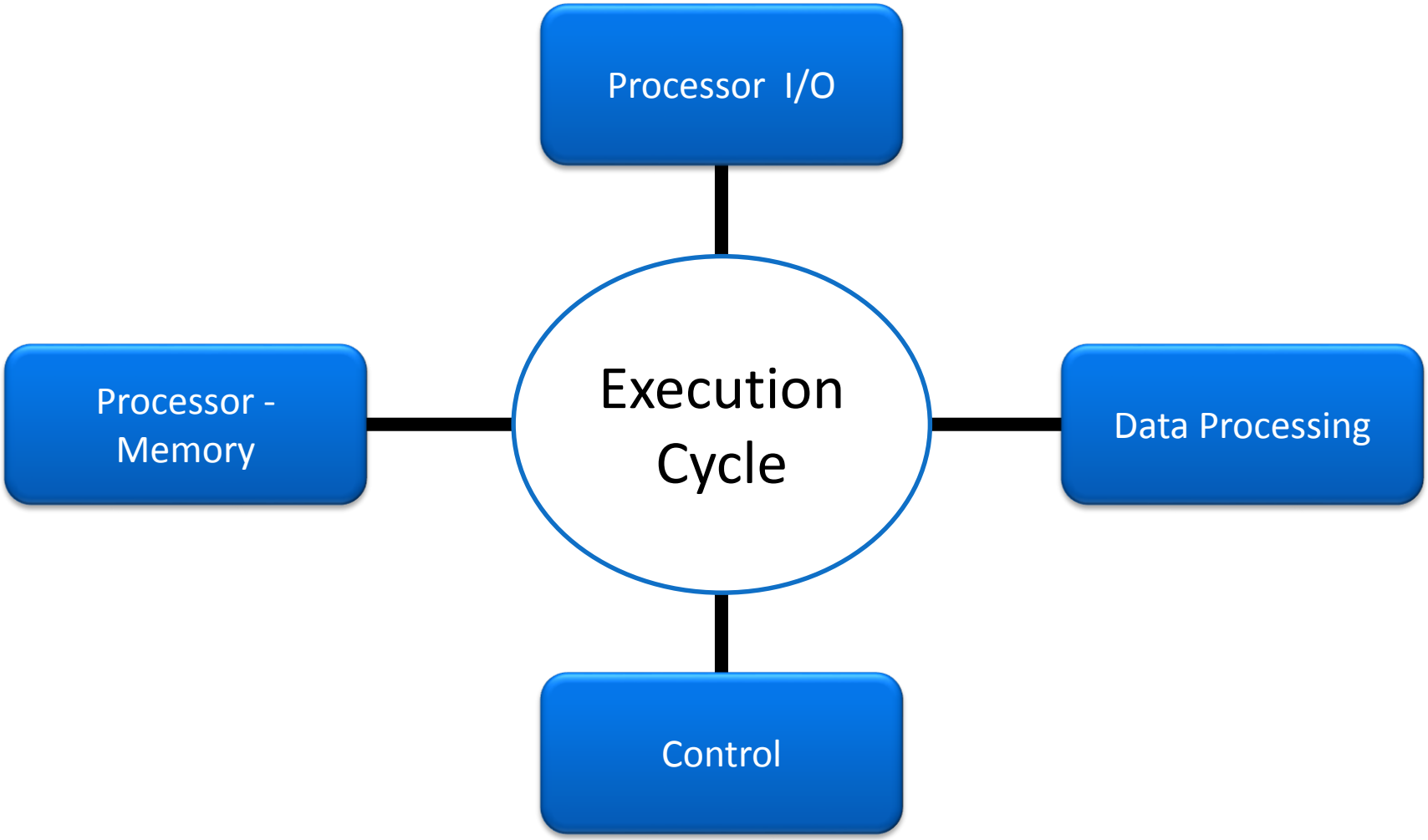
- Holds address of next instruction to fetch

- Fetch instruction from memory location pointed to by PC
- Increment PC

- Load the instruction

- Interprets instruction
- Perform required actions

Execute Cycle

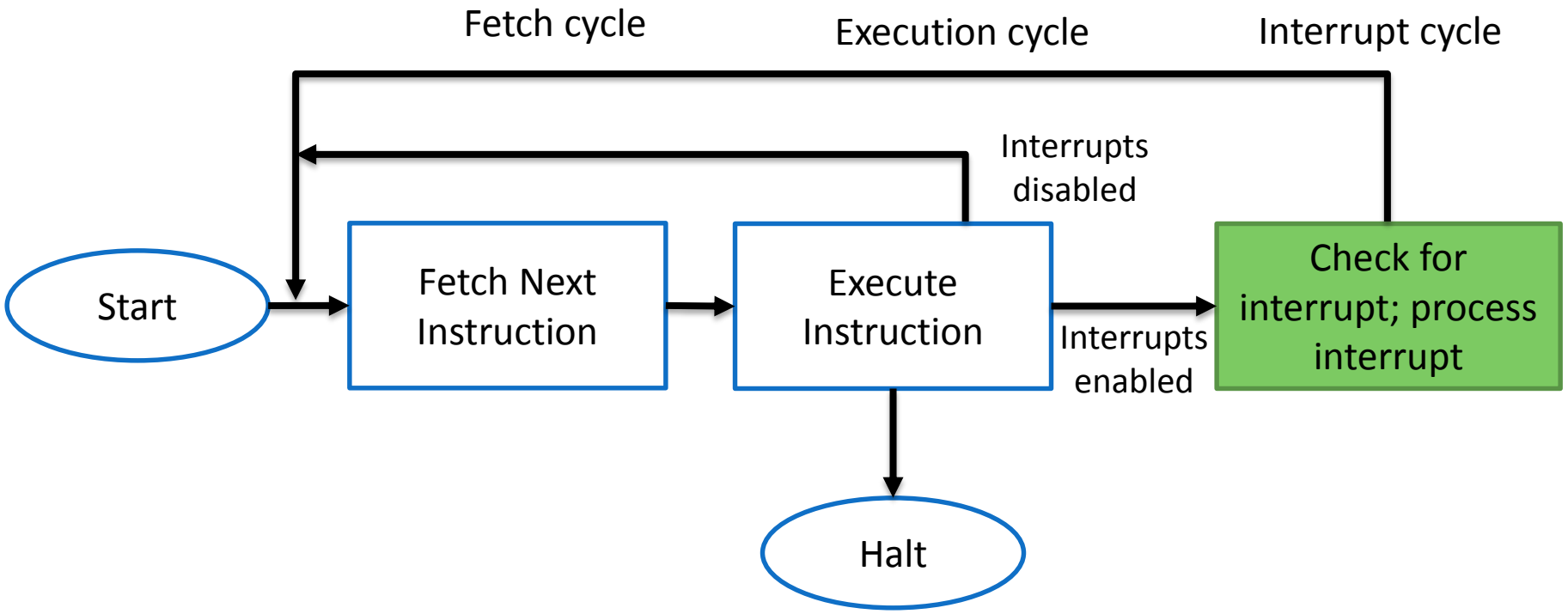


Interrupts

- Mechanism by which other modules (e.g. I/O) may interrupt normal sequence of processing

Interrupt Cycle

- Added to instruction cycle



Interrupt Cycle (Cont.)

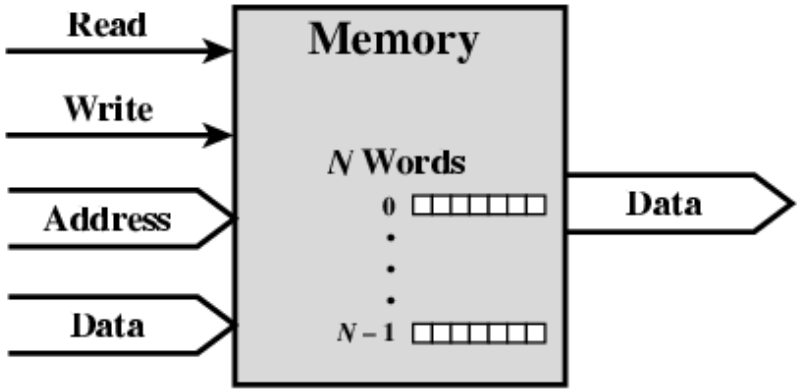
- Processor checks for interrupt
  - Indicated by an interrupt signal
- If no interrupt, fetch next instruction
- If interrupt pending:
  - Suspend execution of current program
  - Save context
  - Set PC to start address of interrupt handler routine
  - Process interrupt
  - Restore context and continue interrupted program

Interconnection Structures

- Collection of paths connecting the various modules
- Modules:
  - Memory
  - Processor
  - I/O module

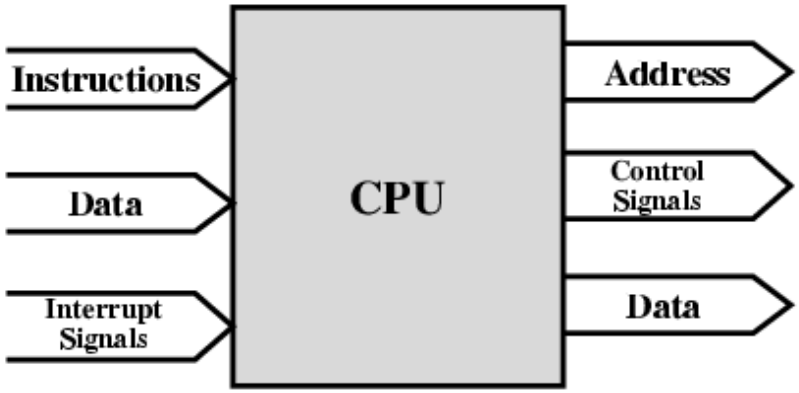
Modules: Major Form of Input and Output - Memory

- **Word** of data - Read from or written into the memory
  - Assigned a unique numerical address
- Nature of the operation – indicated by read and write control signals
- Address – specify the location for the operation



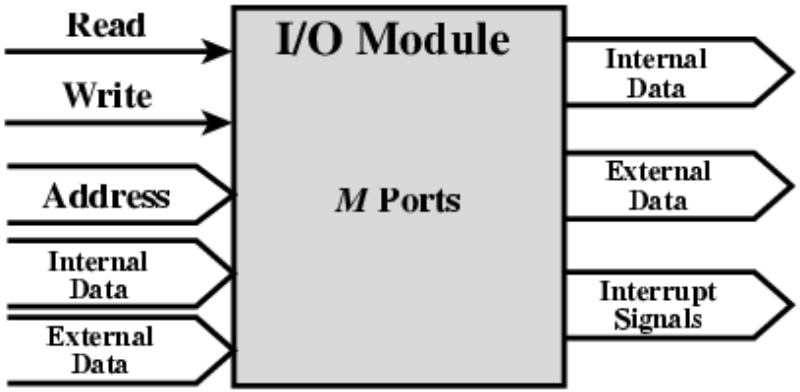
Modules: Major Form of Input and Output - Processor

- Reads instruction and data
- Writes out data (after processing)
- Sends control signals to other units
- Receives (& acts on) interrupts

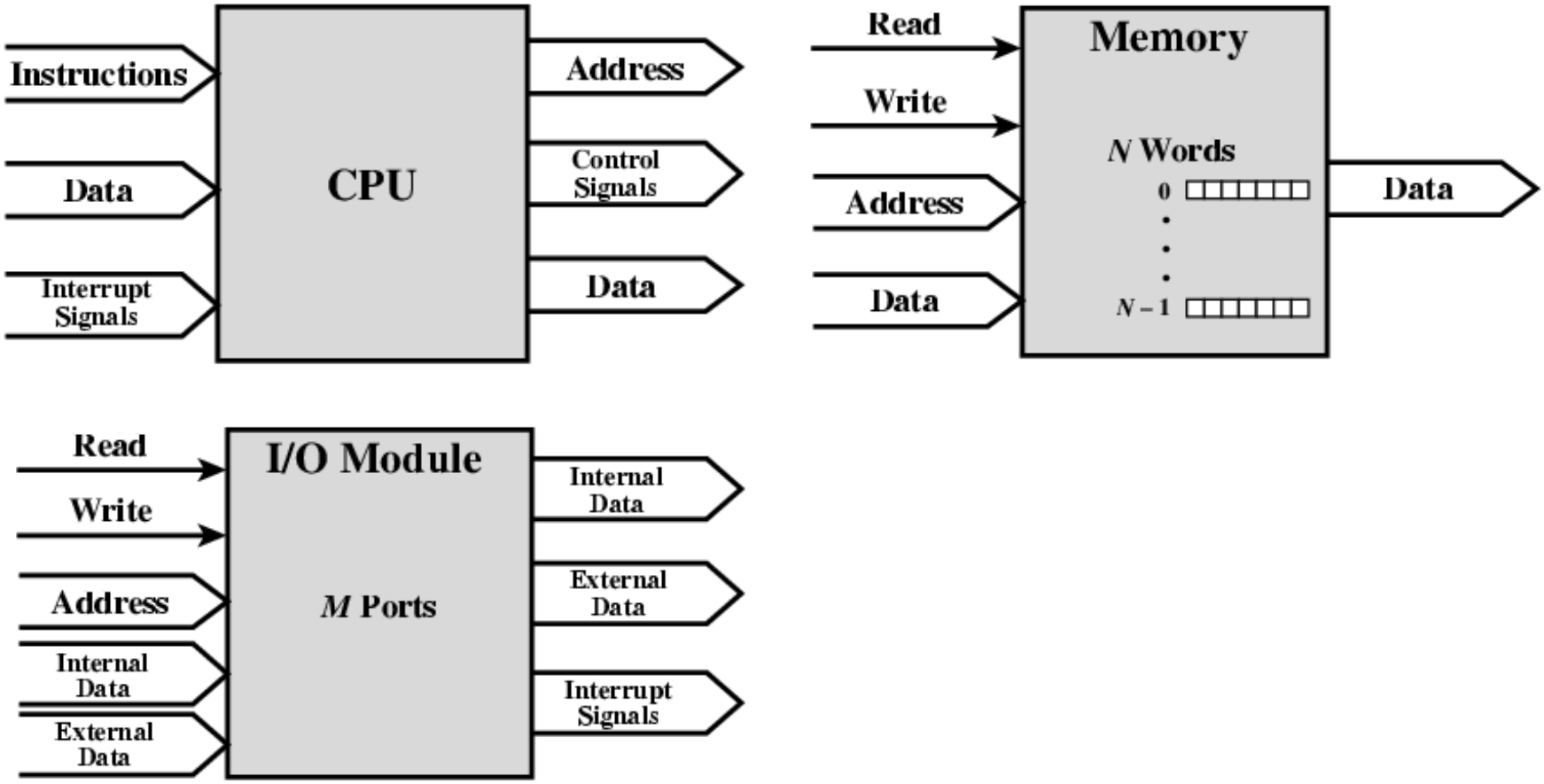


Modules: Major Form of Input and Output – I/O Module

- Operations;
  - Read
  - Write
- Control more than one external device
- External data path – input and output of data
- Send interrupt signals to CPU



Modules:
Major Form of Input and Output



Types of Transfers

- **Memory to processor**: Processor reads instruction/data from memory
- **Processor to memory**: Processor writes data to memory
- **I/O to processor**: Processor reads data from I/O device (via I/O module)
- **Processor to I/O**: Processor sends data to I/O device
- **I/O to/from memory**: allowed to exchange data using Direct Memory Access (DMA) – exclude processor

Bus Interconnection

- Communication pathway connecting two or more devices
- Key characteristic: shared transmission medium
- Consists of multiple communication pathways/lines
  - Lines – transmit signals representing binary 1 and 0 – one data at a time

System Bus

- A bus that connects major computer components (CPU, memory, I/O)
- Computer interconnection structures – use one or more system buses
- Consists of 50 to hundreds of separate lines
  - Each line – function. E.g: power

Data Line

- Provide a path for moving data among system modules
- Collective – data bus

Data Bus

- Collective of data lines
- **Width** of the data bus - Number of lines;
  - 32, 64, 128 …
  - Key factor in determining overall system performance
- Number of data lines – represents number of data can be transferred at a time

Address Lines

- Designate the source or destination of the data on data bus

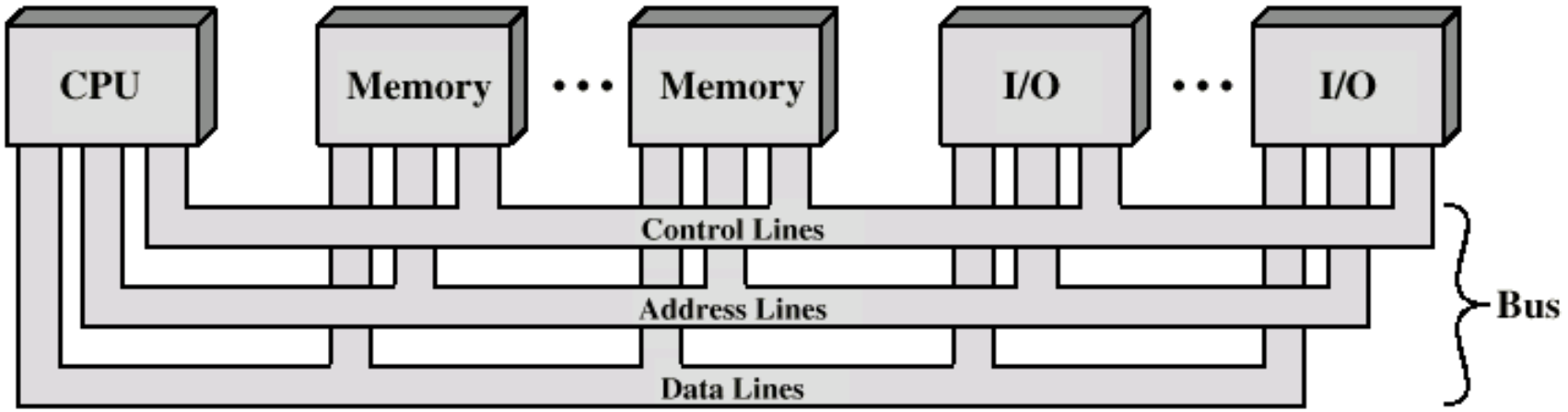
Address Bus

- Collective of address lines
- Width of the address bus determines the maximum possible memory capacity of the system

Control Lines

- Used to control the access to and the use of the **data** and **address lines**
- Control signals transmit both command and timing information among system modules
  - Command signals – specify operations to be performed
  - Timing signals – validity of data and address information

Bus Interconnection Scheme

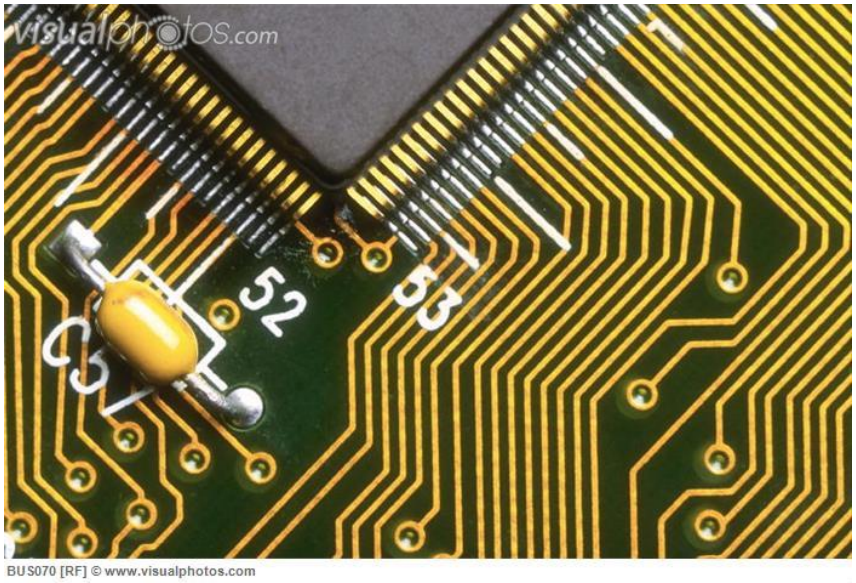


Operation of the Bus

- Send data
  - Obtain the use of the bus
  - Transfer data via the bus
- Request data
  - Obtain the use of the bus
  - Transfer a request to the other module over appropriate control and address lines

System Bus - Physical

- Number of parallel electrical conductors – metal lines on the circuit board



Single Bus - Problem

- Many of devices on one bus leads to:
  - Propagation delays
    - Long data paths mean that co-ordination of bus use can adversely affect performance
    - If aggregate data transfer approaches bus capacity
- Most systems use multiple buses to overcome these problems

Types of Bus

- Dedicated
  - Separate data & address lines
- Multiplexed
  - Shared lines
  - Address valid or data valid control line
  - Advantage
    - Fewer lines
  - Disadvantages
    - More complex control
    - Reduction in performance

Bus Arbitration

- Process of insuring only 1 devices places information onto the bus at a time

Bus Timing

- Synchronous
  - Occurrence of events on the bus is determined by the clock
  - All events start at the beginning of a clock cycle
  - Example: PCI bus (Peripheral Component Interface bus
- Asynchronous
  - The occurrence of one event follows and depends on the occurrence of a previous event
  - More flexible than synchronous bus but more complicated as well
  - Accommodates wider range of device speeds
  - Example: Futurebus+

END