DiLo Excercises on Module 5

Exercise 1

a	*b*	*Y*
0	0	1
0	1	1
1	0	0
1	1	1

Table 1

Assuming that Table 1 is the truth diagram for a circuit whereby *a* and *b* are the input variables and *Y* is the output variable:

1. Derive the Sum of Minterms Boolean expression for *Y*.
2. Draw the circuit diagram for Sum of Minterms *Y* using Cedar Simulator. Name the Sum of Minterms output as *Y1*.
3. Derive the Product of Maxterms Boolean expression for *Y*.
4. Extend the input of the circuit diagram drawn in (2) to include the circuit diagram for Product of Maxterms Y. Name the Product of Maxterms output as *Y2*.
5. Ensure that the variable-rate square wave clock of the input variable drawn in (4) contains all possible input combinations highlighted in Table 1. Run the simulation and produce the timing diagram for all the inputs and outputs.
6. What can you conclude about output signal *Y1* and *Y2*?

Exercise 2

a	*b*	*c*	*Y*
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Table 2

Assuming that Table 2 is the truth diagram for a circuit whereby *a, b, c* are the input variables and *Y* is the output variable. Repeat question 1 until 6 for data in Table 2.

Exercise 3

$$Y\ (a, b, c) = ab + a'c + bc' \text{.....(Equation 1)}$$

Assuming that Equation 1 describes the relationship of a input variables *a, b, c* with the output *Y* in a digital logic circuit design.

1. Derive the Sum of Minterms Boolean expression for *Y*.
2. Draw the circuit diagram for Sum of Minterms *Y* using Cedar Simulator. Name the Sum of Minterms output as *Y1*.
3. Derive the Product of Maxterms Boolean expression for *Y*.
4. Extend the input of the circuit diagram drawn in (2) to include the circuit diagram for Product of Maxterms Y. Name the Product of Maxterms output as *Y2*.
5. By using Equation 1, derive the complete truth table for all possible combination of input. Name the truth table as Table 3. Show your working.
6. Ensure that the variable-rate square wave clock of the input variable drawn in (4) contains all possible input combinations highlighted in Table 4. Run the simulation and produce the timing diagram for all the inputs and outputs.
7. What can you conclude about your timing diagram and the Table 4?