NAND and NOR

Perform the following implementation in a multi layer digital logic design (i.e. without opening up the brackets}. Use CEDAR simulation to demonstrate that both designs are equivalent.

NAND implementation (F1-NAND)

F1 = (BD + B'C)A + B'C'

NOR Implementation (F2-NOR)

F2= {[(A+B)(A'+C)]+D}(B'+C')