Digital Logic Design (CSNB163)

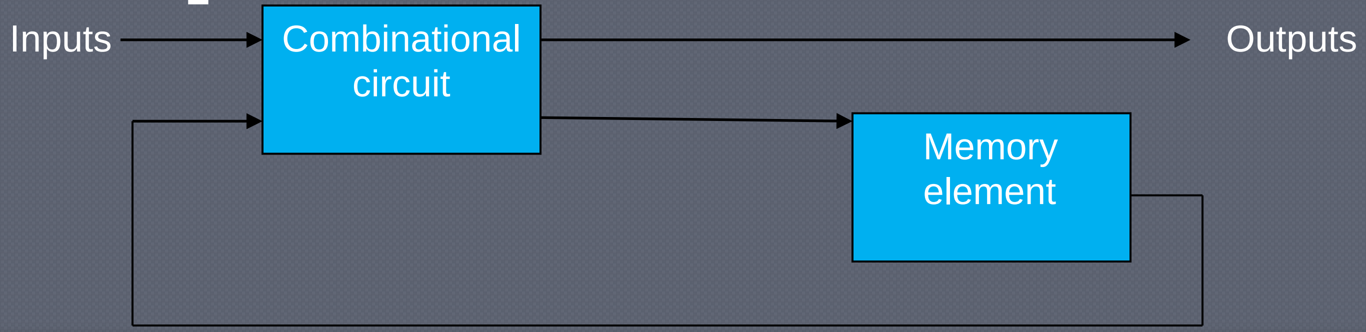
Module 12

Combinational Vs. Sequential Logic Circuit

- In Module 9, 10, 11, you have been introduced to examples of combinational logic circuits whereby the outputs are entirely dependent on the **current inputs**.
- The following topics will be on sequential logic circuits, whereby in addition to the external inputs, the circuits also receives data from the the **present state of the storage elements**.

Sequential Logic Circuit

- A sequential circuit consists of a combinational circuit with a **storage elements** connected to form a **feedback path**.
- The storage elements are devices capable of **storing binary information**.
- The binary information that stored in these elements **at any given time** defines the state of the sequential circuit at that time.

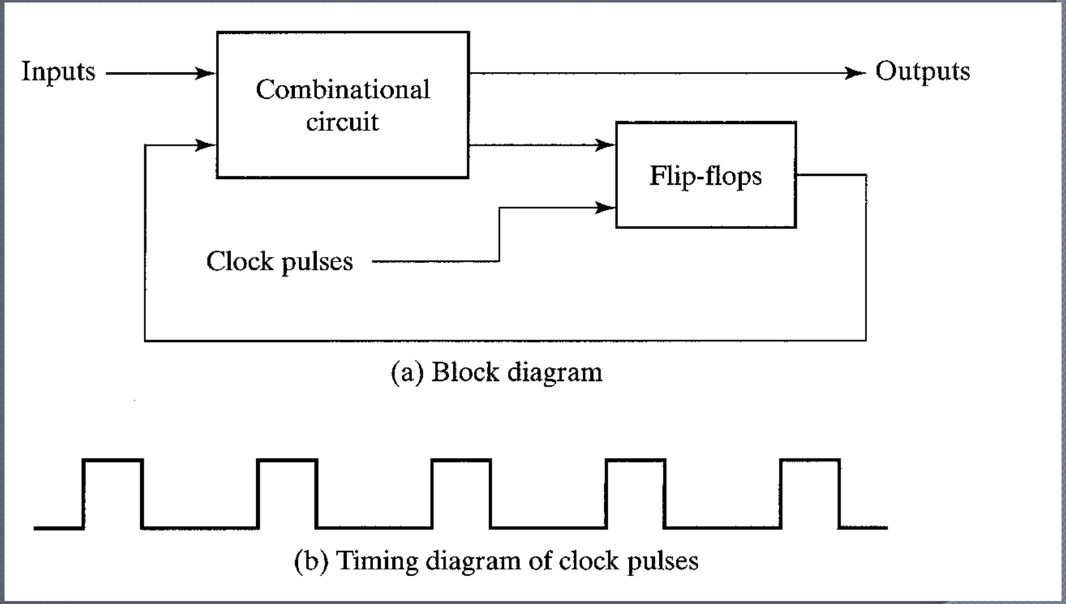


Sequential Logic Circuit (cont.)

- Two main types of sequential circuit (where classification depends on the timing of signals):
  - A **synchronous** sequential circuit - a system whose behavior can be defined from the knowledge of its signals at **discrete instants of time**. Synchronization is achieved by a timing device called a **clock generator** which provide a clock signal having the from of a periodic train of clock pulses.
  - An **asynchronous** sequential circuit - a system whose behavior depends upon the input signals at **any instant of time** and the order in which the inputs change. There is **no clock** in this circuit and thus, the signal changes are run freely and depend on signal order in the circuit.

Flip-Flops

- The storage element in synchronous sequential circuit is called **flip-flop** :- a binary **storage device** capable of storing **one bit binary data**.
- A flip-flop receives inputs from the **combinational circuit** and from a **clock**.
- Flip-flops are constructed by **latches**.
- Flip-flop **remains its state** as long as it is **powered**.



(a) Block diagram

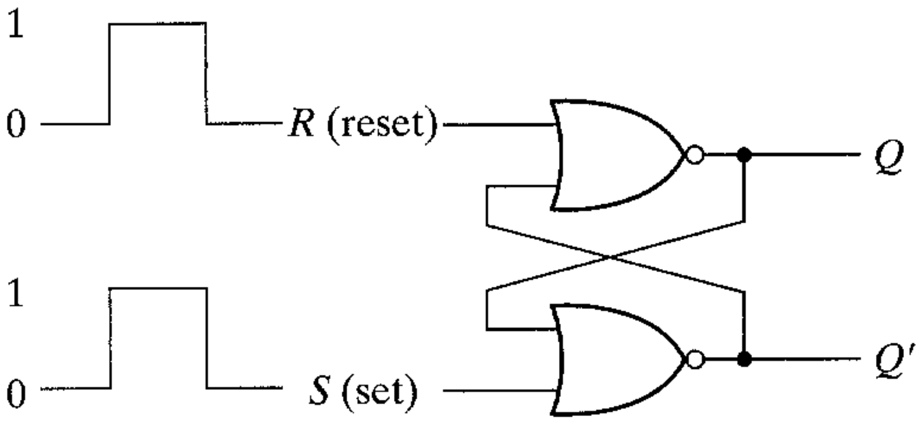
(b) Timing diagram of clock pulses

Latches

- Latches are device that constructed by basic **logic gates** to store **a single bit** of binary data.
- **Flip-flops** are constructed by **latches**.
- **Function table** (or **characteristics table**) describes the properties or characteristics of latches / flip flops.
- There are various kind of latches, we shall cover:
  - **SR latch**
  - **$\overline{S}\overline{R}$ latch**
  - **SR latch with control input**
  - **D latch**

SR Latch

- The SR latch is a circuit with 2 cross-coupled NOR gates. It has 2 inputs labeled S (Set) and R (Reset).



(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1$, $R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0$, $R = 1$)
1	1	0	0	

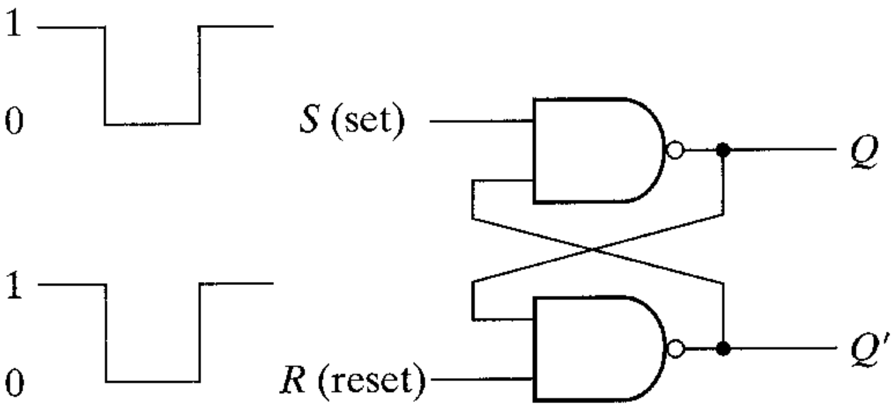
(b) Function table

SR Latch (cont.)

- Characteristics:
  - **Set State: when output Q = 1 and Q' = 0 (S=1, R=0)**
  - **Reset State: when output Q = 0, Q' = 1 (S=0, R=1)**
  - Output Q and Q' is **complement** to each other.
  - Under normal condition, both inputs of SR latch remain at **0** (S = 0 & R = 0), unless the state has to be change.
  - If both inputs are **1** (S = 1 & R = 1), the output is Q = 0, Q' = 0 which regards as an **undefined state**.
  - Before any **state change**, the both SR latch inputs **must be set to 0** (to avoid the occurrence of undefined state).
  - After set or reset state, the output will **remain unchanged** even though the input is removed (return to 0).

$\overline{S}\overline{R}$ Latch

- The characteristics of $\overline{S}\overline{R}$ latch are the **opposite** to SR latch (some references may refer them with the same name, does not matter…)
- It is a circuit with 2 cross-coupled NAND gates instead of 2 NOR gates.



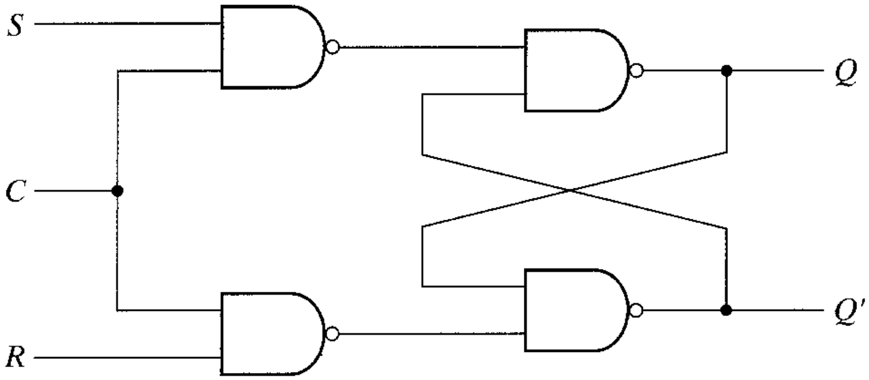
(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1$, $R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0$, $R = 1$)
0	0	1	1	

(b) Function table

SR Latch with Control Input

- The operation of basic SR latch can be modified to determine when the state of the latch can be changed by adding a control input.



(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

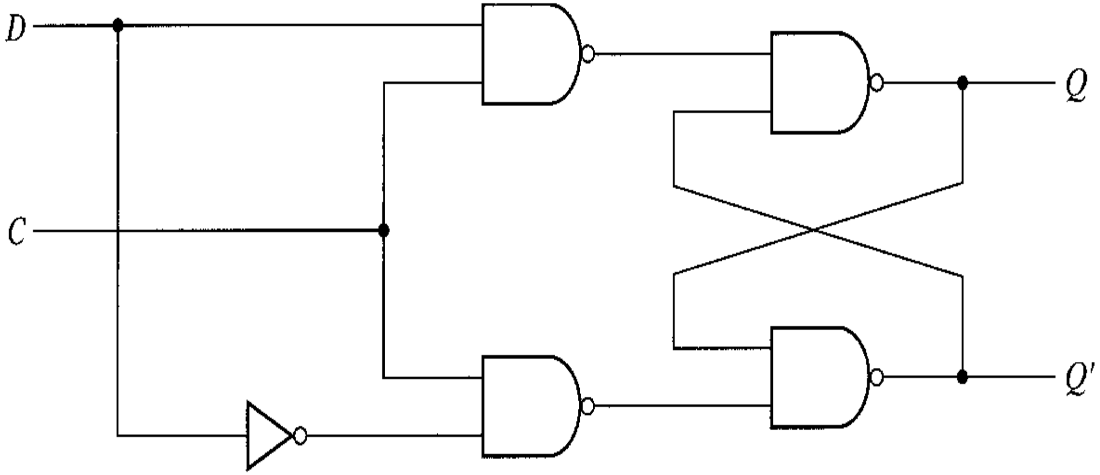
(b) Function table

SR Latch with Control Input (cont.)

- The control C acts like an input to the other 2 inputs. The circuit functions only when C = 1 and remain the output as it is when C = 0.
- Characteristics:
  - **Set State: when output Q = 1 and Q' = 0 (C=1, S=1, R=0)**
  - **Reset State: when output Q = 0, Q' = 1 (C=1, S=0, R=1)**
  - **Remain unchanged: C = 0**
  - **An indeterminate condition occurs when all 3 inputs are equal to 1.**

D Latch

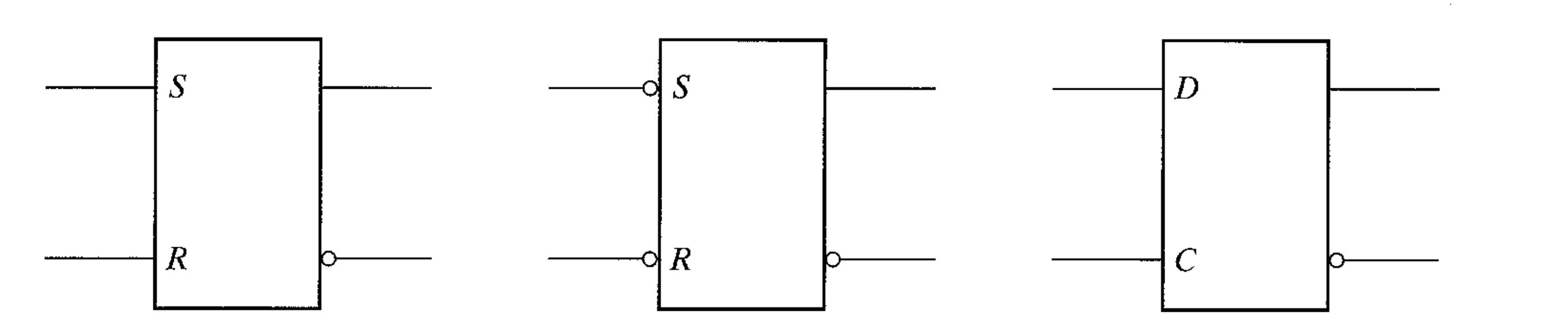
- D **(Delay)** latch is designed **to eliminate the indeterminate condition in the SR latch.**
- D latch ensures that inputs S and R are never equal to 1 at the same time.
- S = D, R = $\overline{D}$, thus **R ≠ S**.



C	D	Next state of Q
0	X	No change
1	0	$Q = 0$; Reset state
1	1	$Q = 1$; Set state

Graphical Symbol of Latches

- The graphical symbol for various latches is shown below.
- The bubble indicates the complement input/output.



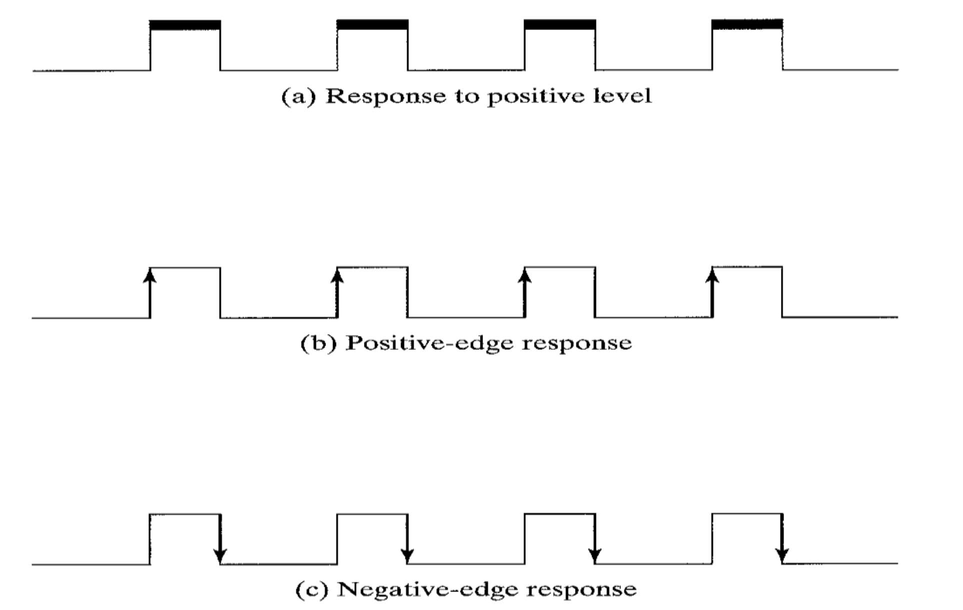
SR latch

$\bar{S}\bar{R}$ latch

D latch

Triggering Flip – Flops

- The state of a flip-flop is switched by a momentary change in **clock signal** that acts as a control input that triggers.
- 3 types of trigger signal:
  - Positive level trigger
  - Positive edge trigger
  - Negative edge trigger



(a) Response to positive level

(b) Positive-edge response

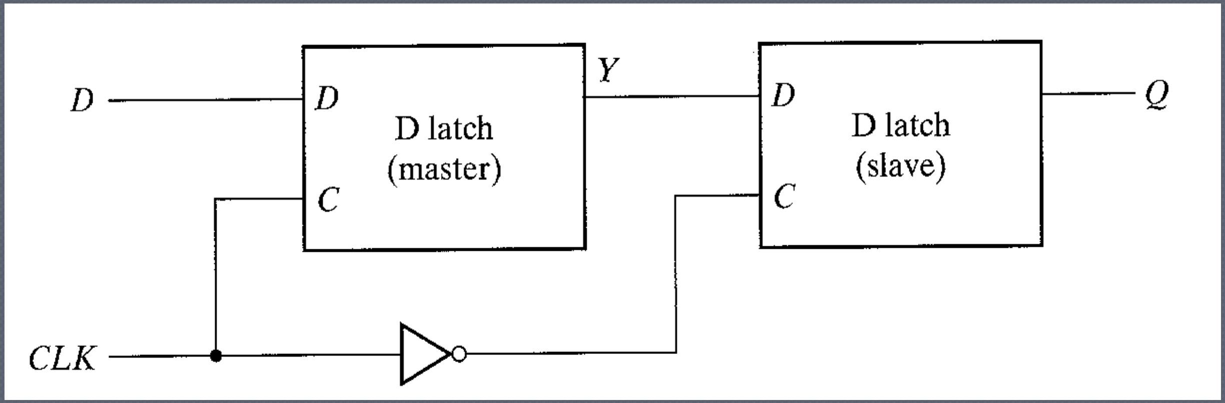
(c) Negative-edge response

Triggering Flip – Flops (cont.)

- Positive level trigger:
  - Allows changes in the output when the input changes while the clock pulse stays at logic '1'
  - Problem: **if more than 1 changes** happen at the input signal and **output will keep on changing** following the input signal as long as the trigger signal still stay in positive level, thus causing confusion
- Edge trigger:
  - **Preferred solution** to avoid confusion.
  - Edge trigger can be **positive** (during '0' to '1' transition) or **negative** (during '1' to '0' transition)
  - In this Module, we use different D-flip flop implementations to demonstrate the example of positive and negative edge flip flops.

Negative Edge Triggerred D Flip–Flop using 2 D-latches

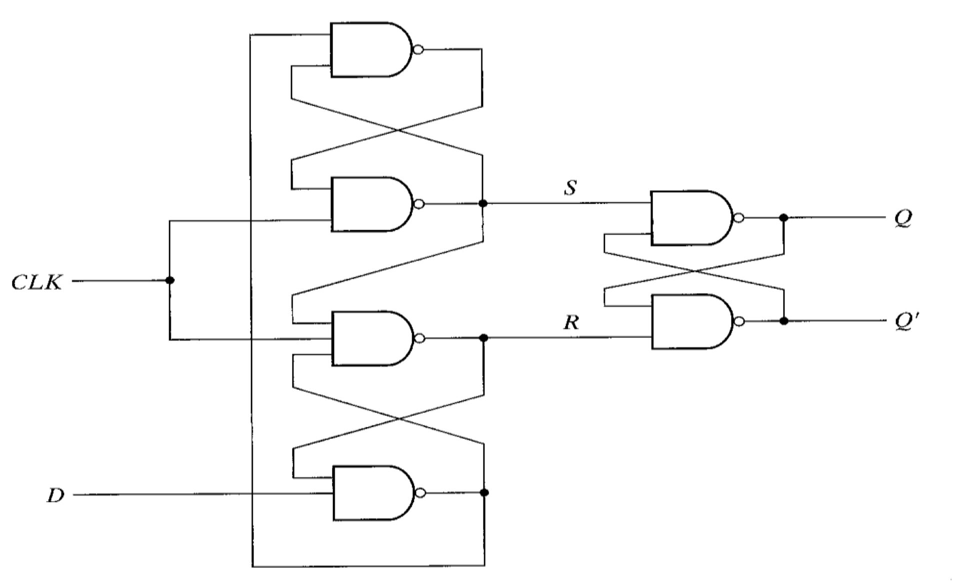
- D flip-flop can be constructed with **two D-latches.**



- Properties:
  - When **CLK is 1**, **master D latch is enabled** but **slave D latch is disabled**. **Input (D)** will be transferred to **Y**.
  - When **CLK is 0, slave D latch is enabled** but **master D latch is disabled**. **Data (Y)** will be transferred to **Q**.
  - Thus, changes in output occur only **during transition from '1' to '0'** (negative edge trigger D flip-flop).

Positive Edge Triggerred D Flip-Flop using 3 SR-latches

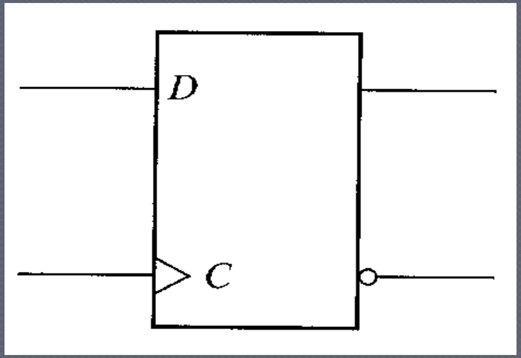
- D flip flop can also be constructed using three NAND coupled SR latches.



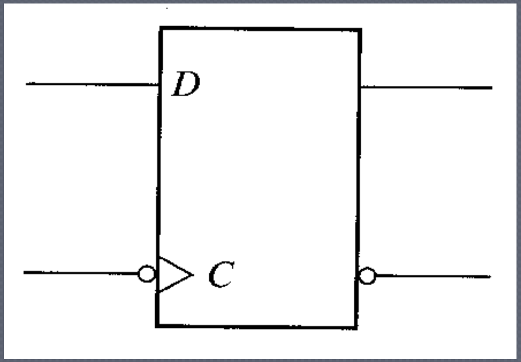
- Properties:
  - When CLK is 0, (regardless of D) both S and R remains 1, thus Q and Q' remains at the previous state (no changes)
  - When CLK is 1, if D = 1, then S = 0, R = 1, thus Q = 1, Q' = 0
  - When CLK is 1, if D = 0, then S = 1, R = 0, thus Q = 0, Q' = 1
  - Thus, changes in output occur only **during transition from '0' to '1'** (positive edge trigger D flip-flop).

Graphical Symbol of Flip Flops

- The graphical symbol for different edge triggered D flip-flops is shown below.
- The bubble indicates the complement input/output.
- The arrowhead symbol in front of C indicates that the flip-flop responds to edge triggering



+ edge triggered D flip flop



- edge triggered D flip flop

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End of Module 12