UNIVERSITI TENAGA NASIONAL

College of Information Technology

BACHELOR OF COMPUTER SCIENCE (HONS.)

FINAL EXAMINATION
SEMESTER I 2013/2014

DIGITAL LOGIC DESIGN
(CSNB163)

September 2013

Time allowed: 3 hours + 10 minutes for reading

INSTRUCTIONS TO CANDIDATES

1. The total marks for this exam is 100 marks.
2. There are **THREE (3) SECTIONS** to this paper: Section A, Section B and Section C.
3. Answer **ALL** questions in the answer booklet provided.

DO NOT OPEN THIS QUESTION PAPER UNTIL YOU ARE INSTRUCTED TO DO SO

THIS QUESTION PAPER CONSISTS OF 9 PRINTED PAGES INCLUDING THIS PAGE

SECTION A: OBJECTIVE QUESTIONS (10 QUESTIONS, 10 MARKS)
Instruction: Answer all TEN (10) questions.

1. Convert binary 111111110010 to hexadecimal.

   A. $EE2_{16}$ B. $FF2_{16}$ C. $2FE_{16}$ D. D. $FD2_{16}$

2. Convert the binary number 1001.0010 to decimal.

   A. 90.125 B. 9.125 C. 125 D. 12.5

3. _____ gives a HIGH (1) output if both or either one of the inputs are HIGH (1).

   A. XNOR gate
   B. OR gate
   C. XOR gate
   D. NAND gate

4. In parity system, there is either_____ or _____ parity. To implement parity system will add an extra _____ to the digital information being transmitted.

   A. positive, negative, byte
   B. odd, even, bit
   C. upper, lower, digit
   D. on, off, decimal

5. The following is an important feature of the sum-of-products (SOP) form of Boolean expression:

   A. No signal must pass through more than two gates, not including inverters.
   B. The delay times are greatly reduced over other forms.
   C. The maximum number of gates that any signal must pass through is reduced by a factor of two.
   D. All logic circuits are reduced to nothing more than simple AND and OR gates.

6. What is the most simplified Sum of Product expression for: F = ABD + CD + ACD + ABC + ABCD.

   A. F = ABD + ABC + CD
   B. F = CD + AD
   C. F = BC + AB
   D. F = AC + AD

7. What are the outputs of a 4-bit comparator given the inputs A = 1100 and B = 1001?

   A. $A > B = 1, A < B = 0, A < B = 1$

   B. $A > B = 1, A < B = 0, A = B = 0$

   C. $A > B = 0, A < B = 1, A = B = 1$

   D. $A > B = 0, A < B = 1, A = B = 0$

8. What are the two types of basic adder circuits?

   A. sum and carry

   B. half-adder and full-adder

   C. asynchronous and synchronous

   D. one- and two's-complements.

9. How many possible outputs would a decoder have with a 6-bit binary input?

   A. 16 B. 32 C. 64 D. 128

10. Which of the following is correct for a D latch?

   A. The output toggles if one of the inputs is held HIGH.

   B. Q output follows the input D when the enable is HIGH.

   C. Only one of the inputs can be HIGH at a time.

   D. The output complement follows the input when enabled.

SECTION B: TRUE/FALSE QUESTIONS (10 QUESTIONS, 10 MARKS)

Instruction: Answer all TEN (10) questions by making a circle around T if the statement is TRUE or F if the statement is FALSE.

1. The Hexadecimal number system consists of eight digits, 0 through 7. T / F

2. A decimal fraction can be converted to binary by using the repeated division-by-2 method. T / F

3. The 2's complement of a binary number is derived by adding 1 to the 1's complement. T / F

4. The sum-of-product (SOP) is sum of a number of terms that consists of ANDed terms. T / F

5. The process of reduction or simplification of combinational logic circuits increases the cost of the circuit. T / F

6. Even parity is the condition of having an even number of 1s in every group of bits. T / F

7. In a priority encoder, the input with the highest priority is represented on the output. T / F

8. An input which can only be accepted when an enable or trigger is present is called asynchronous. T / F

9. In a multiplexer, the data select control inputs are responsible for determining which data input is selected to be transmitted to the data output line. T / F

10. A positive edge-triggered flip-flop changes states with a HIGH-to-LOW transition on the clock input. T / F

SECTION C: SUBJECTIVE QUESTIONS (5 QUESTIONS, 80 MARKS)

Instruction: Answer ONLY FIVE (5) questions out of the SIX (6) questions.

Questions 1

(a) Convert the following:

i. ABC_{16} to Decimal

ii. 1101101_2 to Hexadecimal

iii. 47_8 to Hexadecimal

[6 marks]

(b) Convert 32.22310 to binary.

[2 marks]

(c) Find the 10s complement of 76.

[2 marks]

(d) Show the subtraction process of 43210 – 34510 performed using 2's complement.

[6 marks]

Questions 2

Given the following Boolean expression:

F = W'X'Y'Z + W'X'YZ' + W'X'YZ + WX'YZ' + WXY'Z + WXYZ'

(a) Draw the circuit diagram.

[3 marks]

(b) Using Karnaugh Maps find the minimized expression. Indicate clearly the minimized terms.

[6 marks]

(c) Draw the circuit diagram of the minimized expression.

[4 marks]

(d) Implement the circuit using only NAND gates

[3 marks]

Questions 3

Figure 1 shows a combinational logic circuit:

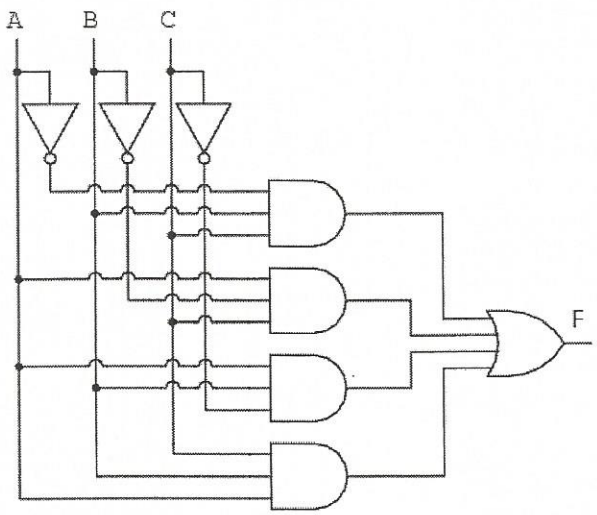

Figure 1

(a) Write the Boolean expression for F in the form of the sum of minterms.

[4 marks]

(b) Find the minimized expression for F.

[4 marks]

(c) Draw the circuits of the minimized expressions. Compare the savings in term of the number of gates used in original and in the minimized expression.

[4 marks]

(d) Draw the circuits of the minimized expressions using only NAND gates.

[4 marks]

Questions 4

A logic circuit has two inputs labeled A and B and an output, F. These inputs give the output F depending on two other inputs X and Y. If both X and Y are 0, then F gives the NOR of A and B, else if X is 0 and Y is 1, F is XNOR of A and B, else if X is 1 and Y is 0, F is NAND of A and B and finally if both X and Y are 1, F is an XOR of A and B.

(a) Obtain the truth table and the Boolean expression for F.

[4 marks]

(b) Draw the Karnaugh map for the expression.

[4 marks]

(c) Obtain the minimized expression.

[4 marks]

(d) Draw the final logic circuit for F.

[4 marks]

Questions 5

(a) Show using an example, the truth tables and the Boolean expressions of a half adder. Draw the circuit diagram of a half adder.

[6 marks]

(b) What is the difference between a full adder and a half adder? Construct the circuit diagram for a full adder using the half adders.

[4 marks]

(c) The multiplication of 2 binary numbers is to be done using a multiplier. The first number must be 5 bit (multiplier) and the second number must be 4 bit (multiplicand). How many AND gates are required? What kind of adders is required? How many resulting bits is the output of the multiplier?

[6 marks]

Questions 6

(a) Describe the differences between combinational logic circuit and sequential logic circuit.

[4 marks]

(b) Differentiate between the following logic circuits:

i. SR latch

ii. D latch

[4 marks]

(c) Explain the operation of the flip-flop in the following figure 2:

[8 marks]

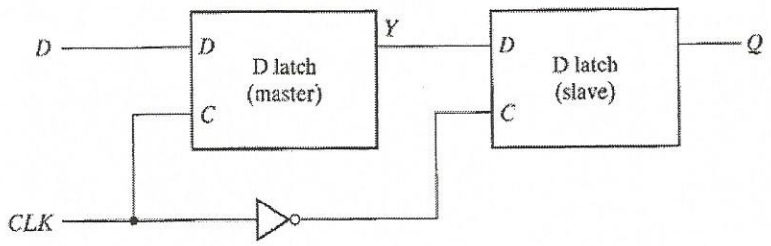

Figure 2

---End of Questions---

APPENDIX

Theorems and Postulates of Boolean Algebra

1.	Postulate 1	(a) $x + 0 = x$	(b) $x.1 = x$
2.	Postulate 2	(a) $x + x' = 1$	(b) $x.x' = 0$
3.	Theorem 1	(a) $x + x = x$	(b) $x \cdot x = x$
4.	Theorem 2	(a) $x + 1 = 1$	(b) $x \cdot 0 = 0$
5.	Theorem 3, involution	(a) $(x')' = x$	
6.	Postulate 3, commutative	(a) $x + y = y + x$	(b) $xy = yx$
7.	Theorem 4, associative	(a) $x + (y + z) = (x + y) + z$	(b) $x(yz) = (xy)z$
8.	Postulate 4, distributive	(a) $x(y + z) = xy + xz$	(b) $x + yz = (x + y)(x + z)$
9.	Theorem 5, De Morgan	(a) $(x + y)' = x'y'$	(b) $(xy)' = x' + y'$
10.	Theorem 6, Absorption	(a) $x + xy = x$	(b) $x(x + y) = x$