

Laboratory 1: Introduction to TTL 74 series basic logic gates and the digital logic experimenter kit.

Equipment - IDL800 digital experimenter
7400
7402
7408
7432
7486.

Keywords - SSI, MSI, LSI, VLSI, IC, chip, gate, truth table, Boolean equation, AND, OR, NOT, NAND, NOR, EXOR, low power Schottky (LS), TTL, combinational circuit and trouble shooting.

Objectives

1. Understand all keywords.
2. Construct and investigate the behavior of simple logic gates and simple logic circuits using TTL components.
3. Learn to find necessary practical information about the TTL 74 series from data sheets.
4. Construct truth tables.
5. Learn features of IDL800 Digital Lab Experimenter.

Reference Materials

1. Contemporary Logic Design, Randy H. Katz.
2. Digital Systems, Ronald J. Tocci.
3. IDL800 Assembly Manual.
4. Digital Fundamental, Thomas L. Floyd

Introduction

1.0 Digital Integrated Circuits (ICs) and the TTL 74 series.

1.1 Digital Integrated Circuits (ICs).

Digital ICs are a collection of resistors, diodes and transistors fabricated on a single piece of semiconductor material usually silicon and referred to as “chip”. The chip is enclosed in a protective plastic or ceramic package with pins extended out for connecting the IC to other devices. The most common type of package is a dual-in-line package (DIP) as shown in figure 1.1. The pins are numbered counterclockwise when viewed from the top of the package with respect to an identifying notch or dot at one end of the chip. The DIP below is a 14-pin package. 16, 20, 24, 28, 40 and 64 pin packages are also available.

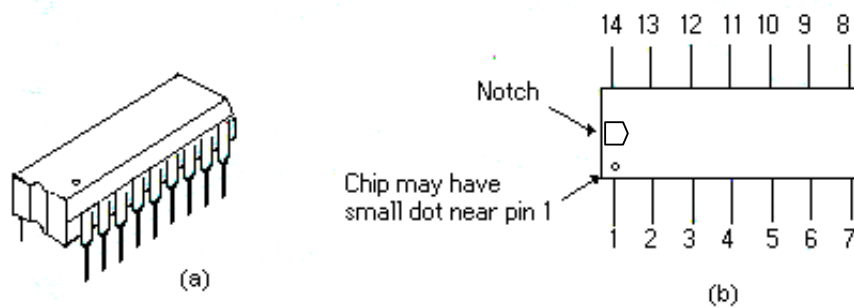


Figure 1.1 (a) Dual-in-line package.
(b) Top view showing pin numbers.

The fabricated resistors, diodes and transistors reside in the chip are called logic gates. Different chip may contain different amount of these logic gates.

Digital ICs are often categorized according to their circuit complexity as measured by the number of equivalent logic gates in an IC. There are currently five standard levels of complexity as in Table 1.1.

<u>Complexity</u>	<u>Approximate number of gates per chip in commercial products.</u>	<u>Typical products</u>
Small-scale integration (SSI).	Less than 12.	Logic gates, flip-flops.

Medium-scale integration (MSI).	12 to 99.	Counters, multiplexers, adders.
Large-scale integration (LSI).	100 to 9999.	8 bit microprocessors, ROM, RAM.
Very large-scale integration (VLSI)	10,000 to 99,999	16 and 32 bit microprocessors, sophisticated peripherals.
Ultra large-scale integration (ULSI)	100,000 or more.	64 bit microprocessors, special processors, real time image processing.

Table 1.1

All the ICs that will be used in Laboratory 1 are ICs of the SSI category. With ICs, electronic circuits become much smaller and less expensive. This expanded the uses of electronics to various sectors such as industrial, telecommunication, aerospace, computers, calculators and home appliances. Modern electronics using ICs is rapidly becoming the “brains and nerves” of our complex society.

1.2 TTL 74 series

The TTL 74 series is the most widely used family of digital ICs in the SSI and MSI categories. Figure 1.2 shows a standard TTL inverter circuit. Notice that it contains several bipolar transistors and this is how the name TTL (transistor-transistor logic) comes.

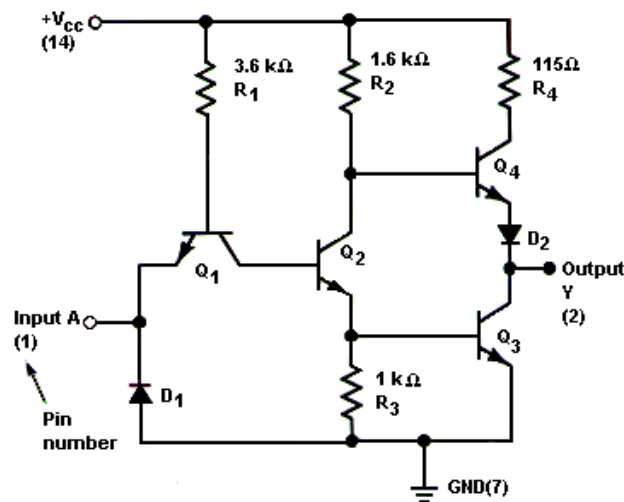


Fig 1.2 TTL inverter circuit

The TTL logic family actually consists of several subfamilies or series. Table 1 –2 lists the name of each TTL series together with the prefix designation used to identify different ICs as being part of that series. The differences between the various TTL series are in their electrical characteristics such as power dissipation, delay times and switching speed. They do not differ in the pin layout or logic operations performed by the internal circuitry.

	74	74s	74LS	74AS	74ALS	74F
Performance rating	9	3	9.5	1.7	4	3
Propagation delay (ns)	10	20	2	8	1.2	6
Power dissipation (mW)	90	60	19	13.6	4.8	18
Speed-power product (pJ)	35	125	45	200	70	100
Max. clock rate (MHz)	10	20	20	40	20	33

1.2.1 TTL Inputs

Power and Ground

Referring to Figure 1.1, all TTL ICs have a dc power supply voltage connected to one of their pins labeled Vcc and ground to another which is labeled as GND. VCC in the range of 4.5V to 5.5V is required. Typically 5V power supplies are used. TTL ICs will not work reliably with dc supply voltages outside of this recommended range and will likely be destroyed if the recommended maximum of 5.5v is exceeded.

Logic level voltage ranges

Figure 1.3 shows the logic-level voltage ranges for TTL ICs. A logic 0 is any voltage in the range from 0 to 0.8V and a logic 1 is any voltage from 2V to 5V. Voltages that are not in either of these ranges are said to be indeterminate and should not be used as inputs to any TTL device.

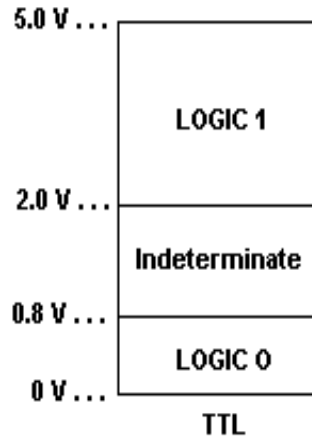


Figure 1.3 Logic level voltage ranges for TTL ICs.

Unconnected (floating) Inputs







If a TTL input is left unconnected, the gate generally reacts as though the input was high. However, an open TTL input is noise-prone. So the high state is not reliable. If only one gate is being used on a multiple gate chip, the inputs to the unused gates may be left open in the breadboard construction in the lab.

2.0 TTL Data Book

This is the manufacturer Data Book which is one of the most important books you will use while working with integrated circuits (ICs). It tells you all the specifications and functions of the particular chip that you need to use to work on your experiments or projects. Also from the Data Book you could know all the ICs that are available for use to perform the functions that you would require for the experiments or the projects assigned.

3.0 Basic logic gates

A logic gate is the simplest device used to construct digital circuits. Logic gates basically have one or more inputs and only one output. The circuits respond to various input combinations and a truth table shows this relationship between the input combinations and its output. Familiarization with a logic circuit's truth table is essential to the technologist or technician before the person can design with or troubleshoot the circuit. Various types of logic gates are available such as inverters (NOT), AND, OR, NAND, NOR, EXOR and EXNOR, each with its own unique logic function.

Gate Name	Gate symbol and Boolean equation	Truth Table															
NOT	input x →  output y Boolean equation: $y = \bar{x}$	<table border="1"> <thead> <tr> <th>input, x</th> <th>output, y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> </tr> </tbody> </table>	input, x	output, y	0	1	1	0									
input, x	output, y																
0	1																
1	0																
OR	inputs x, y →  output z Boolean equation: $z = x + y$	<table border="1"> <thead> <tr> <th>input, x</th> <th>y</th> <th>output, z</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	input, x	y	output, z	0	0	0	0	1	1	1	0	1	1	1	1
input, x	y	output, z															
0	0	0															
0	1	1															
1	0	1															
1	1	1															
AND	inputs x, y →  output z Boolean equation: $z = x \cdot y$	<table border="1"> <thead> <tr> <th>input, x</th> <th>y</th> <th>output, z</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	input, x	y	output, z	0	0	0	0	1	0	1	0	0	1	1	1
input, x	y	output, z															
0	0	0															
0	1	0															
1	0	0															
1	1	1															
NAND	inputs x, y →  output z Boolean equation: $z = \overline{x \cdot y}$	<table border="1"> <thead> <tr> <th>input, x</th> <th>y</th> <th>output, z</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	input, x	y	output, z	0	0	1	0	1	1	1	0	1	1	1	0
input, x	y	output, z															
0	0	1															
0	1	1															
1	0	1															
1	1	0															
NOR	inputs x, y →  output z Boolean equation: $z = \overline{x + y}$	<table border="1"> <thead> <tr> <th>input, x</th> <th>y</th> <th>output, z</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	input, x	y	output, z	0	0	1	0	1	0	1	0	0	1	1	0
input, x	y	output, z															
0	0	1															
0	1	0															
1	0	0															
1	1	0															
EXOR	inputs x, y →  output z Boolean equation: $z = x \oplus y$ $= \bar{x}y + x\bar{y}$	<table border="1"> <thead> <tr> <th>input, x</th> <th>y</th> <th>output, z</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	input, x	y	output, z	0	0	0	0	1	1	1	0	1	1	1	0
input, x	y	output, z															
0	0	0															
0	1	1															
1	0	1															
1	1	0															

3.1 NOT gate

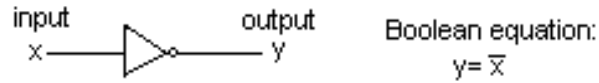


Fig 1.4 NOT gate symbol.

input, x	output, y
0	1
1	0

Table 1.3 Truth table for NOT gate.

The NOT gate available in the TTL 74 series is 7404. Referring to the TTL Data Book for 7404 IC, there are six inverters packed in a package. Each 7404 inverter IC, has one voltage supply pin, Vcc and one ground pin, GND that provide power to all the six inverters.

3.2 OR gate

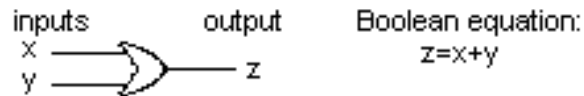


Figure 1.5 OR gate symbol (2 input OR gate)

input, x y	output, z
0 0	0
0 1	1
1 0	1
1 1	1

Table 1.4 Truth table for OR gate

The two input OR gate available in the TTL 74 series is 7432. There are four OR gates in this package (IC chip).

3.3 AND gate

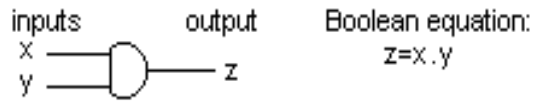


Figure 1.6 AND gate symbol (Two inputs)

input, x y		output, z
0	0	0
0	1	0
1	0	0
1	1	1

Table 1.5 Truth table for AND gate

The two input AND gate available in the 74 series is 7408. There are four AND gate in this IC chip.

3.4 NAND gate

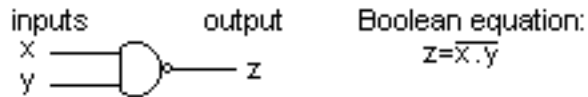


Figure 1.7 NAND gate symbol (two inputs)

input, x y		output, z
0	0	1
0	1	1
1	0	1
1	1	0

Table 1.6 Truth table for NAND gate

The output of NAND logic is actually the invert of AND. The two input NAND gate available in the 74 series is 7400. There are also four NAND gates in this IC chip.

3.5 NOR gate

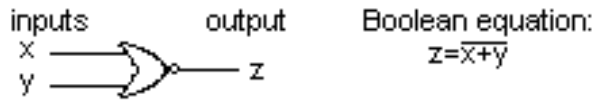


Figure 1.8 NOR gate symbol (Two inputs)

inputs		output,
x	y	z
0	0	1
0	1	0
1	0	0
1	1	0

Table 1.7 Truth table for NOR gate

The output of NOR logic is actually the invert of OR. The two inputs OR gate available in the 74 series is 7402. There are also four NOR gates packed in this IC chip.

3.6 EXOR gate

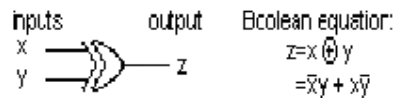


Figure 1.9 EXOR gate symbol

inputs		output,
x	y	z
0	0	0
0	1	1
1	0	1
1	1	0

Table 1.8 Truth table for EXOR gate

EX-OR actually the abbreviation of exclusive OR. The EXOR gate available in the 74 series is 7486. There are also four EXOR gates packed in this IC chip.

More information regarding the TTL 74 series gates and ICs could be found in the Manufacturer's Data Book (TTL Data Book).

4.0 **Combinational Circuit**

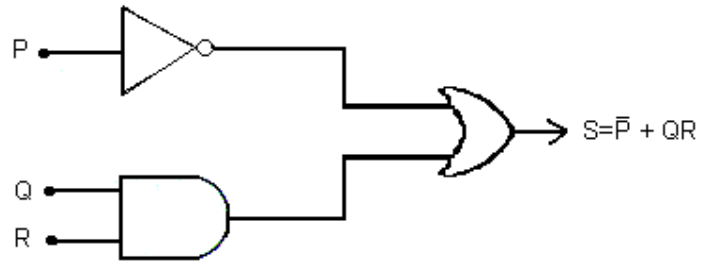


Fig 1.10

Combinational logic circuits are constructed by interconnecting various logic gates together to implement a particular circuit function. The combinational logic circuit in Fig 1.10 using many gates can also be easily represented in a logic truth table as given in Table 1.9

P	Q	R	S
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Table 1.9 Truth table for combinational circuit in Fig 1.10.

The circuit in Fig 1.10 can also be implemented using all NAND gates only. The equivalent NAND gates implementation is given in Fig. 1.11.

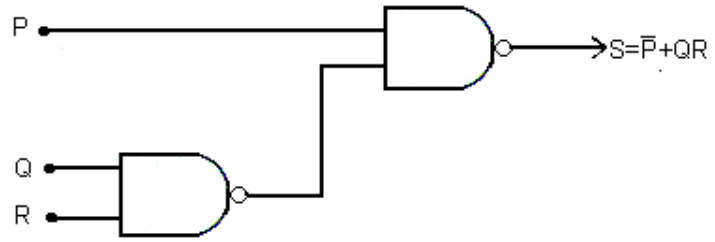
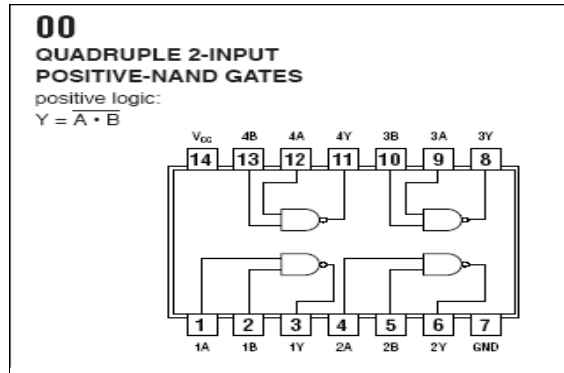


Fig 1.11 NAND gates implementation of combinational circuit in Fig. 1.10.

Prelab Exercises

- In your log book, draw all the gates within each TTL chip for the following gates: NOT, OR, AND, NOR, NAND and EXOR.

For example: NAND gate



- In your drawing, name the number of the TTL equivalent ICs for all the gates above.

-



FIG 1.12

- For the circuit in Fig 1.12 complete the truth table below:

inputs		output,
X		Z
0		
1		

- Write the Boolean Equation for the output Z.
- Indicate on the diagram in Fig 1.12 the pin numbers that you would use to implement the circuit in the lab.

4.

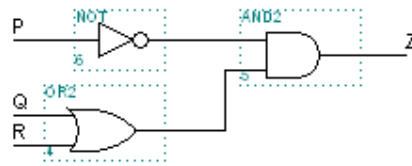


FIG 1.13

Redraw the combinational circuit in Fig 1.13, and its truth table in your log book.

State the following:

- The type of gates.
- The equivalent TTL IC number.
- Assign the pin numbers that you would use to make connections to the circuits in the lab.
- The quantity of ICs (chips) that should be used for circuit implementation with TTL 74 series ICs.

Laboratory Experiments

1.0 Basic gates

- 1.1 Place the 7404 NOT gate on the experimenter breadboard. Connect pin 7 (GND pin) to ground and pin 14 (Vcc pin) to +5V supply of the experiment.
- 1.2 Apply all the input combinations to the input pin of the 7404 IC. Refer to the truth table in the pre lab exercises. Use the input pin that you have assigned in the pre lab exercises.

(Note : Apply only one input combination (if the gate has more than one input) at a time. You will use the switches on the experimenter as inputs to the ICs. An 'ON' switch on the experimenter will give a logic 1 and on 'OFF' switch will produce a logic 0. The outputs from the ICs will be connected to the LEDs on the experimenter. A logic 1 output will light up the LED on the experimenter while a logic 0 will OFF the LED. Refer to the Appendix for some useful tips and guidelines for hardware experiments).

- 1.3 Verify the truth table for the gates. Record your observations in the log book (in truth table form)..
- 1.4 Is this IC functioning corectly?
- 1.5 Repeat procedure 1.1 to 1.4 for the following gates:
OR, AND, NAND, NOR and EXOR.
- 1.6 Assemble the circuit as in Fig. 1.12 in the pre lab exercises. Remember to connect the **Vcc and GND** pins appropriately. Use the pin assignments that have been made in the prelab exercises.
- 1.7 Apply all the input combinations and verify your output with reference to the truth table in 3(a) of the prelab exercises. Record your observations in the log book (in truth table form).

2.0 Combinational logic

- 2.1 Assemble the circuit in Figure 1.13. Use the pin assignments that you have made in the pre lab exercises. Remember to correctly connect the **Vcc and GND** pins for every IC in use.
- 2.2 Apply all the input combinations and verify its output with reference to the truth table.
Record all your observations in the log book (in truth table form)..
- 2.3 If there is any unmatched result, troubleshoot your circuit.
- 2.4 If your circuit is functioning accordingly, demonstrate your circuit, to the lab demonstrator and get his/her approval that your circuit is working.

Report:

There is no report for this experiment